FUZZY LOGIC CONTROLLED DISTRIBUTED POWER FLOW CONTROLLER FOR VOLTAGE REGULATION OF TEN-BUS SYSTEM

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ABSTRACT

This paper deals with the comparison of responses of Buck-Boost Fed PV and Inverter System (BBPVIS) with PID and FLC controllers. The output of PV array is stepped up using Buck-Boost converter and its output is converted to fifty hertz AC using an inverter. LCLC filter is proposed at the output of the inverter to reduce the harmonics. Closed loop PID & FLC based BBPVIS system is modeled, simulated and the corresponding results are presented. The results of comparison with PID and FLC controller show a reduction in the peak value of current. The simulation results indicate that the time domain response with FL controller is superior to the PID controlled system.

1. INTRODUCTION

The proposed work deals with the comparison of the PID and Fuzzy Logic controlled closed loop DPFC systems. The voltage across the load decreases due to the addition of extra load and the load voltage is restored back to the normal value by using the closed-loop system.. The simulation studies for closed-loop systems are performed on a standard two-bus radial test system and the results are presented.

This research deals with modelling and tuning of the ten-bus system with closed loop Fuzzy Logic controlled DPFC systems. The result of comparison with PID and Fuzzy Logic controller shows a reduction in the peak value of current. FLC is observed to provide better control than other controllers. The results of comparison with and without hysteresis controller show reduction in the peak value of current and THD content. . From the consumer point of view, any problem occurring about current, voltage or the frequency deviation that results in a power failure is called power quality problems. L. Gyugyi, (1992) have depicted Unified Power-Flow Control Concept for Flexible AC Transmission Systems [1]. Y. Ikeda and T. Kataoka (2005) have depicted a UPFC based voltage compensator with current and voltage balancing function [2]. Z. Yuan, et al (2007) has introduced a new facts component: Distributed Power Flow Controller (DPFC)[3].

S. MasoudBarakatietal (2011) have introduced Voltage Sag and Swell Compensation with DVR Based on a symmetrical Cascade Multi- cell Converter [11]. Zhihui Yuan et al (2009) have modelled DPFC control during shunt converter failure [12]. R. Lokeswar Reddy and K. Vasu (2012) have gone for the technology of designing the Distributed Power Flow Controller [13]. L.

Gyugvi et al (1995) have developed the Unified Power Flow Controller as a new approach to power transmission control [14].

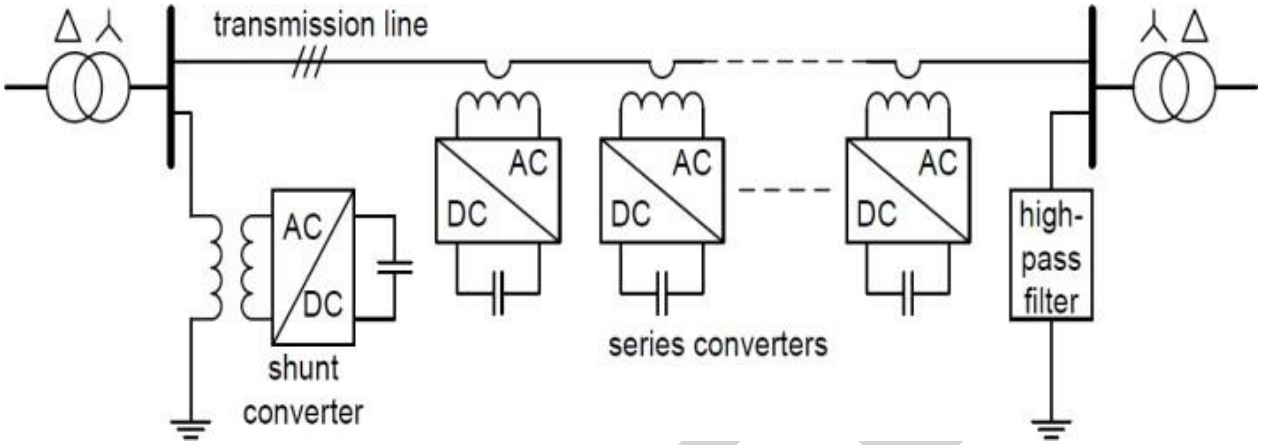


Fig.1 Structure of DPFC

The Distributed Power Flow Controller (DPFC) recently presented as a powerful device within the family of FACTS devices, which provides much lower cost and higher reliability than conventional FACTS devices. It is derived from the UPFC and has the same capability of simultaneously adjusting all the parameters of the power system: line impedance, transmission angle, and bus voltage magnitude.

2. PRINCIPLE OF DPFC

Multiple individual converters co-ordinate together and compose the DPFC. The converters connected in series with the transmission lines are the series converters. They can inject a controllable voltage at the fundamental frequency; consequently, they control the power flow through the line. The converter connected between the line and ground is the shunt Converter. The function of the shunt converter is to compensate reactive power to the grid and to supply the active power required by the series converter. In a normal UPFC, there is active power exchange through the DC link that connects the series converter with the shunt converter.

Since there is no common DC link between the shunt and series converters in the DPFC, the active power is exchanged by harmonics and through the AC network. The principle is based on the definition of active power, which is the mean value of the product of voltage and current, where the voltage and current comprise fundamental and harmonics. Since the integrals of all the cross product of terms with different frequencies are zero, the time average active power can be expressed by:

$$P = \sum_{n=1}^{\infty} V_n I_n \cos\phi_n \qquad (1)$$

Where *n* is the order of the harmonic frequency and ϕ_n *is* the angle between the current and voltage of the nth harmonic. Equation 1 describes that active powers at different frequencies are isolated from each other and that voltage or current in one frequency component has no influence on other frequency components. The third harmonic is chosen here to exchange the active power, because Y-Δ transformers can easily filter it.

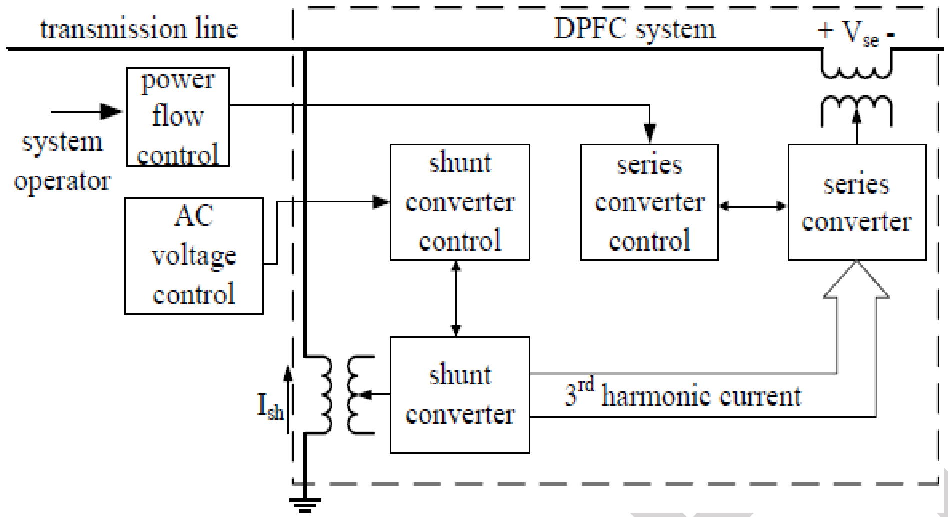


Fig.2 Block diagram of the control of a DPFC

3. SIMULATION RESULTS

Ten-bus system with DPFC and PID controller

Ten-bus system with DPFC and PID controller is shown in figure 3.1. The receiving end voltage is shown in figure 3.2The receiving end current is shown in figure 3.3. the real and reactive power is shown in 3.4

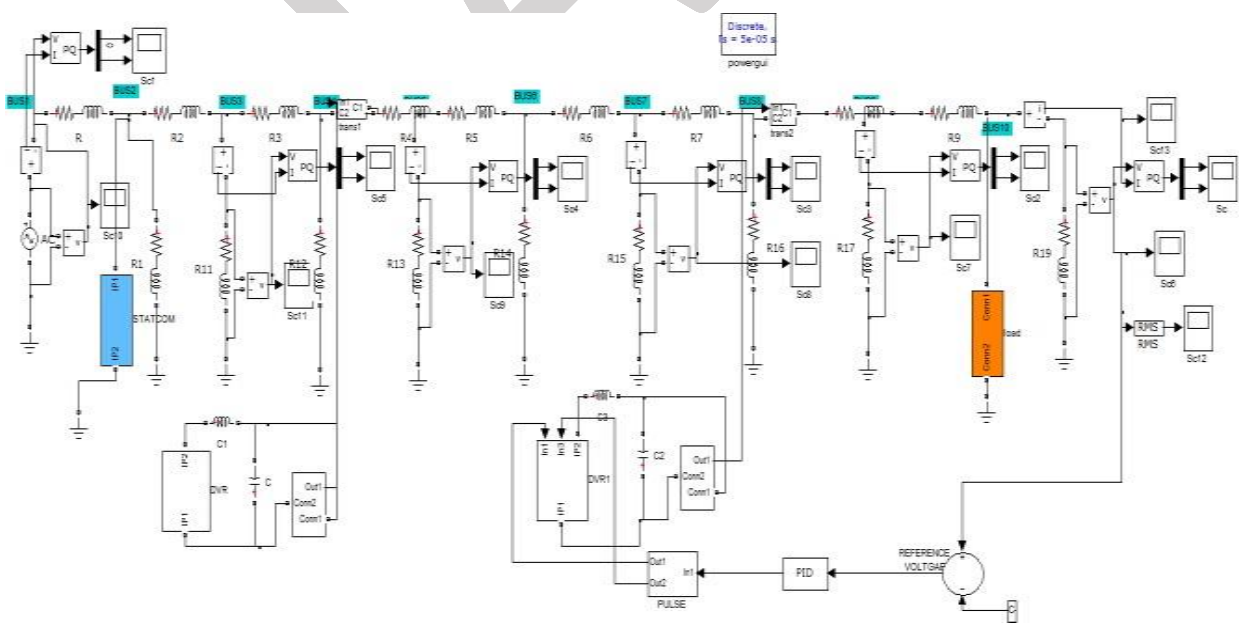


Fig 3.1 Ten-bus system PID controller

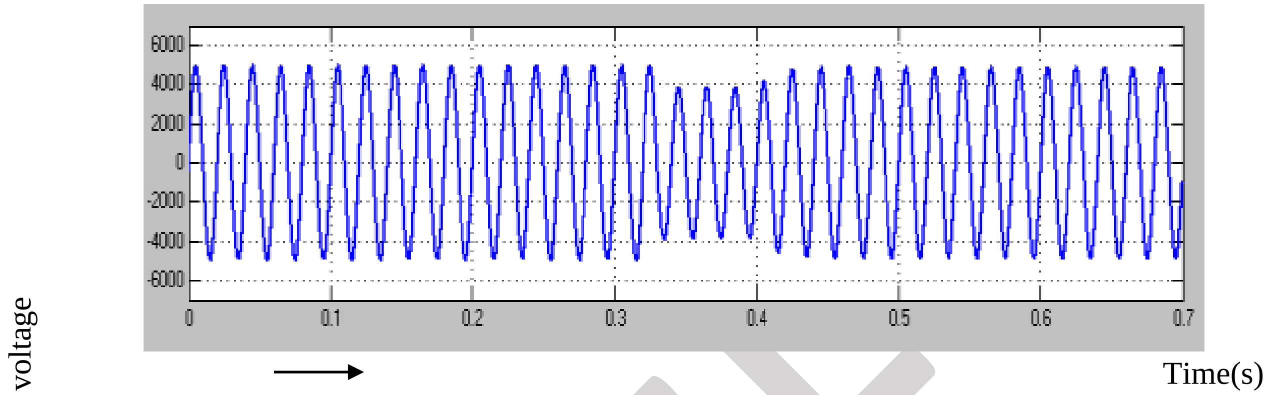


Fig 3.2 Output voltage

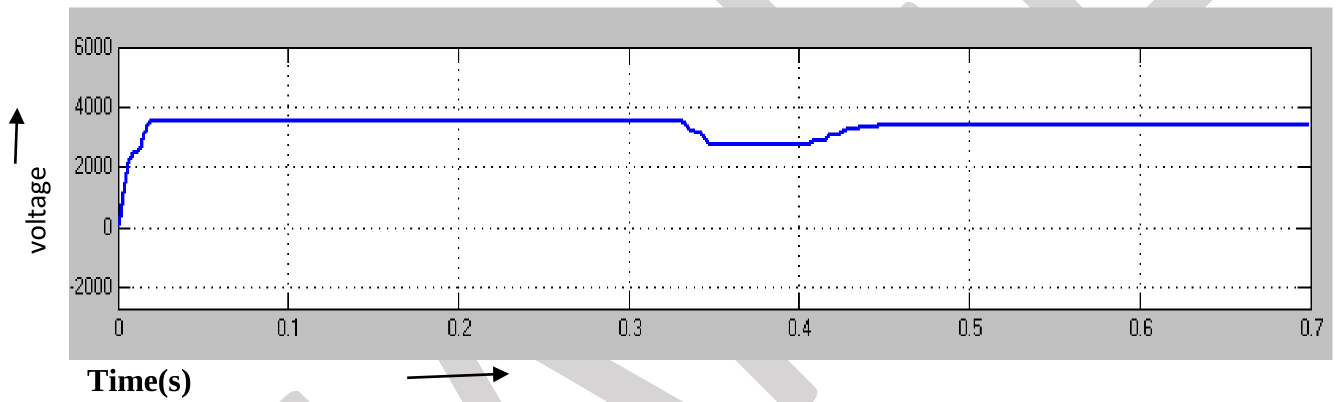
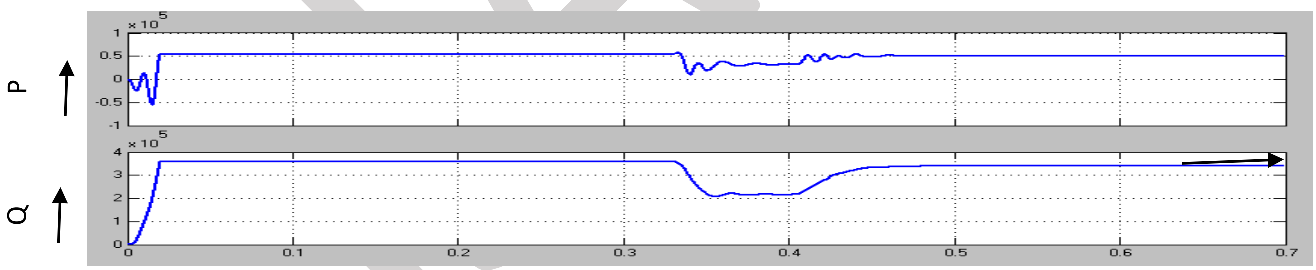


Fig 3.3 RMS voltage



Ten-bus system with DPFC and FLC controller

The Closed loop system with the Fuzzy logic controller is shown in Fig 4.1 The output voltage is shown in Fig 4.2 and its value is 5000 volts. The RMS output voltage is shown in Fig

4.3 and its value is 3800 volts. The Real power & Reactive power is shown in Fig 4.4.

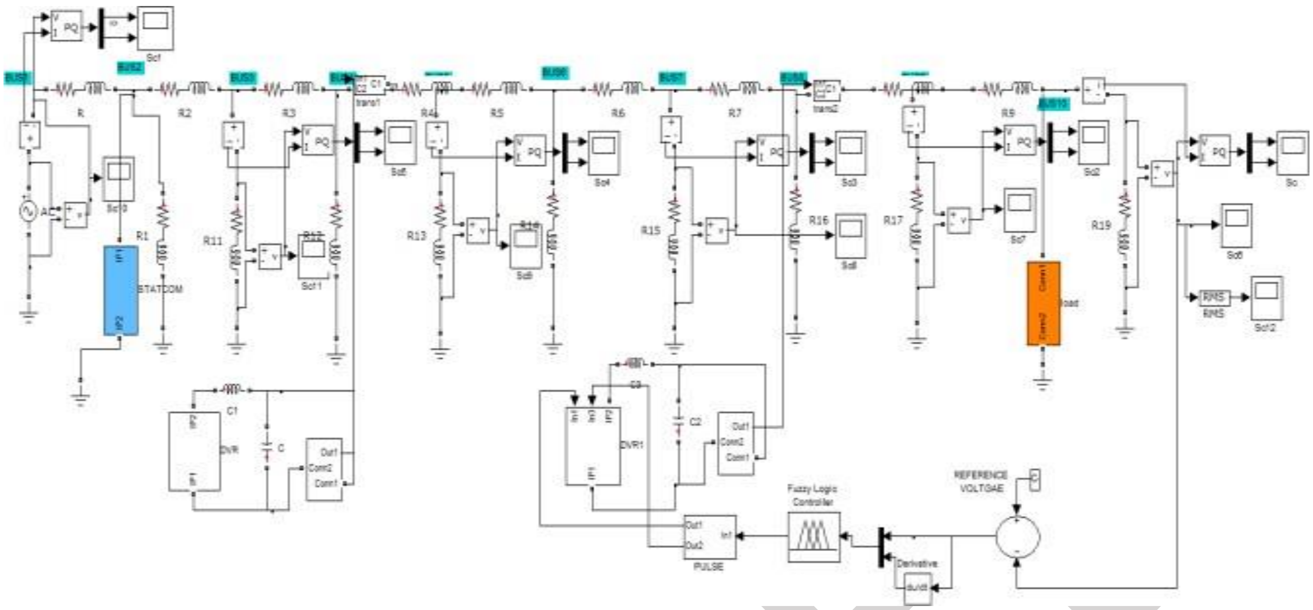


Fig 4.1 Closed loop system with Fuzzy logic controller

The Time domain parameters are given in Table-1. It is noticed that the peak time is reduced from 0.35s to 0.33s. The setting time is reduced from 0.45s to 0.36s and steady-state error is also reduced from 9.3s to 0.09s. The comparison of time domain parameter like rise time, setting time, peak time, and steady-state error for both PID and FL controllers is tabulated in Table 3.3.

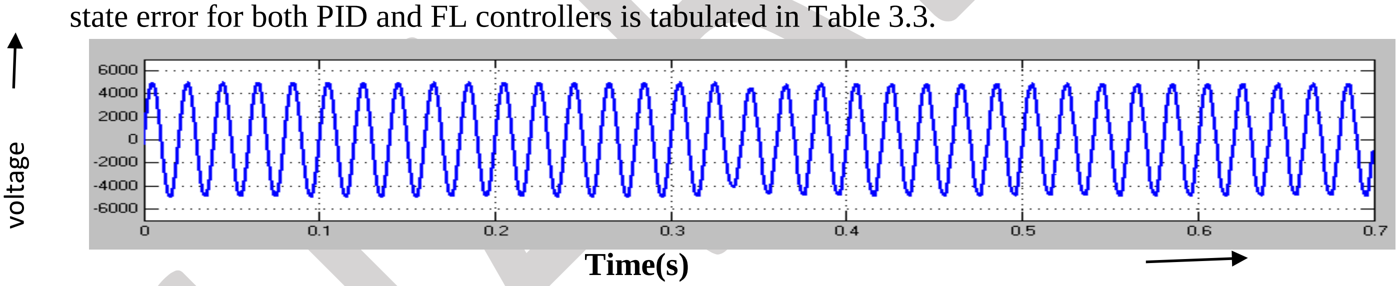


Fig 4.2 Output voltage

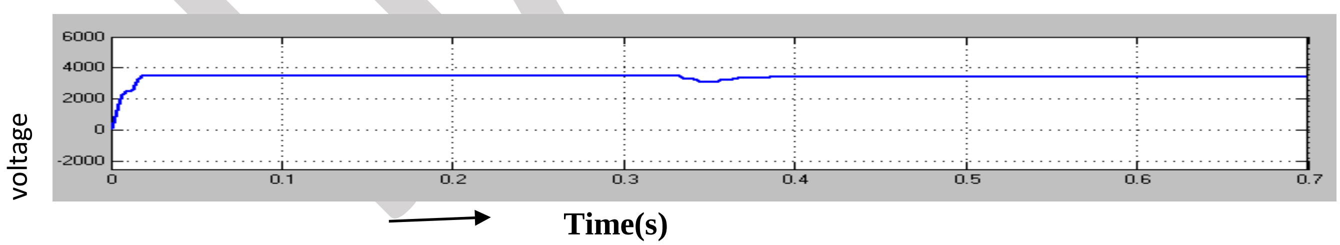


Fig 4.3 RMS output voltage

CONCLUSION

Controllers	Rise time (s)	Peak time (s)	Settling time (s)	Steady state error (V)
PID controller	**0.32**	**0.35**	**0.45**	**9.3**
FLC	**0.31**	**0.33**	**0.36**	**0.09**

The ten-bus systems with PID and FL controllers for DPFC are modeled and simulated using Simulink. The simulation results indicate that the time domain response with FLcontroller is superior to the PID controlled system. The settling time is as low as 0.36 Seconds. The steady state error is 0.09V. The advantage of the proposed system is reduced settling time and steady-state error. The comparison of PID and FL controllers is done.

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