REGULATION 2015

M.TECH VLSI

CURRICULUM AND SYLLABUS

SEMESTER-I					
Code	**Subject Name**	**L**	**T**	**P**	**C**
Theory					
MMA105	Applied Mathematics for Electronics Engineers	3	1	0	4
MVL101	Solid state device modeling and simulations	3	0	0	3
MAE102	Advanced Digital System Design	3	1	0	4
MVL102	Introduction to VLSI Design	3	0	0	3
MAE1E1	Elective-I	3	1	0	4
Practical					
MVL1L1	VLSI Design lab – I	0	0	4	2
				Total Credits:	**20**
SEMESTER-II					
Code	**Subject Name**	**L**	**T**	**P**	**C**
Theory					
MAE201	Analysis and Design of Analog Integrated circuits	3	0	0	3
MVL201	Computer Aided design of VLSI Circuits	3	1	0	4
MVL202	Low Power VLSI	3	0	0	3
MAE2E2	Elective-II	3	1	0	4
MAE2E3	Elective-III	3	1	0	4
Practical					
MVL2L2	VLSI Design Lab – ll	0	0	4	2
				Total Credits:	**20**

SEMESTER-III					
Code	**Subject Name**	**L**	**T**	**P**	**C**
Theory					
MVL3E4	Elective-IV	3	1	0	4
MVL3E5	Elective-V	3	1	0	4
MVL3E6	Elective-VI	3	1	0	4
MVL3P1	Project work phase-I	0	0	12	6
				Total Credits:	**18**

SEMESTER-IV					
Code	**Subject Name**	**L**	**T**	**P**	**C**
MVL4P2	Project work phase-II	0	0	24	12
				Total Credits:	**12**

TOTAL CREDITS FOR THE PROGRAMME-70

Code	LIST OF ELECTIVES	L	T	P	C
MVL001	CMOS VLSI Design	3	1	0	4
MVL002	VLSI Signal Processing	3	1	0	4
MVL003	Analog VLSI Design	3	1	0	4
MVL004	System On Chip Design	3	1	0	4
MVL005	Design of Semiconductor Memories	3	1	0	4
MVL006	VLSI Architecture and Design Methodologies	3	1	0	4
MVL007	SubMicron VLSI Design	3	1	0	4
MVL008	Testing Of VLSI Circuits	3	1	0	4
MVL009	Nanoscale Devices And Circuit Design	3	1	0	4
MVL010	Optimization Techniques In VLSI Design	3	1	0	4
MVL011	VLSI for Wireless Communication	3	1	0	4

MVL012	Computer Architecture and Parallel Processing	3	1	0	4
MVL013	Electromagnetic Interference and Compatibility in System Design	3	1	0	4
MVL014	Advanced Digital Signal Processing	3	1	0	4
MVL015	Real Time Operating System	3	1	0	4
MVL016	Embedded Systems	3	1	0	4
MVL017	ASIC Design	3	1	0	4
	Research Methodology	3	0	0	3

MMA105 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

OBJECTIVES: 3 1 0 4

- To apply all taught techniques to unseen problems,
- Queuing is a major branch of optimization, Random variable compute and interprets means.
- Correlation/covariance, PERT and CPM chart is mainly used for documenting the data(visually) on projects.

COURSE OUTCOMES:

After successful completion of this course, the students should be able to

CO1: The Student will learn to analyze and solve the fundamental problems with prescribed conditions in simple cases.

CO2: The Student will learn to understand how signals, systems, inference combine in prototypical tasks of communication, control and signal processing.

CO3: The Student will learn to manipulate matrices and to do Matrix algebra, determinants, Eigen values Eigen vectors and to solve the system of linear equations.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	P11	P12
CO1	S		M									
CO2		M		W	S	W						
CO3			S		M							
CO4	M			M								
CO5	S		M									

Course Assessment methods:

	Direct		Indirect
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I: ONE DIMENSIONAL RANDOM VARIABLES 12

Random variables and their functions - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Exponential, Gamma, Weibull and Normal distributions.

UNIT-II : MATRIX THEORY **12**

Eigen values using QR Transformations generalized eigenvectors – Canonical forms, singular valued composition and application – matrix norms and induced norms Psuedo inverse – least square approximations.

UNIT-III : SPECIAL FUNCTIO

NS **12**

Bessel's Equation- Bessel Functions- Legendre's Equation- Legendre Polynomials- Rodrigue's Formula- Recurrence Relations- Generating Functions and Orthogonal Property for Bessel Function of the First Kind.

UNIT- IV : OPERATIONS RESEARCH **12**

Network Definitions – Minimal Spanning Tree algorithm – Shortest Route Problem – Maximal Flow model – Minimum Cost Capacitated Flow Problem – CPM and PERT**.**

UNIT-V : QUEUEING THEORY **12**

Single and Multiple Server Markovain Queuing Models – Customer Impatience Priority Queues M/g / I Queuing System –Queuing Applications

Total Periods: 60Hrs

References:

1. Freund J.D. and Miller JR "Probability Statistics for Engineers" Prentice Hall of India, 5th Edition, New Delhi. 1994.
2. Gupta.SC and Kapoor V.K. "Fundamentals of Mathematics Statistics" Sultan Chand & Sons, New Delhi.
3. Steart G.W. "Introduction to Matrix Computaions" Academic Press, New York.
4. Handy A.Taha., "Operations Research An Introduction", 7th Edn. Pearson Education , Chennai-113. 2002.
5. Donald Gross and Carl M. Harris, "Fundamentals of Queuing Theory", 2nd Edn WileyIndia Pvt Ltd, New Delhi.

MVL101 SOLID STATE DEVICE MODELING AND SIMULATIONS 3 0 0 3

Objectives:

- To learn the modeling of bipolar devices.
- To understand about the modeling of MOSFET.
- To learn about the circuit simulators.
- Understanding of the physics of solid state devices.
- Device fabrication and characterization techniques

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Understand the complicated device models that are widely used in VLSI CAD Tools

CO2: Understand the changes introduced in the device models as well as contribute to the development of appropriate device models.

CO3: Understand the parameter measurement Long and Short Channel Parameters..

CO4: Understand the Statistical Modeling of Bipolar and MOS Transistor

CO5: Understand the Modeling of device mismatch for Analog/RF applications

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I BASIC SEMICONDUCTOR PHYSICS **09**

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation Bandgap, Mobility and Resistivity, Carrier Generation and Recombination Avalanche Process, Noise Sources.

UNIT-II MODELING BIPOLAR DEVICE PHENOMENA **09**

Injection and Transport Model, Continuity Equation, Diode Small Signal and Large Signal (Charge Control Model), Transistor Models: Ebber – Molls and Gummel Poon Model, Mextram Model, Spice Modeling Temperature and Area Effects.

UNIT-III MOSFET MODELING **09**

Introduction Inversion Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

UNIT-IV PARAMETER MEASUREMENT **09**

General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Bipolar and MOS Transistor.

UNIT-V OTHER MOSFET MODELS **09**

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling,

Noise model, temperature effects, MOS model 9, MOSAI model, PSP model, Influence of process variation, Modeling of device mismatch for Analog/RF Applications.

Total Periods :45Hrs

Text Books:

1. PhilipE.Allen,DouglasR.Hoberg."CMOSAnalogCircuitDesign" Second Edition, Oxford Press-2002 (Unit III)
2. CMOS/BICMOS CLSI Low Voltage Power Kiat Seng Yeo,Samir S Rofail,Wang-Ling Gob,Person Education low price edition– 2002(Unit IV)

References:

1. S.M.Sze "Semiconductor Devices – Physics and Technology". John Wiley and Sons 1985
2. Giuseppe Massobrio and Paolo Antogentti, "Semiconductor Device Modeling with SPICE
   "Second Edition, McGraw-Hill Inc, New York. 1993 (Unit I, Unit II and Unit III).
3. Mohammed Ismail & Tern Fiez "Analog VLSI – Signal & Information Processing",(Statistical Modeling of Mosfet unit IV).

MAE102 ADVANCED DIGITAL SYSTEM DESIGN 3 1 0 4

Objectives:

- To learn the concepts of theorems and other techniques to design minimized logic functions.
- To Understand the concepts of synchronous and asynchronous sequential circuit design
- To learn about the faults in logic circuits and methods of diagnosing it.
- To learn about programmable logic devices.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: The candidate should after this course have an in-depth knowledge of digital integrated circuit hardware design.

CO2: The emphasis is on FPGA technology, but most of the design techniques can also be applied to ASIC devices.

CO3: The student should be familiar with the latest state-of-the-art system on chip(SoC) design methodologies, including high-level synthesis and partial run-time reconfiguration.

CO4: Students should be able to learn the benefits and drawbacks of the various design methods for solving a problem.

CO5: Through practical assignments, experience will be achieved from both using tools as well as designing their own system.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	

CO2	S	S	S		S			S	M		S	
CO3	S	S	S		S			S	M		S	
CO4	S	S	S		S			S	M		S	
CO5	S	S	S		S			S	M		S	

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I ADVANCED TOPICS IN BOOLEAN ALGEBRA 12

Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT/INCLUSION/AOI/Driver /Buffer gates ,Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method ,Design of static hazard free and dynamic hazard free logic circuits.

UNIT II STNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 12

Analysis of clocked synchronous sequential Networks (CSSN), Modeling of CSSN,State table assignment and reduction, Design of CSSN,Design of iterative circuit, ASM Chart, ASM Realization. Design of Arithmetic circuits for Fast adder,Array Multiplier.

UNIT III ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 12

Analysis of Asynchronous Sequential Circuit (ASC) ,Flow Table Reduction , Races in ASC , State Assignment Problem and the Transition Table, Design of ASC ,Data Synchronizers, Designing vending Machine Controller, Mixed Operating Mode Asynchronous Circuits.

UNIT IV FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 12

Fault Table Method ,Path Sensitization Method, Boolean Difference Method,Kohavi Algorithm, Tolerance Techniques , The Compact Algorithm,Practical PLA‟s, Fault in PLA Circuit Test Approach, Transition Check Approach , State identification and fault detection experiment .

UNIT-VPROGRAMMMABLE LOGIC DEVICES 12

Basic concepts, Programming technologies, Programmable Logic element(PLE), Programmable Logic Array(PLA),System Design using PLD's-Design of combinational and sequential circuits using PLD's(CPLD).Programming PAL device using PALSAM ,Design of state machine using Algorithmic State Machines (ASM) chart as a design tool, Introduction to Field Programmable Gate Arrays –Types of FPGA, Xilinx XC 3000 series, Logic Cell Array (LCA),Configurable Logic Blocks(CLB) INPUT/OUTPUT Block(IPB)-Programmable Interconnect Point (PIP),Introduction to Actel AACT2 FAMILY AND XILINX XC 4000 families ,Design examples.

Total Periods: 60Hrs

References:

1. William I.Flectcher, “An Engineering Approach to Digital Design”, PrenticeHall of India.
2. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
3. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
4. Digital Circuits and Logic Design – Samuel C. Lee , PHI
5. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill 2002.
6. Parag K Lala, “Digital System design using PLD”, BS Publications, 2003.
7. John M Yarbrough, “Digital Logic applications and Design”, Thomson Learning, 2001.
8. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
9. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning, 2004.

MVL102 INTRODUCTION TO VLSI DESIGN 3 0 0 3

Objectives:

- To understand the concepts of MOS transistors operations and their AC , DC characteristics.
- To know the fabrication process of CMOS technology and its layout design rules.
- To know the concepts of power estimation and delay calculations in CMOS circuits.
- To learn about the VLSI circuit components and physical design.
- To study the concepts of Verilog in designing digital logic circuits.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Design layout and schematic and analysis digital logic gates

CO2: Simulate different logic gates using industry standard software CAD tools Cadence

CO3: Explain the purpose and applications of CMOS technology

CO4: Familiar with Digital Integrated Circuits and System Building Blocks

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	P11	P12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5												

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		

6	End Semester Examinations		

UNIT – I MOS TECHNOLOGY AND CIRCUITS **09**

MOS Technology and VLSI, Process parameters and consideration for BJT, MOS and CMOS, CMOS logic, MOS transistor theory , Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage, Body effect,Design equations, Second order effects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model.

UNIT –II CMOS CIRCUITS DESIGN PROCESS **09**

CMOS fabrication, P -Well process, N -Well process, twin - tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERIZATIONAND PERFORMANCE ESTIMATION **09**

Resistance estimation, Capacitance estimation, Inductance, switching characteristics,transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT – IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN **09**

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits,Ripple carry adders,Carry look ahead adders,High-speed adders, Multipliers. Physical design – Delay modelling ,cross talk, floor planning, power distribution. Clock distribution.

UNIT V SPECIFICATION USING VERILOG HDL **09**

Basic concepts- identifiers- gate primitives, gate delays, operators, timing controls, procedural assignments conditional statements, Data flow and RTL, structural gate level switch level modeling, Design hierarchies, Behavioral and RTL modeling, Test benches, Design of decoder, equality detector, comparator, priority encoder, half adder, full adder, Ripple carry adder, D latch and D flip flop

Total Periods: 45Hrs

References:

1. Douglas A. Pucknell and Kamran Eshraghian, “Basic VLSI Design Systems and Circuits”, Prentice Hall of India Pvt. Ltd., 1995.
2. Wayne Wolf, ”Modern VLSI Design”, 2nd Edition, Prentice Hall 2002.
3. Amar Mukherjee, “Introduction to NMOS and CMOS VLSI System Design,” Prentice Hall,
4. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
5. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc.,2002..
6. Fabricious E. “Introduction to VLSI Design”, McGraw Hill, 1990
7. J.Bhasker:Verilog HDL primer, BS publication,2001

MVL1L1 **VLSI DESIGN LAB-1** **0 0 4 2**

LIST OF EXPERIMENTS

Objectives:

- To learn about the design of digital circuits using Hardware description languages
- To learn about the design of FPGA based design methodology.
- To study about the design of simulation of analog building blocks.
- To understand about digital CAD design flow.
- To know about SPICE simulation.

Course Outcomes:

CO1: Design and test digital logic circuits on FPGA.

CO2: Design Electronic circuits using SPICE and PCB layout using EDA tools

CO3: To design and Test of multiplexers and coders

CO4: To design and Test of flipflops

CO5: To design and Test of counters and registers

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	P11	P12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

	Direct		Indirect
1	Observation Book	1	Students Exit Survey
2	Record Book	2	Faculty Survey
3	Model Examination	3	Industry
4	End Semester Examinations	4	Alumni

(ALL SHOULD BE DONE USING VERILOG HDL & VHDL CODE ON FPGA)

1. Design and Testing of Half Adder, Full Adder.
2. Design and Testing of Half Subtractor/Full Subtractor.
3. Design and Testing of Multiplexer, Demultiplexer.
4. Design and Testing of Encoder, Decoder.
5. Design and Testing of Magnitude Comparator With 8 Bits.
6. Design and Testing of Code Converters.
7. Design and Testing of Jk, D, T, SR Flipflops.
8. Design and Testing of Counters.
9. Design and Testing of Up/Down Counters, Ram & Rom.
10. Design and Testing of N- Bit Shift Registers .

11. Design and Testing of ALU .

MAE201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS 3 0 0 3

Objectives:

- To Design the single stage amplifiers using PMOS and NMOS driver circuits with different loads.
- To Analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
- To Study the different types of current mirrors and to know the concepts of voltage and current reference circuits.
- To Understand about MOS switched capacitor filters.
- Apply the methods learned in the class to design and implement practical projects.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Students understand the actual steps involved in the fabrication of a CMOS integrated circuit.

CO2: Students understand the functional characteristics of basic digital integrated circuits and different logic families including the static and dynamic logic.

CO3: Students can design and simulate various functional blocks utilized in CMOS digital integrated circuits. Such blocks include: combinational and sequential logic blocks (both static and dynamic styles); and differential pairs.

CO4: Students understand how to perform physical layout of basic functional circuit blocks that have been designed.

CO5: To know about the MOS Switched Capacitor Filters

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

	Direct		**Indirect**
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I CIRCUIT CONFIGURATION FOR LINEAR IC **09**

Current source, analysis of difference amplifiers with active load, Supply and temperature Independent biasing techniques, voltage references.

UNIT-II OPERATIONAL AMPLIFIERS **09**

Analysis of operational amplifier circuits, slew rate model and high frequency analysis, operational amplifier noise analysis and low noise operational amplifiers.

UNIT-III ANALOG MULTIPLIER AND PLL **09**

Analysis of MOS operational Amplifier, CMOS voltage references, MOS Power amplifier and analog switches.

UNIT-IV MOS ANALOG IC **09**

Design of MOS Operational Amplifier, CMOS Voltage references, MOS power amplifier and analog switches.

UNIT-V MOS SWITCHED CAPACITOR FILTER **09**

Design techniques for switched capacitor filter, CMOS switched capacitor filters, MOS integrated active RC filters. Design techniques for switched capacitor filter, CMOS switched capacitor filters, MOS integrated active RC filters.

Total Periods:45Hrs

References:

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009
2. Gray, Wooley, Broderson, "Analog MOS Integrated Circuits", IEEE Press 1989
3. Kenneth R.Laker, Willy M.C.Sansen, William M.C.Sansen, "Design of Analog Integrated Circuits and Systems ", McGraw Hill, 14.
4. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill,2001
5. Willey M.C. Sansen, "Analog design essentials", Springer, 2006.
6. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley &sons,Inc., 2003.
7. Phillip E.Allen, DouglasR.Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2002

MVL201 COMPUTER AIDED DESIGN OF VLSI CIRCUITS **3 1 0 4**

Objectives:

- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques.
- To use the simulation techniques at various levels in VLSI design flow,
- To understand the concepts of various algorithms used for floor planning placement and routing techniques.
- To describe the basic algorithms used for modeling, design synthesis, simulation and analysis of ICs.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Understand about algorithms and graph theory for the development of

VLSI tools

CO2: Know the limitations and advantages of CAD tools by means of which they can be operated successfully**.**

CO3: Understand about methods for combinational optimization

CO4: Understand about the logical synthesis and simulation

CO5: Understand about scheduling algorithm , Assignment problem &High level transformation

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	P11	P12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		**Indirect**	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT – I INTRODUCTION TO VLSI METHODOLOGIES 12

Introduction to VLSI Methodologies – VLSI Physical Design Automation – Design and Fabrication of VLSI Devices – Fabrication Process and its impact on Physical Design.

UNIT – II VLSI DESIGN AUTOMATION TOOLS 12

A Quick Tour of VLSI Design Automation Tools – Data Structures and Basic Algorithms – Algorithms Graph Theory and Computational Complexity – Tractable and Intractable Problems.

UNIT – III OPTIMIZATION AND PARTITIONING 12

General purpose methods for combinational optimization – partitioning – Floor Planning and Pin Assignment – Placement – Routing.

UNIT – IV MODELING AND SIMULATION 12

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT – V SCHEDULING ALGORITHMS 12

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

Total Periods: 60Hrs

References:

1. N.A Sherwani, "Algorithms for VLSI Physical Design Automation", 1999.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", 1998.

MVL202 LOW POWER VLSI DESIGN 3 0 0 3

Objectives:

- To know the sources of power consumption in CMOS circuits
- To understand the various power reduction techniques and the power estimation methods.
- To study the design concepts of low power circuits**.**
- To study the concepts on different levels of power estimation.
- To study the concepts on different levels of optimization techniques.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Know the basics and advanced techniques in low power design as reduction of power is much needed to enhance the performance of the system

CO2: Understand about the Circuit &Logic Techniques

CO3: Know the basics and advanced techniques in Low Power CMOS VLSI Design .

CO4: Understand about the Synthesis for Low Power Design and Test of Low Voltages

CO5: Understand about the Low Energy

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT – I INTRODUCTION **09**

Introduction – Simulation – Power Analysis – Probabilistic Power Analysis.

UNIT – II CIRCUIT LEVEL & LOGIC LEVEL DESIGN TECHNIQUES **09**

Circuit – Logic – Special Techniques – Architecture and Systems.

UNIT – III LOW POWER DESIGN ANALYSIS **09**

Advanced Techniques – Low Power CMOS VLSI Design – Physical of Power Dissipation in CMOS FET Devices.

UNIT – IV POWER ESTIMATION **09**

Power Estimation – Synthesis for Low Power – Design and Test of Low Voltages – CMOS Circuits.

UNIT – V SPECIAL LOW POWER DESIGN TECHNIQUES **09**

Low Power Static RAM Architectures – Low Energy Computing Using Energy Recovery Techniques – Software Design for Low Power.

Total Periods:45Hrs

Text Books:

1. Gary Yeap "Practical Low Power Digital VLSI Design", 1997.
2. Kaushik'Roy, Sharat Prasad, "Low Power VLSI Circuit Design" 2000.

MVL2L2 VLSI DESIGN LAB II 0 0 4 2

LIST OF EXPERIMENTS

Objectives:

- To understand about layout ,placement and routing in VLSI design
- To understand about SPICE simulation of basic analog citcuits.
- The focus of this course the CAD based VLSI design flow.
- Exposure to various stages of a typical 'state of the art' CAD VLSI tool be provided by various experiments.
- Important module in the CAD tool including the synthesis, place and route,layout, LVS, simulation, and power and clock routing modules

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: An ability to design CMOS logic circuits

CO2: Simulate circuits within a CAD tool and compare to design specifications.

CO3: Design, implement, and simulate circuits using VHDL

CO4: Learn by using Xilinx Foundation tools and Hardware Description Language (VHDL).

CO5: Analyze the results of logic and timing simulations and to use these simulation results to debug digital systems

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	P11	P12
CO1	S	S	S		S			S	M		S	S

CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		Indirect	
1	Lab Records	1	Students Exit Survey
2	Observation books	2	Faculty Survey
3	Model Exam	3	Industry
4	End Semester Examinations	4	Alumni

1. Introduction to layout design rules
   Layout, physical verification, placement & route and static timing analysis for the following:
2. CMOS inverter
3. CMOS NOR/ NAND gates
4. CMOS XOR and MUX gates
5. CMOS half adder and full adder
6. Static / Dynamic logic circuits (register cell)
7. Latch
8. Pass transistor
9. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
10. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
11. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
12. Analog Circuit simulation (AC analysis) – CS & CD amplifier
13. System level design using PLL

ELECTIVES

MVL001 CMOS VLSI DESIGN 3 1 0 4

Objectives:

To understand about the basic concepts of CMOS logic.
To learn about the performance estimation of CMOS logic.
To understand about the design strategies and CMOS subsystem design.
To focus will on the transistor level design.
To address all important issues related to size, speed and power consumption

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand about the basics of CMOS technology and its performance Estimation.

CO2: To learn about the design strategies used in CMOS subsystem**.**

CO3: To understand about the basics of CMOS Circuit and Logic Design

CO4: To learn about the Systems Design and Design Method

CO5: To understand about the basics of CMOS Sub System Design

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		**Indirect**	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I INTRODUCTION TO CMOS CIRCUITS 12

MOS Transistors, MOS Transistors switches, CMCS logic circuit and System representations, MOS Transistor theory – Introduction MOS device design equation, the complementary CMOs inverter – DC characteristics, Static Load MOS inverters, The differential inverter, The transmission gate, The Tri state inverter, Bipolar Devices.

UNIT-IICIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 12

Introduction, Resistance estimation, Capacitance estimation, Inductance estimation, Switching characteristics of CMOS gate Transistor, Sizing, Power Dissipation, Sizing Routing conductors, Charge sharing, Design Margining, Reliability.

UNIT-IIICMOS CIRCUIT AND LOGIC DESIGN 12

CMOs Logic Gate design, Basic Physical Design of simple gate, CMOS Logic structures clocking strategies, i/o Structures, Low Power Design.

UNIT-IVSYSTEMS DESIGN AND DESIGN METHOD 12

Design Strategies CMOS chip Design options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, and Data Sheets. CMOS Testing – Manufacturing Test Principles, Design Strategies for Test, Chip level Test Techniques, System Level Test Techniques, and Layout Design for Improved Testability.

UNIT-VCMOS SUB SYSTEM DESIGN 12

Data path operations – Addition/Subtraction party generators, Comparators. Zero/one Detectors, Binary Counters, ALU's, Multiplication shifters, Memory Elements, Control-FSM, Control Logic Implementation.

Total Periods: 60 Hrs

References:

1. Nell H E Weste and Kamran Eshraghian, "Principles Of CMOS VLSI Design", 2nd Edition, Addision Westley, 1998.
2. Jaycob Backer, Harry W L and David E Byce, "CMOS Circuit Design, Layout and Simulation", PHI, 1998.

MVL 002 VLSI SIGNAL PROCESSING 3 1 0 4

Course Objectives:

- To understand the various VLSI architectures for digital signal processing.
- To know the techniques of critical path and algorithmic strength reduction in the filter structures.
- To study the performance parameters, viz. area, speed and power.
- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Modify the existing or new DSP architectures suitable for VLSI

CO2: Know the basics of Retiming, Algorithmic Strength Reduction

CO3: Understand about the basics of Fast Convolution, Pipelining and Parallel Processing Of IIR Filters

CO4: Know the basics of Bit-Level Arithmetic Architectures

CO5: Understand about the basics of Numerical Strength Reduction, Synchronous, Wave and Asynchronous Pipelining

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni

5	Online test		
6	End Semester Examinations		

UNIT-1INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSINGOF FIR FILTERS 12

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT-II RETIMING, ALGORITHMIC STRENGTH REDUCTION 12

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT- III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 12

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT-IV BIT LEVEL ARITHMETIC ARCHITECTURES 12

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT-V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 12

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

Total Periods :60Hrs

Text Books:

1. Keshab K. Parthi, "VLSI Digital Signal Processing Systems", Design and implementation, Wiley, Inter Science, 1999.
2. S.Y. Kung, H.J. White House, T.Kailath, "VLSI and ModernSignal Processing", Prentice Hall, 1985.
3. Jose E. France, Yannis Tsividis, "Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994

MVL003 ANALOG VLSI DESIGN 3 1 0 4

Objectives:

- To study the concepts of CMOS and BICMOS analog circuits.
- To understand the concepts of A/D convertors and analog integrated sensors.

- To understand the testing concepts in analog VLSI circuits and its statistical modeling.
- To learn about Device Modeling- Various types of analog systems
- To study about CMOS amplifiers and Comparators.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Understand that analog circuits are essential in interfacing and building amplifiers and low pass filters.

CO2: Learn About Basic BICMOS Circuit Techniques, Current-Mode Signal Messing and Neural Information Processing

CO3: Learn About Sampled-Data Analog Filters, Over Sampled A/D Converters and analog Integrated Sensors

CO4: Learn About Design For Testability And Analog VLSI Interconnectors

CO5: Learn About Statistical Modeling And Simulation, Analog Computer-Aided Design and Analog And Mixed Analog-Digital Layout

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		**Indirect**	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW VOLTAGE SIGNAL PROCESSING 12

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques –Super MOS Transistor-Primitive Analog Cells-Linear Voltage-Current converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT-II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT-MODE SIGNAL MESSING AND NEURAL INFORMATION PROCESSING 12

Continuous-Time Signal Processing-Sampled-Data Signal Processing-artiched-current Data Converters-Practical Consideration in SI Circuits Logically-Inspired Neural Networks-Floating-Gate,Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-contrast Sensitive Silicon Retina

UNIT-III SAMPALED-DATA ANALOG FILTERS,OVER SAMPLED A/D CONVERTERS AND ANALOG INTERGRATED SENSORS 12

First-order and second SC Circuits-Bilinear transformation-Cascade Design-Switched-Capacitor Ladder-Synthesis of Switched –Current filter-Nyquist rate A/D converters-Modulators for over Sampled A/D conversion- First and second Order and Multibit Sigma-Delta Modulators-interpolative Modulators-Cascade Architecture-Decimation Filters-Mechanical, Thermal, Humidity and Magnetic Sensors-Sensor interfaces.

UNIT-IVDESIGN FOR TESTABLITY AND ANALOG VLSI INTERCONECTORS 12

Faults modeling and Simulation- Testability-Analysis Technique-AdHoc Methods and General Guidelines Scan Techniques-Boundary Scan-Built-in self Test- Analog Test Buses-Design for Election-Beam Testability-Physics of Interconnects in VLSI- Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping analog Circuits.

UNIT-VSTATISTICAL MODELLING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT 12

Review of statistical concepts- statistical Device Modeling-Statistical Circuit Simulation-Automation Analog Circuit Design-Automatic Analog Layout-CMOS Transistor layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog-Digital Layout.

Total Periods: 60 Hrs

Text Books:

1.”Analog VLSI Signal and information Processing”, Mohammed Ismail, Terri Fiez, McGraw-Hill International Editions,1994.

References:

1. Malcom R. Haskard, Lan C. May, “Analog VLSI Design- NMOS and CMOS”, Prentice hall,1998.
2. Randall I. Geiger, Phillip & Allen, Neol K. Strader, “VLSI Design Techiniques for Analog and Digital Circuits”, McGraw Hill International Company,1990
3. Jose E. France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing,” Prentice Hall, 1994

MVL004 SYSTEM ON CHIP DESIGN 3 1 0 4

Objectives:

- To learn System on chip fundamentals, their applications.
- To gain knowledge on NOC design
- To learn the various Computation models of SOCs.
- Optimize the performance and power of electronics systems on chip
- Arithmetic data path design

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Understand about design of soc in various factors
CO2: Understand about soc models in computation and co design
CO3: Understand about communication and networking of soc
CO4: Understand about various low power NOC design
CO5: Understand about IP cores and application specific design

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		**Indirect**	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I INTRODUCTION **12**

Introduction to SoC Design., Platform-Based SoC Design., Multiprocessor SoC and Network on Chip, Low-Power SoC Design

UNIT-II SYSTEM DESIGN WITH MODEL OF COMPUTATION AND CO-DESIGN **12**

System Models, Validation and Verification, Hardware/Software Codesign Application Analysis, Synthesis.

UNIT-III COMPUTATION–COMMUNICATION PARTITIONING AND NETWORK ON CHIP-BASED SOC **12**

Communication System: Current Trend, Separation of Communication and Computation. Communication-Centric SoC Design, Communication Synthesis, Network-Based Design, Network on Chip, Architecture of NoC

UNIT-IV NOC DESIGN **12**

Practical Design of NoC, NoC Topology-Analysis Methodology, Energy Exploration, NoC Protocol Design, Low-Power Design for NoC: Low-Power Signaling, On-Chip Serialization, Low-Power Clocking, Low-Power Channel Coding, Low-Power Switch, Low-Power Network on Chip Protocol

UNIT-V NOC /SOC CASE STUDIES **12**

Real Chip Implementation-BONE Series-,BONE 1-4, Industrial Implementations-,Intel's Tera-FLOP 80-Core NoC, Intel's Scalable Communication Architecture, Academic Implementations-FAUST, RAW;design case study of SoC –digital camera.

Total Period :60Hrs

References:

1. Hoi-jun yoo, Kangmin Lee, Jun Kyoung kim, *"Low power NoC for high performance SoC desing"*,CRC press, 2008.

2. Vijay K. Madisetti Chonlameth Arpikanondt, *"A Platform-CentricApproach to System-on-Chip (SOC) Design"*, Springer, 2005.

MVL005 DESIGN OF SEMICONDUCTOR MEMORIES 3 1 0 4

Objectives:

- To study the architectures for SRAM and DRAM
- To know about various non-volatile memories.
- To study the fault modeling and testing of memories for fault detection.
- To learn the radiation hardening process and issues for memory.
- To know about Ferroelectric Random Access Memories (FRAMs).

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Design Memory Structures.

CO2: Decide the type of memory for a specific application.

CO3: Describe the smartness in the circuits used for memories.

CO4: Design the architectures of Static and Random Access, Nonvolatile memories.

CO5: Evaluate the fault modeling and testing procedures for memory circuit.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		

6	End Semester Examinations		

UNIT-I RANDOM ACESS MEMORY TECHNOLOGY 12

Static Random Access Memories(SRAM) SRAM Cell Structure-MOS SRAM Architecture-MOS SRAM Cell and Peripherals Circuit Operation – Bipolar SRAM Technologies –Silicon On Insulator (Sol) Technology – Advanced SRAM Architecture and Technologies – Application Specific SRAMs Dynamic Random Access Memoirs(DRAMs) DRAM Technology Development – CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures-BICMOS DRAMs – Soft Error Failure in DRAMs – Advanced DRAM Designs and Architecture – Application Specific DRAMs.

UNIT-II NON VOLATILE MEMORIES 12

Mask Read Only Memories(ROMs)-High Density ROMs-Programmable Read Only Memories(PROMs)-Bipolar PROMs CMOS PROMs-Erasable (UV) – Programmable Read Only Memories(EPROMs) - Floating – Gate EPROM Cell-One Time Programmable (OTP) EPROMs -Electrically Erasable PROMs(EEPROMs) – EEPROM Technology and Architecture – Non Volatile SRAM – Flash Memories (EPROM or EEPROM)

UNIT-III MEMORY FAULTS MODELLING, TESTING AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE 12

RAM Fault, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault modeling and Testing-Application Specific Memory Testing

UNIT-IVSEMICONDUCTOR MEMORY RELIABILITY AND RANDOM EFFECTS 12

General Reliability Issues-RAM Failure Modes and Mechanism - Nonvolatile Memory Reliability – Reliability Modeling and Failure Rate Prediction – Design for Reliability – Reliability Test Structures – Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP) – Radiation Hardened Memory Characteristics – Radiation Hardness Assurance and Testing – Radiation Dosimettry - Water Level Radiation Testing and Test Structures.

UNIT–VADVANCED MEMORY TECHNOLOGIES AND HIGH DENSITY MEMORY PACKAGING TECHNOLOGICS 12

Ferroelectric Random Access Memories (FRAMs) – Gallium Arsenide (GaAs) FRAM – Analog Memories Magneto Resistive Ferroelectric Random Access Memories (MRAMS) – Experimental Memory Devices Memory Hybrids and MCMs (2D – Memory Stacks and MCMs 3D) – Memory MCM Testing and Reliability Issues – Memory Cards – High Density Memory Packing Feature Directions.

Total periods: 60 Hrs

Text Books:

1. Ashok K. Sharma, “Semiconductor Memories Technology, Testing, and Reliability”, Prentice Hall of India Limited. New Delhi 1997.

MVL006 VLSI ARCHITECTURE AND DESIGN METHODOLOGIES 3 1 0 4

Objectives:

- To give an insight to the students about the significance of CMOS technology and fabrication process.

- To teach the importance and architectural features of programmable logic devices.
- To introduce the ASIC construction and design algorithms
- To teach the basic analog VLSI design techniques.
- To study the Logic synthesis and simulation of digital system with Verilog HDL.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand about the advanced topics in Boolean algebra.

CO2: To know about analog and high speed VLSI.

CO3: To know in detail about programmable ASICs and its interconnects.

CO4: To understand about programmable ASIC its logic synthesis, simulation and testing of VLSI circuits

CO5: To understand about simulation and testing of VLSI circuits

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		**Indirect**	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I INTRODUCTION **12**

Overview of a Digital VLSI design Methodologies- Trends in IC Technology advanced Boolean algebra- Shannon's expansion theorem- consensus theorem – Octal designation-Run Measure – Buffer gates- Gate Expander- Reed Muller expansion- Synthesis of multiple output combinational logic circuits by product map method- Design of Static hazard free and dynamic hazard free logic circuits.

UNIT-II ANALOG VLSI AND HIGH SPEED VLSI **12**

Introduction to analog VLSI- Realisation of Neural Networks and switched capacitors filters-sub- micron Technology and GaAS VLSI technology.

UNIT-III PROGRAMMABLE ASICS **12**

Antifuse- Static RAM-EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA- Altera FLEX- Altera MAX DC & AC inputs and outputs – clocks and power inputs – Xilinx I/O blocks.

UNIT-IV PROGRAMMABLE ASIC DESIGN SOFTWARE 12

Actel ACT – Xilinx LCA- Xilinx EPLD - Altera MAX 5000 & 7000 – Altera Max 9000 – Design Systems – Logic synthesis – half gate ASIC – Schmatic entry – low level design language – PLA tools – EDIF – CFI design representation.

UNIT-V LOGIC SYNTHESIS , SIMULATION AND TESTING 12

Basic features of VHDL language for behavioral modeling and simulation – Summary of VHDL data types – Dataflow and structural modeling – VHDL and logic Synthesis – types of simulation – Boundary scan Test – fault Simulation – Automatic test Pattern Generation.

Total Periods: 60 Hrs

References:

1. Willam I. Fletcher " An Engineering Approach to Digital Design" Prentice Hall of India 1996.
2. Amar Mukherjee, Introduction to NMOS and CMOS VLSI System Design. Prentice Hall of India 1986.
3. M.J.S. Smith " Application – Specific Integrates Circuits ", Addison Wesley Longman Inc. 1997.
4. Fedrick J. Hill and Gerald R. Peterson. " Computer Aider Logical Design with emphasis on VLSI

MVL007 SUBMICRON VLSI DESIGN 3 1 0 4

Objectives:

- To introduce the concepts of Silicon realization of ASIC and cmos devices at deep submicron level.
- To study and apply the deep submicron concepts to cmos low power devices.
- To study and discuss about RF CMOS transistor sizing and its limitations.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Understand the Concepts of silicon realization of ASIC and CMOS devices at deep Submicron Level.

CO2: Apply the deep Submicron concepts to CMOS low power devices

CO3: Discuss about RF CMOS transistor sizing and its limitations.

CO4: Understand about the design constraints for CMOS devices at deep submicron level for low power and high speed

CO5: Understand about the reliability constraints while designing CMOS devices at submicron level.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	P011	P012
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I SILICON REALIZATION OF ASIC 12

Introduction-Handcrafted layout implementation-bit-slice layout implementation-Cell based layout implementation- gate array layout implementation-Hierchial design approach- The choice of layout implementation form

UNIT-II LOW POWER DESIGN 12

Sources of CMOS power consumption-technology options for low power-reduction of P-leak by technological measures Reduction of P-dyn by technology measures-reduction of P-dyn by reduced voltage process-design option for low power-computing power vs chip power-a scaling perspectives.

UNIT-III DESIGN FOR RELIABILITY 12

Introduction-latch up in CMOS circuits-Electrostatics discharge-and its protection-Electro migration-Hot carrier degradation design for signal integrity-clock distribution and critical timing issues-clock generation and synchronization in different domain on a chip-the influence of interconnection-design organization

UNIT-IV DEEP SUB MICRON 12

RF-CMOS Transistor downsizing limitations-. RF basic blocks layout implementation Submicron technology and layout dependent effects-input output interfacing, the bonding pad, the pad ring, electrostatic discharge prevention.

UNIT-VCMOSDEVICES 12

Clamp CMOS devices, zener diode-input structure-output structure-pull up-pull down-i/o pad,power clamp-core/pad limitation I/O Pad description using Ibis-Connecting to the package-Signal propagation between integrated circuits

Total Periods: 60Hrs

References:

1. Deep-Submicron Cmos Ics: From Basics to Asics By Harry J. M. Veendrick
2. Low Power Design in Deep Submicron Electronics by W. Nebel, Jean P. Mermet
3. Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction by P.R.Van Der Meer, Arie van Staveren, Arthur H. M. van Roermund

MAE 008 ASIC DESIGN 3 1 0 4

Objectives:

- To learn the fundamentals of ASIC and its design methods
- To gain knowledge on programmable architectures for ASICs

- To understand the physical design of ASIC.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC.

CO2: Analyse the synthesis, Simulation and testing of systems.

CO3: Describe the different phases of the design flow for digital ASICs.

CO4: Explain how non-functional design constraints affect the design process.

CO5: Categorize different types of ASICs and explain their technology.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I SILICON REALIZATION OF ASIC **12**

Introduction-Handcrafted layout implementation-bit-slice layout implementation-Cell based layout implementation- gate array layout implementation-Hierchial design approach- The choice of layout implementation form

UNIT-II LOW POWER DESIGN **12**

-Sources of CMOS power consumption-technology options for low power-reduction of P-leak by technological measures Reduction of P-dyn by technology measures-reduction of P-dyn by reduced voltage process-design option for low power-computing power vs chip power-a scaling perspectives.

UNIT-III DESIGN FOR RELIABILITY **12**

Introduction-latch up in CMOS circuits-Electrostatics discharge-and its protection-Electro migration-Hot carrier degradation design for signal integrity-clock distribution and critical timing issues-clock generation and synchronization in different domain on a chip-the influence of interconnection-design organization

UNIT-IV DEEP SUB MICRON **12**

RF-CMOS Transistor downsizing limitations-. RF basic blocks layout implementation Submicron technology and layout dependent effects-input output interfacing, the bonding pad, the pad ring, electrostatic discharge prevention.

UNIT-V CMOS DEVICES **12**

Clamp CMOS devices, zener diode-input structure-output structure-pull up-pull down-I/O PAD ,power clamp-core/PAD limitation I/O Pad description using Ibis-Connecting to the package-Signal propagation between integrated circuits

Total Periods: 60Hrs

References:

1. Deep-Submicron Cmos Ics: From Basics to Asics By Harry J. M. Veendrick
2. Low Power Design in Deep Submicron Electronics by W. Nebel, Jean P. Mermet
3. Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction by P.R.Van Der Meer, Arie van Staveren, Arthur H. M. van Roermund

MVL008 TESTING OF VLSI CIRCUITS 3 1 0 4

Objectives:

- To know the various types of faults and also to study about fault detection, dominance
- To know the concepts of the test generation methods-DFT-BIST.
- To understand the fault diagnosis methods
- To study about Testable Memory Design.
- To study about Diagnosis by UUT reduction.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand the various types of models and testing..

CO2: To understand the test generation in sequential and combinational circuits.

CO3: To understand the design for test ability in various design types

CO4: To apply various test algorithms in bist.

CO5: To develop more efficient tools from the fault coverage and speed point of view.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	S	S	S		S			S	M		S	S
CO3	S	S	S		S			S	M		S	S
CO4	S	S	S		S			S	M		S	S
CO5	S	S	S		S			S	M		S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey

3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I TESTING AND FAULT MODELLING **12**

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models– Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation

UNIT-II TEST GENERATION **12**

Test generation for combinational logic circuits – Testable combinational logic circuit design– Test generation for sequential circuits – design of testable sequential circuits.

UNIT-III DESIGN FOR TESTABILITY **12**

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT-IV SELF – TEST AND TEST ALGORITHMS **12**

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT-V FAULT DIAGNOSIS **12**

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

Total Periods: 60Hrs

References:

1. Viswani D. Agarval, Michael L. Bushnell, “Essential of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuit”. Kulwer Academic Publications, 1999.
2. Alfred L. Crounch “Design for Test for Digital IC’s and Embedded Core Systems”. – PHI 1999.
3. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House,2002.
4. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
5. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.

MVL009 NANOSCALE DEVICES AND CIRCUIT DESIGN 3 1 0 4

Objectives:

- To understand the necessary of scaling of MOS transistor.
- To introduce the concepts of nanoscale MOS transistor concepts and their performance characteristics.
- To study the various nano scaled MOS transistors.
- To study about various nanoscale devices.
- To design CMOS circuit using non-classical devices.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To learn about leakage current and its control and reduction techniques in CMOS

devices

CO2: To know the device technologies for sub 100nm CMO device scaling of single and multigate MOSFETs

CO3: To familiarize the low power design and voltage scaling issues in Nano scale devices

CO4: To study about various nanoscale devices CMOS circuit using non-classical devices.

CO5: To undertand about the concepts of nanoscale devices which in turn can be used for high speed VLSI circuits.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1							S					S
CO2		S	S	M	M							
CO3	S					M		M				**S**
CO4		M	S			S						
CO5	S				M							**S**

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I CMOS SCALING CHALLENGES IN NANOSCALE REGIMES 12

Leakage current mechanisms in nanoscale CMOS, leakage control and reduction techniques, process variations in devices and interconnects. Device technologies for sub 100nm CMOS: Silicidation and Cu-low k interconnects, strain silicon – biaxial stain and process induced strain; Metal-high k gate; Emerging CMOS technologies at 32nm scale and beyond – FINFETs, surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs.

UNIT-II DEVICE SCALING AND BALLISTIC MOSFET 12

Two dimensional scaling theory of single and multigate MOSFETs, generalized scale length, quantum confinement and tunneling in MOSFTEs, velocity saturation, carrier back scattering and injection velocity effects, scattering theory of MOSFETs.

UNIT-III EMERGING NANOSCALE DEVICES 12

Si and hetero-structure nanowire MOSFETs, carbon nanotube MOSFETs, quantum wells, quantum wires and quantum dots; Single electron transistors, resonant tunneling devices.

UNIT-IV NANOSCALE CMOS DESIGN 12

CMOS logic power and performance, voltage scaling issues; Introduction to low power design; Performance optimization for data paths.

UNIT-V NANOSCALE CIRCUITS **12**

Statistical circuit design, variability reduction, design for manufacturing and design optimization; Sequential logic circuits, registers, timing and clock distribution, IO circuits and memory design and trends. Non-classical CMOS: CMOS circuit design using non-classical devices – FINFETs, nanowire, carbon nanotubes and tunnel devices.

Total Periods : 60Hrs

References:

1. Lundstrom, M., "Nanoscale Transport: Device Physics, Modeling, and Simulation",Springer. 2000
2. Maiti, C.K., Chattopadhyay, S. and Bera, L.K., "Strained-Si and Hetrostructure Field Effect Devices", Taylor and Francis, 2007
3. Hanson, G.W., "Fundamentals of Nanoelectronics", Pearson, India., 2008.
4. Wong, B.P., Mittal, A., Cao Y. and Starr, G., "Nano-CMOS Circuit and Physical Design", Wiley, 2004
5. Lavagno, L., Scheffer, L. and Martin, G., "EDA for IC Implementation Circuit Design and Process Technology", Taylor and Francis, 2005

MVL010 OPTIMIZATION TECHNIQUES IN VLSI DESIGN 3 1 0 4

Objectives:

- To know in detail about the optimization techniques.
- To gain knowledge on Genetic algorithms
- To learn implementation of genetic algorithms for VLSI physical design problems
- To understand implementation of genetic algorithms for testing of VLSI circuits and technology mapping.
- To know about FPGA technology mapping.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand about different optimization models.

CO2: To know about different statistical performance, power and yield analysis.

CO3: To learn implementation of genetic algorithms in convex optimization.

CO4: To understand implementation of genetic algorithms FPGA

CO5: Optimization methods are necessary for making circuits and making device layouts.

CO/PO Mapping
(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1							S					S
CO2		S	S	M	M							
CO3	S					M	S					S

CO4		M	S			S						
CO5	S				M			S				S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I STATISTICALMODELING 12

Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom‟s model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models

UNIT-II STATISTICAL PERFORMANCE,POWER AND YIELD ANALYSIS 12

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation

UNIT-III CONVEX OPTIMIZATION 12

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT-IVGENETIC ALGORITHM 12

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routing technology,Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding-local improvement-WDFRComparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

UNIT-V GA ROUTING PROCEDURES AND POWER ESTIMATION 12

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

Total Periods : 60Hrs

References:

1. Ashish Srivastava, Dennis Sylvester, David Blaauw “Statistical Analysis and Optimization for VLSI:Timing and Power” , Springer, 2005.
2. Pinaki Mazumder, E.Mrudnick, “Genetic Algorithm for VLSI Design,Layout and test Automation”, Prentice Hall,1998.
3. Stephen Boyd, Lieven Vandenberghe “Convex Optimization”, Cambridge University

MVL011 VLSI FOR WIRELESS COMMUNICATION 3 1 0 4

Objectives:

- To study the design concepts of low noise amplifiers.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of CDMA in wireless communication.
- To know about VLSI architecture for Multitier Wireless System .

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand basic components and devices

CO2: To study the various types of mixers in low power

CO3: To understand concept of frequency synthesizers

CO4: To understand the concepts of sub systems.

CO5: To know the concepts related to wireless communication in VLSI which can be efficiently implemented in real time**.**

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			S	M								S
CO2	S	M	M		S			M				
CO3				S	W		M					S
CO4		S	W		M							S
CO5	M											S

Course Assessment methods:

Direct		**Indirect**	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I COMPONENTS AND DEVICES 12

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers

UNIT-II MIXERS 12

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency

Case – Noise- A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT-III FREQUENCY SYNTHESIZERS 12

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

UNIT-IV SUB SYSTEMS 12

Data converters in communications, adaptive Filters, equalizers and transceivers

UNIT-V IMPLEMENTATIONS 12

VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System .

Total Periods:45Hrs

References:

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall 1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.
4. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", Kluwer Academic Publishers, 2000.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.
6. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 1997.

MVL012 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING 3 1 0 4

Objectives:

- To understand the difference between the pipeline and parallel concepts.
- To study the various types of architectures and the importance of scalable architectures.
- To study the various memories and optimization of memory.
- To know about Parallel and scalable architectures
- To study about environments, UNIX, MACH and OSF/1 for parallel computers.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand the performances and measures for VLSI.

CO2: To understand the various types of architectures.

CO3: To study the various memories and optimization of memory.

CO4: Compare and evaluate the performance of various architectures

CO5: Analyze the requirements of large systems to select and build the right infrastructure.

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M			W	S					S
CO2		M		W	S			M				
CO3			S		M							**S**
CO4	M			M			M					**S**
CO5												

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I THEORY OF PARALLESISM –PART-I **12**

Parallel computer models-the state of computing, Multiprocessor and Multicomputer and Multivectors and SIMD computers, PRAM and VLSI mode Architectural development tracks .Program and properties Conditions of parallelism.

UNIT-II THEORY OF PARALLELISM –PART-II **12**

Program partitioning and scheduling, Program flow mechanism, System inter connect architecture, Principles of scalable performance–performance matrices and measures, Parallel processing application speedup performance laws, scalability analysis and approaches.

UNIT-III HARDWARE TECHNOLOGIES **12**

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory-backplane bus systems, cache memory organizations, shared memory organization, sequential and weal consistency model.

UNIT-IV PIPELINING AND SUPERSCALAR TECHNOLOGIES **12**

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivectors and SSIMD Computers, Scalable Multithread and dataflow architectures.

UNIT-V SOFTWARE AND PARALLEL PROCESSING **12**

Parallel models,Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

Total Periods: 60Hrs

References:

1. Kai Hawang, “Advanced Computer Architecture”, McGraw Hill international, 1993.

2. William Stallings, “Computer Organization and Architecture”, Macmillan Publishing Company, 1990.
3. M.J.Quinn, “Designing Efficient Algorithms for Parallel Computer”, McGraw Hill International1994.

MVL013 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN 3 1 0 4

Objectives:

To know about

- EMI Environment
- EMI Coupling Principles
- EMI Specification, Standards and Limits
- EMI Measurements and Control Techniques
- EMC Design of PCBs

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To know about EMI Environment

CO2: Ability to analyze Electromagnetic interference effects in PCBs

CO3: Ability to propose solutions for minimizing EMI in PCBs

CO4: EMI Specification, Standards and Limits, EMI Measurements and Control Techniques

CO5: Ability to propose solutions for minimizing EMI in PCBs

CO/PO Mapping
(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1							S					S
CO2		S	S	M	M							
CO3	S					M						S
CO4		M	S	W		S						
CO5	S				M							S

Course Assessment methods:

	Direct		**Indirec**
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I EMI ENVIRONMENT/SPECIFICATIONS /STANDARDS 12

Sources of EMI conducted and radiated EMI, Transient EMI, EMI-EMC Definitions and units of parameters, unit of specifications, Civilian standards, and Military standards.

UNIT-II EMI COUPLING PRINCIPLES 12

Conducted, Radiated and Transient Coupling, common impedance ground coupling, radiated common mode and ground loop coupling radiated differential mode coupling, near field, cable to cable coupling, power mains and power supply coupling.

UNIT-II MEASUREMENTS 12

UMI Test instruments/systems,EMI Test ,EMI Shielded Chamber ,Open Area Test Site ,TEM Cell Antennas ,Conductors Sensors /Injectors /Couplers ,Military Test Method AND Procedures ,Calibration procedures.

UNIT-IV EMI CONTROL TECHNIQUES 12

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, signal Control, Component Selection and mounting.

UNIT-VEMC DESIGN OF PCBS 12

PCB Traces Cross Talk, Impedance Control, Power Distribution decoupling, Zoning, Motherboard Designs and propagation Delay performance models.

Total Periods: 60Hrs

Text books:

1. Bernhard Kerser, “Principles of Electromagnetic Compatibility”, Artech house, 3rd Ed 1986.
2. Henry W.Ott, “Noise Reduction Techniques in Electronic Systems”, John Wiley and Sons, New York, 1986.
3. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, 1986.

MVL014 ADVANCED DIGITAL SIGNAL PROCESSING 3 1 0 4

Objectives:

- To learn about random signal processing
- To know about spectrum and linear estimation.
- To know about adaptive filters
- To understand the concepts related to multirate digital signal processing.
- To study about Decimation by an integer factor

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To learn about random signal processing and there algorithms

CO2: To know about spectrum and linear estimation for various methods of spectrum analyser

CO3: To know about adaptive filters linear estimation and their premitives.

CO4: To understand the concepts related to adaptive filters digital signal processing.

CO5: To understand different amplifiers in low signal.

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M			W						S
CO2		M		W	S							S
CO3			S		M							S
CO4	M			M								
CO5												S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I DISCRETE RANDOM SIGNAL PROCESSING 12

Discrete Random Processes,Expectations,Variance,Co-variance,Scalar product, Energy of Discrete Signals-Parseval's Theorem, Wiener Khintchine Relation-Power Spectral Density-Periodogram-Sample Autocorrelation-Sum Decomposition Theorem, Spectral Factorization Theorem-Discrete Random Signal Processing by Linear Systems-Simulation of White Noise-Low Pass filtering of white noise.

UNIT-II SPECTRUM ESTIMATION 12

Non-Parametric Methods–Correlation Method–Co-Variance Estimator-Performance Analysis of Estimator-Barlett Spectrum Estimation –Welch Estimation-Model Based Approach-AR,MA,ARMA Signal Modeling –Parameter Estimation using Yule-Walker Method.

UNIT-III LINEAR ESTIMATION AND PREDICTION 12

Maximum likelihood criterion-efficiency of estimator-least mean squared error criterion-Wiener filter –Discrete Wiener Hoff Equation–Recursive estimators–Kalman filter–linear prediction, prediction error whitening filter, inverse filter-Levinson recursion, Lattice realization and Levinson recursion algorithm for solving Toeplitz system of equations.

UNIT-IVADAPTIVE FILTERS 12

FIR adaptive filters-Newton's steepest descent method-adaptive filter based on steepest descent method-Widrow Hoff LMS adaptive algorithm-Adaptive channel equalization-Adaptive echocarcellor-Adaptive noise cancellation –RLS adaptive filter-Exponentially weighted RLS –Sliding window RLS –Simplified IIRLMS adaptive filter.

UNIT-V MULTIRATE DIGITAL SIGNAL PROCESSING 12

Mathematical description of sample rate-interpolation and Decimation-continuous time model direct digital approach-Decimation by an integer factor–interpolation by an integer factor-Single and multistage realization-poly phase realization-Application to Sub band coding-Wavelet transform and filter bank implementation of wavelet expansion of signals.

Total Periods : 60Hrs

Textbooks:

1. Monson.H.Hayes, Statiscal Digital Processing and Modelling, John Wiley and Sons.INC, New York.1996.

References:

1. Sophocles J.Orfanidis, OptimumSignal Processing, McGraw Hill.1990.
2. John.G.Proakis, Dimitris G.Manofakis.Digital Signal Processing Prentice Hall of India, 1995.

MVL015 REAL TIME OPERATING SYSTEMS 3 1 0 4

Objectives:

- The aim of the course is to impart the concepts related to operating systems concepts and to discuss about RTOS application domains.
- To study about client server model- distributed file systems.
- To learn about synchronization control blocks
- To know about comparison and study of various RTOS like QNX-VX works
- To understand RTOS for image processing

Course Outcomes:

After successful completion of this course, the students should be able

CO1: To understand and review about different operating system
CO2: To understand about networking and distributed operating system
CO3: To understand about real time models and languages
CO4: To understand about real time kernel
CO5: To know about various application domains in RTOS.

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M			W	S				S	S
CO2		M		W	S							S
CO3			S		M						S	
CO4	M			M			M					S
CO5											S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey

3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I REVIEW OF OPERATING SYSTEMS **12**

Basic Principles – System calls – Files – Processes – Design and Implementation of Processes – Communication Between Processes – Operating System Structures.

UNIT-II DISTRIBUTED OPERATING SYTEMS **12**

Topology – Network types – communication – RPC- client server model- distributed file systems- design strategies.

UNIT-III REAL TIME MODELS AND LANGUAGES **12**

Events based – process based and graph based models – petrinet models – real time languages – RTOS tasks – RT scheduling – interrupt processing – synchronization control blocks – memory requirements.

UNIT-IV REAL TIME KERNEL **12**

Principles – design issues – Polled loop systems - RTOS porting to a target – comparison and study of various RTOS like QNX-VX works – PSOS – C executive - Case studies

UNIT-V RTOS APPLICATION DOMAINS **12**

RTOS for image processing - Embedded RTOS for voice over IP – RTOS for voice over IP – RTOS for fault tolerant applications – RTOS for control systems.

Total Periods : 60Hrs

References:

1.Herma K, " Real time systems – Design for distributed Embedded Applications ", Kluwer Academic, 1997.

2.Charles Crowly, "Operating System – A design oriented approach" McGraw Hill, 1997.

3.R.J.A Bhur, D.L. Bailey, "An introduction to Real Time Systems', PHI 1999.

4.C.M. Krishna, Kang G Shin, "Real time systems", McGraw Hill, 1997

MVL016 EMBEDDED SYSTEMS 3 1 0 4

Objectives:

- To have knowledge about the basic functions of embedded systems.
- To know in detail about PIC microcontroller.
- To have knowledge about the basic structure of embedded systems.
- To discuss about the software environment in embedded systems.
- To learn about real time operating systems.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand about the concepts of embedded systems..

CO2: To know in detail about PIC microcontroller and interfacing.

CO3: To understand in detail about embedded microcontroller and architecture.

CO4: To apply software tools in various embedded hardware.

CO5: To apply embedded system for real time applications.

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M			W	S				S	S
CO2		M		W	S							S
CO3			S		M						S	
CO4	M			M			M					S
CO5											S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I INTRODUCTION REVIEW OF EMBEDDED HARDWARE 12

Terminology Gates – Timing Diagram – Memory – Microprocessors Busses – Direct Memory Access – Interrupts – Built – Ins on the Microprocessor – Conventions used on Schematic – Interrupt Microprocessor Architecture – Shared Data Problem – Interrupt Latency.

UNIT-II PIC MICROCONTROLLER AND INTERFACING 12

Introduction – CPU Architecture – Registers – Instruction Sets Addressing Modes – Loop Timers - Interrupts – Interrupt Timing I/O Expansion – 12C Bus Operation Serial EEPROM – Analog to Digital Converter – UART Baud Rate – Data Handling – Initialization – Special Features – Serial Programming – Parallel Slave Port.

UNIT-III EMBEDDED MICROCONTROLLER SYSTEMS 12

Motorola MC68H11 Family Architecture Registers - Addressing Modes – Programs – Interfacing Methods – Parallel I/O Interface – Parallel Port Interface – Memory Interfacing – High Speed I/O Interfacing - Interrupts – Interrupt SERVICE Routing – Features of Interrupts – Interrupt Vector and Priority – Timing Generation and Measurement – Input Capture – Output Compare – Frequency Measurement – Serial I/O Devices RS232, RS485 – Analog Interfacing – Applications.

UNIT-IV SOFTWARE DEVELAPMENT AND TOOLS 12

Embedded System Evolution Trends – Round – Robin with Interrupts – Function –One – Scheduling Architecture – Algorithms – Introduction to Assembler – Compiler – Cross Compilers and Integrated Development Environment (IDE) – Object Oriented Interfacing – Recursion – Debugging Strategies – Simulators.

UNIT-V REAL TIME OPERATING SYSTEMS **12**

Task and Task States – Tasks and Data – Semaphores and Shared Data Operating System Services – Message Queues – Timer Function – Events – Memory Management – Interrupt Routines in an RTOS Environment – Basic Design Using RTOS.

Total Periods: 60Hrs

Text books:

1. David E. Simon, "An embedded Software Primer" Pearson Education Asia, 2001.
2. John B Peat man "Design with Microcontroller" Pearson Education Asia, 1998.
3. Jonathan W. Volcano Brooks/Cole "Embedded Micro Computer Systems. Real Time Interfacing". Thomson Learning 2001.

References:

1. Burns, Alan and Welling, Andy, "Real - Time Systems and Programming Languages", Second Edition, Harlow: Addison – Wesley – Longman, 1997
2. Raymond J. A. Blur and Donald L. Bailey, "Introduction to Real Time Systems: Design to Networking with C/C++" Prentice Hall Inc. New Jersey, 1999
3. Graham Moore, and Cylix, "Real – Time Programming: A Guide to 32 Bit Embedded Development. Reading" Addison - Wesley – Longman, 1998.
4. Heath. Steve, "Embedded Systems Design", Newness 1997.

MVL017 **ASIC DESIGN** **3 1 0 4**

Objectives:

- To learn the fundamentals of ASIC and its design methods
- To gain knowledge on programmable architectures for ASICs
- To understand the physical design of ASIC.
- To study about VHDL and LOGIC Synthesis
- To know about FPGA Partitioning

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To study the design flow of different types of ASIC.

CO2: To familiarize the different types of programming technologies and logic devices.

CO3: To gain knowledge about partitioning, floor planning, placement and routing Including.

CO4: To know about different high performance algorithms and its applications in ASICs.

CO5: To analyse the synthesis, Simulation and testing of systems

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M			W	S				S	S
CO2		M		W	S							S
CO3			S		M						S	

CO4	M			M			M					S
CO5											S	S

Course Assessment methods:

Direct		Indirect	
1	Internal Tests	1	Students Exit Survey
2	Assignments	2	Faculty Survey
3	Seminar	3	Industry
4	Quiz	4	Alumni
5	Online test		
6	End Semester Examinations		

UNIT-I INTRODUCTION TO ASIC, CMOS LOGIC AND ASIC LIBRARY DESIGN 12

Capacitance – Logical Effort – Library Cell Design – Library Architecture Types of ASIC **–** Design Flow – CMOS Transistors – CMOS Design Rules – Combinational Logic Cell – Sequential Logic Cell – Data Path Logic Cell – Transistors as Resistors – Transistor Parasitic**.**

UNIT-II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 12

Anti fuse – Static RAM – EPROM and EEPROM Technology – PREP Bench Marks – Acted ACT – Xilinx LCA – Altars FLEX – Alters MAX – DC & AC Input and Output – Clock and Power Input – Xilinx I/O Blocks.

UNIT-III PROGRAMMABLE ASICS INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 12

Acted ACT - Xilinx LCA - Xilinx EPLD - Alters MAX 5000 & 7000 - Alters MAX 9000 - Alters FLEX – Design System – Logic Synthesis – Half Gate ASIC – Schematic Entry – Low Level Design Language – PLA Tools – EDIF – CFI Design Representation**.**

UNIT-IV LOGIC SYNTHESIS, SIMULATION AND TESTING 12

Verilog and Logic Synthesis– VHDL and LOGIC Synthesis– Types of Simulation – Boundary Scan Test– Fault Simulation- Automatic Test Pattern Generation.

UNIT-V BASICS CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 12

System Partition – FPGA Partitioning – Partitioning Methods – Floor Planning – Placement – Physical Design Flow – Global Routing – Detailed Routing – Special Routing –Circuit Extraction – DRC. **Total Periods: 60Hrs**

Text Books:

1. M. J. S. Smith, “Application Specific Integrated Circuits” , Addison – Wesley L Ongnam Inc., 1997.

References:

1. Andrew Brown, “VLSI Circuits and Systems in Silicon”, McGraw Hill 1991.
2. S. D. Brown, R. J. Francis, J. ROX, Z. G. Urines, “Field Programmable Publishers, 1992.
3. Mohammed Ismail and Terri Fief, “Analog VLSI and Modern Signal Processing,” McGraw Hill 1994.

4. S. Y. Kang, H. J. While Hours, T. Kailath, “VLSI Modern Signal Processing,” Prentice Hall, 1985. Jose E. France, Yantis Tsividis, “Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing”, Prentice Hall, 1994.

RESEARCH METHODOLOGY 3 0 0 3

1. RESEARCH CONCEPTS 9

Concepts, meaning, objectives, motivation, types of research, approaches, research (Descriptive research, Conceptual, Theoretical, Applied & Experimental).

Formulation of Research Task – Literature Review, Importance & Methods, Sources, quantification of Cause Effect Relations, Discussions, Field Study, Critical Analysis of Generated Facts, Hypothetical proposals for future development and testing, selection of Research task.

2. MATHEMATICAL MODELING AND SIMULATION 9

Concepts of modeling, Classification of Mathematical Models, Modeling with Ordinary differential Equations, Difference Equations, Partial Differential equations, Graphs, Simulation, Process of formulation of Model based on Simulation.

3 EXPERIMENTAL MODELING 9

Definition of Experimental Design, Examples, Single factor Experiments, Guidelines for designing experiments. Process Optimization and Designed experiments, Methods for study of response surface, determining optimum combination of factors, Taguchi approach to parameter design.

4 ANALYSIS OF RESULTS 9

Parametric and Non-parametric, descriptive and Inferential data, types of data, collection of data (normal distribution, calculation of correlation coefficient), processing, analysis, error analysis, different methods, analysis of variance, significance of variance, analysis of covariance, multiple regression, testing linearity and non-linearity of model.

5 REPORT WRITING 9

Types of reports, layout of research report, interpretation of results, style manual, layout and format, style of writing, typing, references, tables, figures, conclusion, appendices.

TOTAL: 45

TEXT BOOKS

1. Willktnsion K. L, Bhandarkar P. L, „Formulation of Hypothesis‟, Himalaya Publication.

2. Schank Fr., „Theories of Engineering Experiments", Tata Mc Graw Hill Publication.

REFERENCE BOOKS

1. Douglas Montgomary, „Design of Experiments", Statistical Consulting Services, 1990.

2. Douglas H. W. Allan, „Statistical Quality Control: An Introduction for Management", Reinhold Pub Corp, 1959.

3. Cochran and Cocks, „Experimental Design", John Willy & Sons.

4. John W. Besr and James V. Kahn, „Research in Education", PHI Publication.

5. Adler and Granovky, „Optimization of Engineering Experiments", Meer Publication.

6. S. S. Rao, „Optimization Theory and Application", Wiley Eastern Ltd., New Delhi, 1996.