Course Number and Name
BEC702 - DIGITAL CMOS VLSI

Credits and Contact Hours
4 and 60

Course Coordinator’s Name
Ms M. Jasmin

Text Books and References
6. J.Bhasker: Verilog HDL primer, BS publication,2001

Course Description
- To learn basic CMOS Circuits.
- To learn CMOS process technology.
- To learn techniques of chip design using programmable devices.
- To learn the concepts of designing adders and multipliers.

Prerequisites

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<th>Principles of Digital Electronics</th>
<th>Co-requisites</th>
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<td>Required, elective, or selected elective (as per Table 5-1)</td>
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Co-requisites

Required

Course Outcomes (COs)
CO1 To learn about IC fabrication, MOS transistor action and its parameters.
CO2 Express the Layout of simple MOS circuit using Lambda based design rules.
CO3 About the design of various adders and multipliers in VLSI technology.
CO4 About the design styles of FPGA.
CO5 About testing of CMOS circuits.
CO6 To understand the concepts of modeling a digital system using Hardware Description Language

Student Outcomes (SOs) from Criterion 3 covered by this Course

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List of Topics Covered

UNIT I  INTRODUCTION TO MOS TRANSISTOR  12

MOS Fabrication,  Enhancement mode and Depletion mode MOSFET,  Threshold voltage derivation – body effect – Drain current Vs voltage derivation – channel length modulation – CMOS technologies, CMOS Fabrication: n-well – p-well – twin tub – DC transfer characteristics

UNIT II MOS CIRCUITS DESIGN PROCESS AND CMOS LOGIC GATES  12


UNIT III VLSI IMPLEMENTATION STRATEGIES  12


UNIT IV CMOS TESTING  12

Need for testing- Testers, Text fixtures and test programs- Logic verification- Silicon debug principles- Manufacturing test – Design for testability – Boundary scan

UNIT V SPECIFICATION USING VERILOG HDL  12

Basic concepts- identifiers- gate primitives, gate delays, operators, timing controls, procedural assignments conditional statements, Data flow and RTL, structural gate level, switch level modeling, Design hierarchies, Behavioral and RTL modeling, Test benches, Design of decoder, equality detector, comparator, priority encoder, half adder, full adder, Ripple carry adder, D latch and D flip flop

Total: 60 Periods