Course Number and Name
BEC302 - PRINCIPLES OF DIGITAL ELECTRONICS

Credits and Contact Hours
4 & 60

Course Coordinator’s Name
Dr M. Sangeetha

Text Book and References

**TEXT BOOK:**

**REFERENCES:**

Course Description
To manipulate across various number systems and to compute binary arithmetic operations.
To understand the design of combinational and sequential circuits using gates.
To know the concept of memories and programmable logic devices
To learn the design of asynchronous and synchronous sequential circuits.

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<th>Prerequisites</th>
<th>Co-requisites</th>
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<tr>
<td>Basic Electrical &amp; Electronics Engineering</td>
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<td>Required, elective, or selected elective (as per Table 5-1)</td>
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Course Outcomes (COs)

CO1 - Recall the different number systems and demonstrate the simplification of Boolean expressions using Boolean algebra & K-Map method.

CO2 - Analyze the Combinational building blocks

CO3 - Analyze the sequential building blocks.

CO4 - Develop a state diagram and simplify the given sequential logic

CO5 - To illustrate the concept of synchronous sequential circuits

CO6 - To illustrate the concept of asynchronous sequential circuits

Student Outcomes (SOs) from Criterion 3 covered by this Course

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<th>COs/SOs</th>
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List of Topics Covered

UNIT I BASIC CONCEPTS, BOOLEAN ALGEBRA AND LOGIC GATES
Number systems - Binary, Octal, Decimal, Hexadecimal, conversion from one to another, complement arithmetic, Boolean theorems of Boolean algebra, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map, Quine-McCluskey method of minimization, NAND-NOR implementation of Logic gates, Multilevel gate implementation, Multi output gate implementation, TTL and CMOS logic and their characteristics, Tristate gates.

UNIT II COMBINATIONAL CIRCUITS

UNIT III SEQUENTIAL CIRCUIT

UNIT IV MEMORY DEVICES
Classification of memories – ROM, ROM organization - PROM, EPROM, EEPROM, EAPROM, RAM – RAM organization – Write operation, Read operation, Memory cycle, Timing wave forms, Memory decoding, memory expansion, Static RAM Cell, Dynamic RAM cell, Programmable Logic Devices – Programmable Logic Array (PLA) and Programmable Array Logic (PAL), Field Programmable Gate Arrays (FPGA), Implementation using ROM, PLA, and PAL.

UNIT V SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS
Synchronous Sequential Circuits: General Model – Classification – Design – Use of Algorithmic State Machine – Analysis of Synchronous Sequential Circuits.