Course Number and Name
BEC001 - ADVANCED COMPUTER ARCHITECTURE

Credits and Contact Hours
3 and 45

Course Coordinator’s Name
Ms C. Geetha

Text Books and References

TEXT BOOKS:

REFERENCES:
2. www.sci.tamucc.edu/~sking/Courses/COSC5351/syllabus.php

Course Description
- To make students know about the Parallelism concepts in Programming
- To give the students an elaborate idea about the different memory systems and buses.
- To introduce the advanced processor architectures to the students.
- To make the students know about the importance of multiprocessor and multi-computers.
- To study about data flow computer architectures

Prerequisites
Principles of digital electronics

Co-requisites
Microprocessor & Microcontroller required, elective, or selected elective (as per Table 5-1)
Selected Elective

Course Outcomes (COs)
CO1: Demonstrate concepts of parallelism in hardware/software.
CO2: Discuss memory organization and mapping techniques.
CO3: Describe architectural features of advanced processors.
CO4: Interpret performance of different pipelined processors.
CO5: Explain data flow in arithmetic algorithms
CO6: Development of software to solve computationally intensive problems.

Student Outcomes (SOs) from Criterion 3 covered by this Course
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<th>List of Topics Covered</th>
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<td><strong>UNIT- I</strong></td>
<td><strong>9</strong></td>
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<tr>
<td>PARALLEL COMPUTER MODELS</td>
<td>Evolution of Computer architecture, system attributes to performance, Multi processors and multi computers, Multi-vector and SIMD computers, PRAM and VLSI models-Parallelism in Programming, conditions for Parallelism-Program Partitioning and Scheduling-program flow Mechanisms-Speed up performance laws-Amdahl's law, Gustafson's law-Memory bounded speedup Model.</td>
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<td><strong>UNIT- II</strong></td>
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<td>MEMORY SYSTEMS AND BUSES</td>
<td>Memory hierarchy-cache and shared memory concepts-Cache memory organization-cache addressing models, Aliasing problem in cache, cache memory mapping techniques-Shared memory organization-Interleaved memory organization, Lower order interleaving, Higher order interleaving. Back plane bus systems-Bus addressing, arbitration and transaction.</td>
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<td><strong>UNIT -III</strong></td>
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<td>ADVANCED PROCESSORS</td>
<td>Instruction set architectures-CISC and RISC scalar processors-Super scalar processors-VLIW architecture- Multivector and SIMD computers-Vector processing principles-Cray Y-MP 816 system-Inter processor communication</td>
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<td><strong>UNIT- IV</strong></td>
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<td>MULTI PROCESSOR AND MULTI COMPUTERS</td>
<td>Multiprocessor system interconnects- Cross bar switch, Multiport memory-Hot spot problem, Message passing mechanisms-Pipelined processors-Linear pipeline, on linear pipeline-Instruction pipeline design-Arithmetic pipeline design.</td>
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<td><strong>UNIT- V</strong></td>
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<td>DATA FLOW COMPUTERS AND VLSI COMPUTATIONS</td>
<td>Data flow computer architectures-Static, Dynamic-VLSI Computing Structures-Systolic array architecture, mapping algorithms into systolic arrays, Reconfigurable processor array-VLSI matrix arithmetic processors-VLSI arithmetic models, partitioned matrix algorithms, matrix arithmetic pipelines.</td>
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