Unit - I

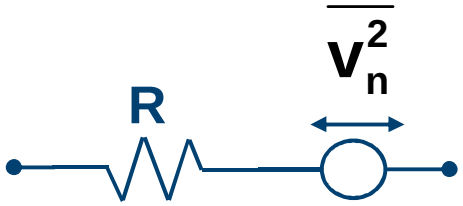
SINGLE STAGE AMPLIFIERS

Outline – Part II

- Noise in analog ICs
- Matching in analog ICs
- Operational Amplifier design examples
- Analog design methodology

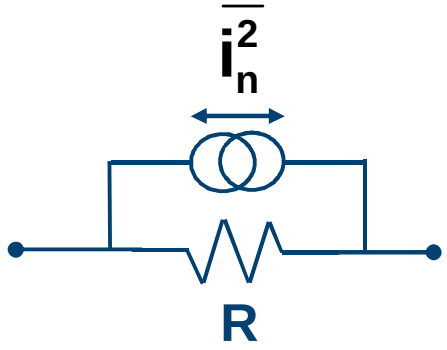
Thermal noise in passive components

Thermal noise is caused by the random thermally excited vibration of the charge carriers in a conductor.



Power spectral density [V^2 / Hz]

$$\overline{v_n^2} = 4kTR \cdot \Delta f \quad [\ V^2\ ]$$



$$\overline{i_n^2} = \frac{4kT}{R} \cdot \Delta f \quad [\ A^2\ ]$$

There are no sources of noise in ideal capacitors or inductors. In practice, real components have parasitic resistance that does display thermal noise!

Noise sources in MOS transistors

Channel thermal noise: **due to the random thermal motion of the carriers in the channel**

1/f noise: **due to the random trapping and detrapping of mobile carriers in the traps located at the Si-SiO_2 interface and within the gate oxide.**

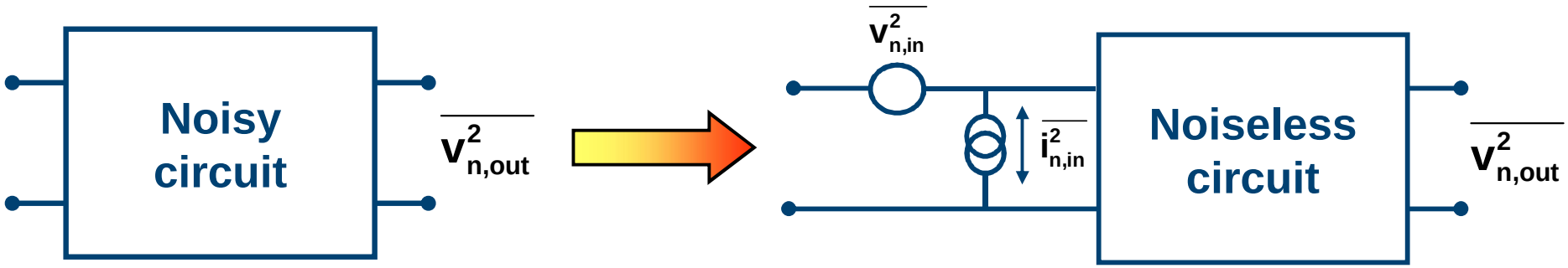
Bulk resistance thermal noise: **due to the distributed substrate resistance.**

Gate resistance thermal noise: **due to the resistance of the polysilicon gate and of the interconnections.**

Noise in circuits

To be independent from the gain of a given system, we use the concept of input-referred noise. This allows comparing easily the noise performance of different circuits (with different gains), and calculating easily the Signal-to-Noise Ratio (SNR).

At the input of our linear two-port circuit, we use two noise generator (one noise voltage source and one noise current source) to represent the noise of the system regardless the impedance at the input of the circuit and of the source driving the circuit.



Input-referred voltage noise

The MOS transistor is represented by its small-signal equivalent circuit. We can refer the noise sources inside the MOS transistor to the input, obtaining an input-referred voltage noise.

$$\frac{\overline{v_{in}^2}}{\Delta f} = 4kTn\gamma\frac{1}{g_m} + \frac{K_a}{C_{ox}^2 WL}\frac{1}{f^{\alpha}} + 4kTR_G + 4kT\frac{g_{mb}^2}{g_m^2}R_B$$

Channel thermal noise	1/f noise	Gate resistance thermal noise	Bulk resistance thermal noise

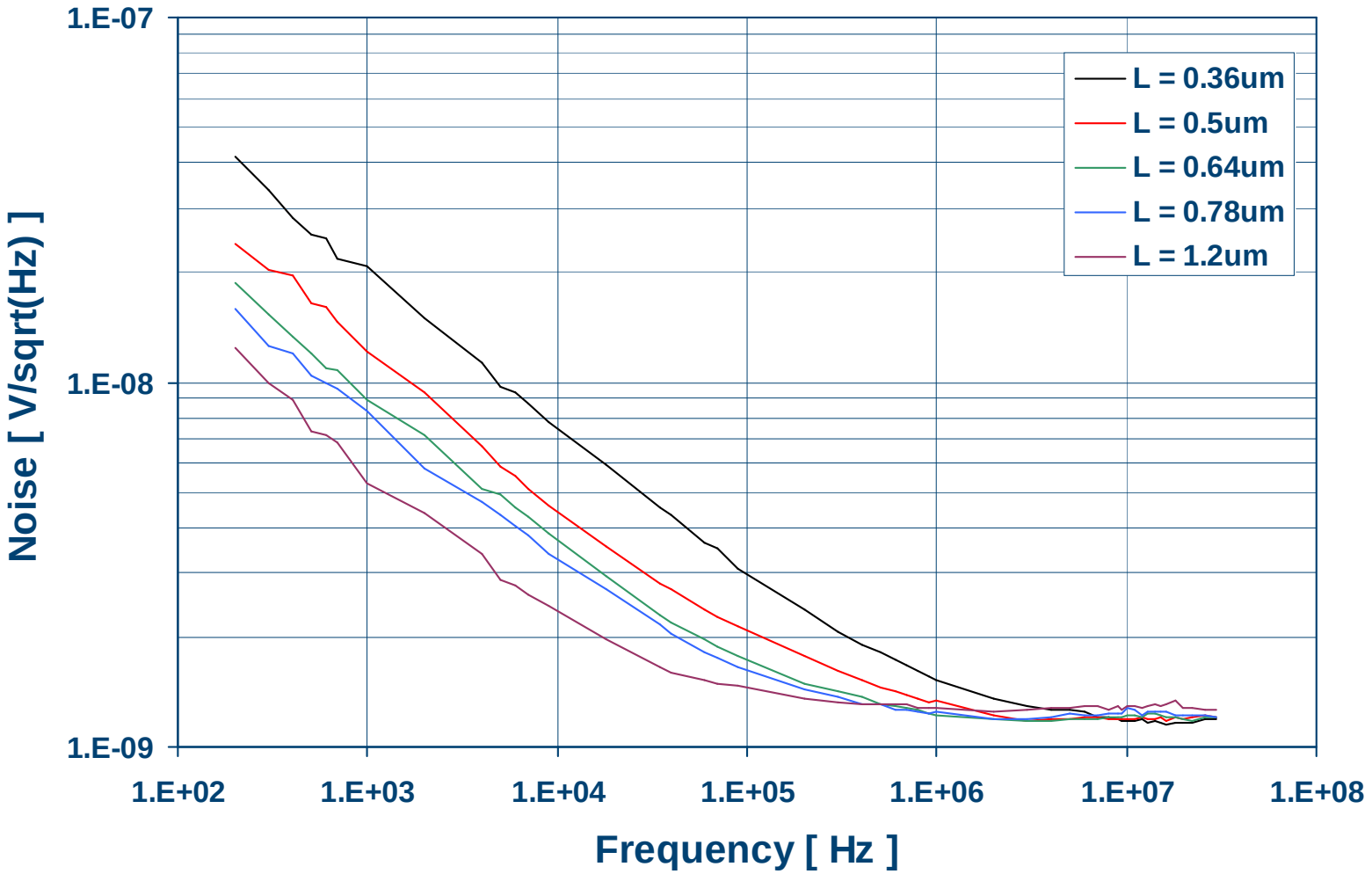
γ ideally varies from 1/2 (w.i.) to 2/3 (s.i.)

K_a = 1/f noise parameter, technology dependent

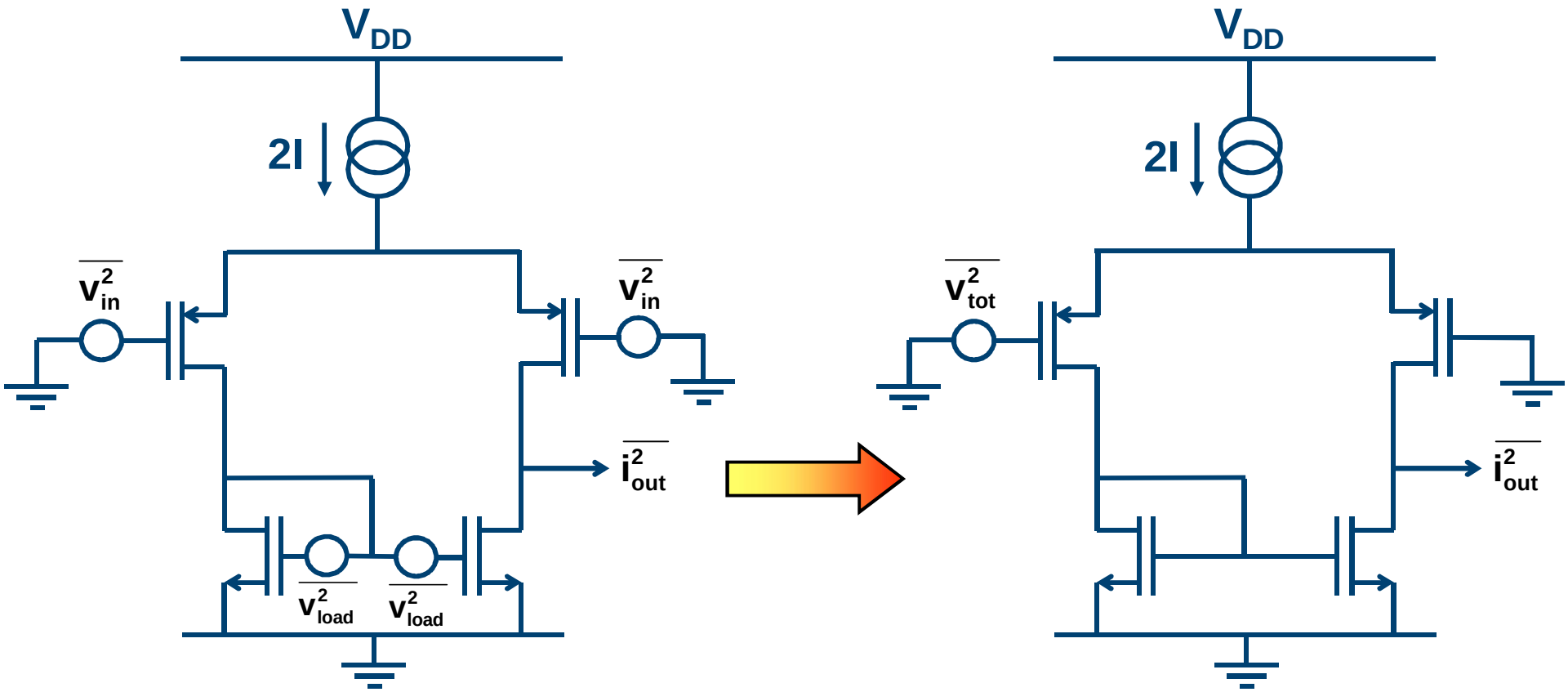
Usually, the first two terms are the most important

N-channel noise spectra

W = 2 mm, I_{DS} = 0.5 mA, V_{DS} = 0.8 V, V_{BS} = 0 V

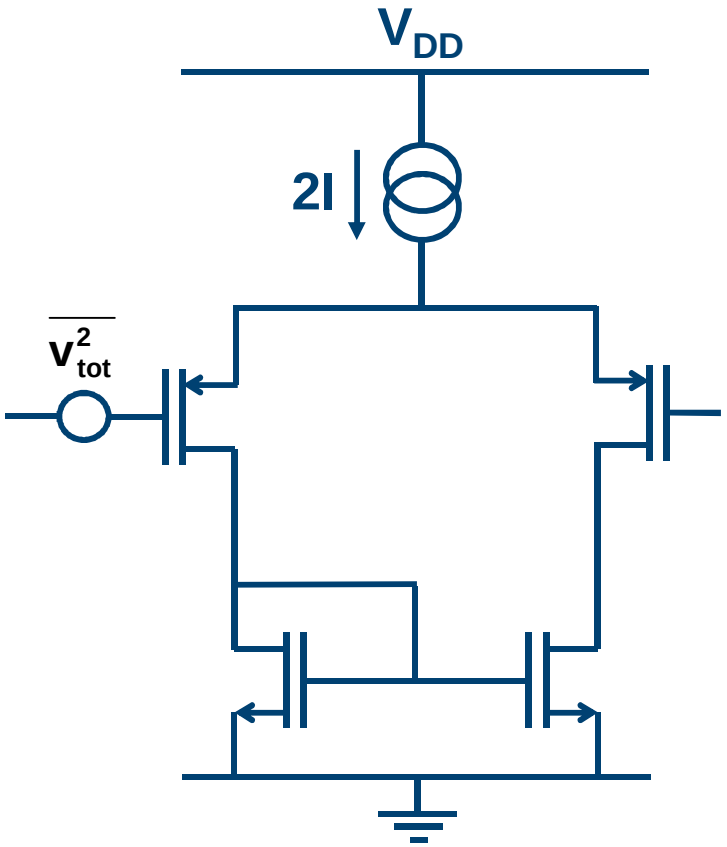


Noise in a DP + Active CM



$$\overline{v_{tot}^2} = 2 \cdot \overline{v_{in}^2} + 2 \cdot \left(\frac{g_{m\_load}^2}{g_{m\_in}^2} \right) \cdot \overline{v_{load}^2}$$

Noise in a DP + Active CM



$$\overline{v_{tot\_1/f}^2} = 2 \cdot \frac{K_{a\_in}}{C_{ox}^2 W_{in} L_{in}} \cdot \frac{1}{f} \cdot \left(1 + \frac{K_{a\_load} \cdot \mu_{load} \cdot L_{in}^2}{K_{a\_in} \cdot \mu_{in} \cdot L_{load}^2} \right) \cdot \Delta f$$

Make $W_{in} L_{in}$ big and $L_{load} > L_{in}$

$$\overline{v_{tot\_th}^2} = 4kTn\gamma \cdot \frac{2}{\sqrt{2\mu_{in} C_{ox} \frac{W_{in}}{L_{in}} I}} \cdot \left(1 + \sqrt{\frac{\mu_{load} \left(\frac{W}{L} \right)_{load}}{\mu_{in} \left(\frac{W}{L} \right)_{in}}} \right) \cdot \Delta f$$

Make $\left(\frac{W}{L} \right)_{in} > \left(\frac{W}{L} \right)_{load}$

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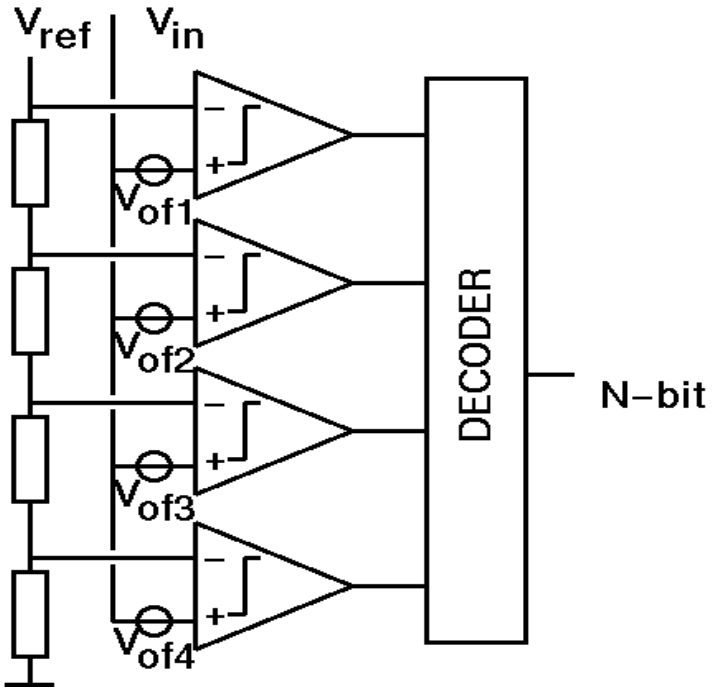
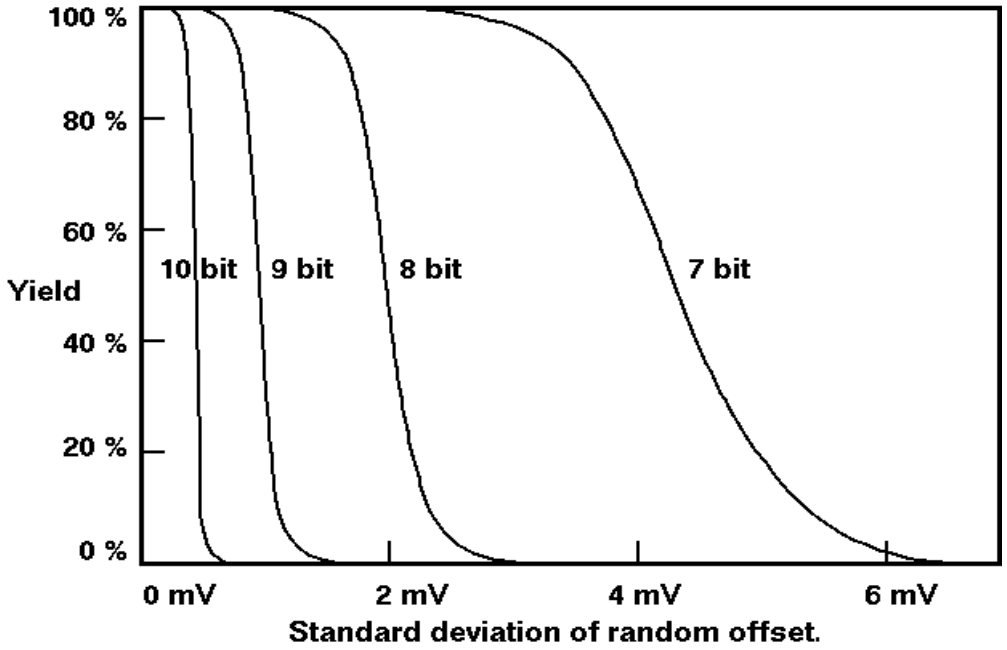
The importance of matching

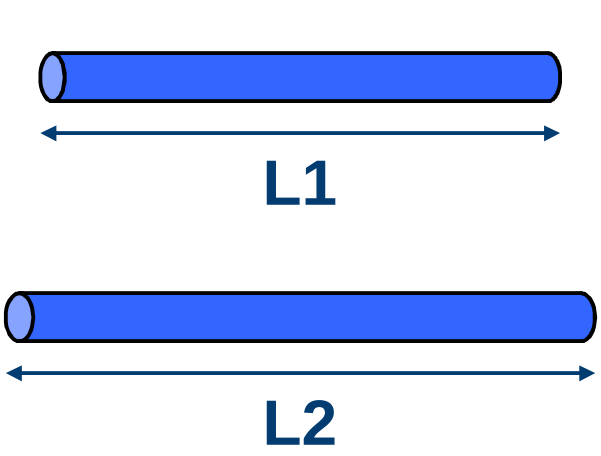
Yield of an N-bit flash Analog-to-Digital converter as a function of the comparator mismatch

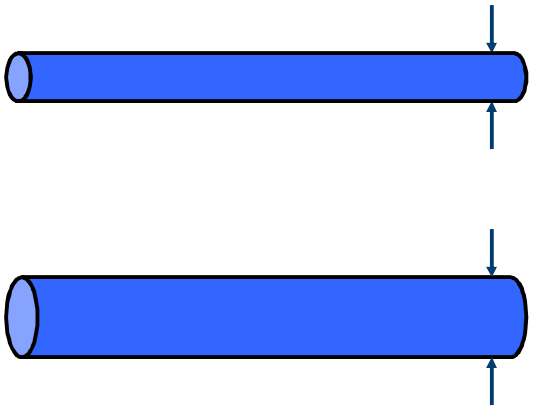




Relative & absolute mismatch

Mismatch occurs for all IC components (resistors, capacitors, bipolar and MOS transistors)





$$\frac{\Delta L}{L} = 200 \cdot \frac{L2 - L1}{L2 + L1} \; [\%]$$

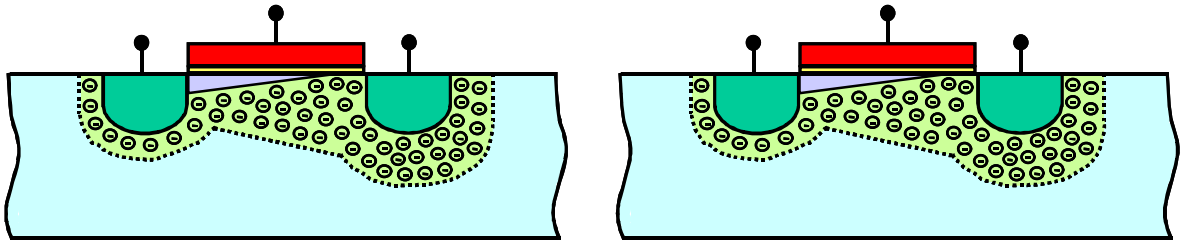
Relative mismatch

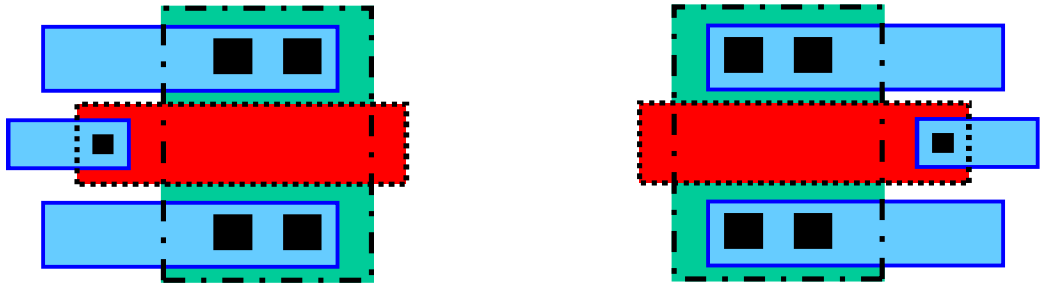
$$\Delta D = \Delta D1 - \Delta D2 \quad [\mu m]$$

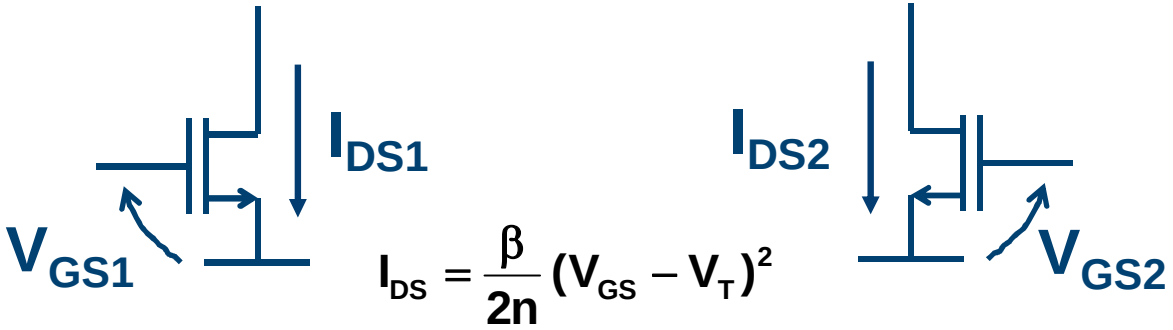
Absolute mismatch

Mismatch in MOS transistors

Mismatch in physical parameters (N_a, μ, T_{ox}) and layout dimensions (W, L) gives origin to mismatch in electrical parameters (V_T, β and therefore I_D)







$$I_{DS} = \frac{\beta}{2n}(V_{GS} - V_T)^2$$

Mismatch in N_a, μ, T_{ox}

+

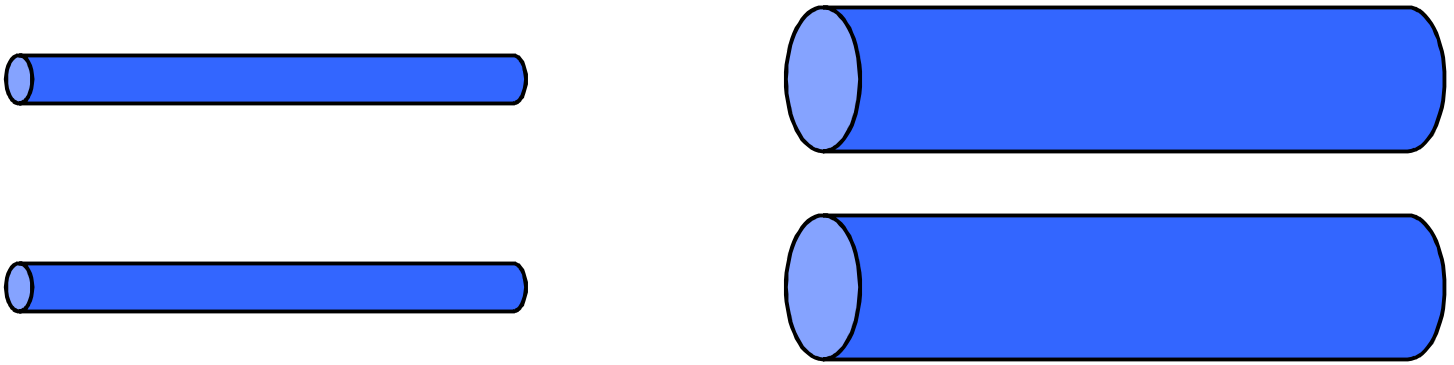
Mismatch in W and L

⇩

Parameter mismatch ΔV_T and $\frac{\Delta\beta}{\beta}$

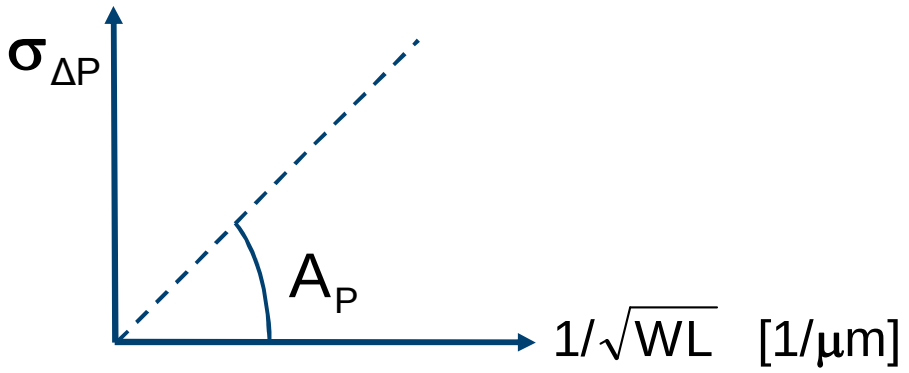
I mismatch and V offset ΔV_{GS} and $\frac{\Delta I_D}{I_D}$

The golden rule: Bigger is better!



Random effects "average out" better if the area is bigger. Therefore, for a given parameter P, we expect something like

$$\sigma_{\Delta P} = \frac{A_P}{\sqrt{W\,L}}$$



Expected mismatch

Usually in a pair of identical transistors the two most important parameter subject to mismatch are the threshold voltage V_{th} and the current factor β

$$\sigma_{\Delta V_{th}} = \frac{A_{V_{th}}}{\sqrt{W\,L}} \qquad \sigma_{\Delta\beta/\beta} = \frac{A_{\beta}}{\sqrt{W\,L}}$$

$A_{Vth} / t_{ox} \sim 1\ mV \cdot \mu m / nm$

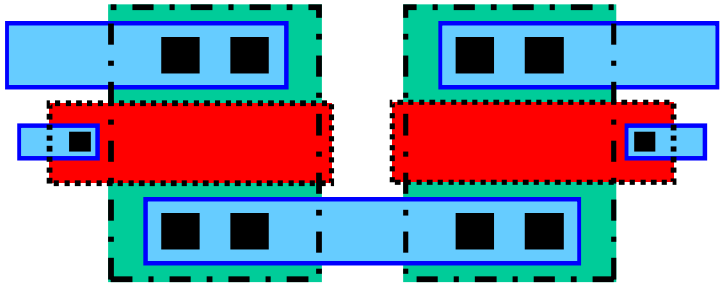
$A_{\beta} \sim 1$ to $3\ \% \cdot \mu m$

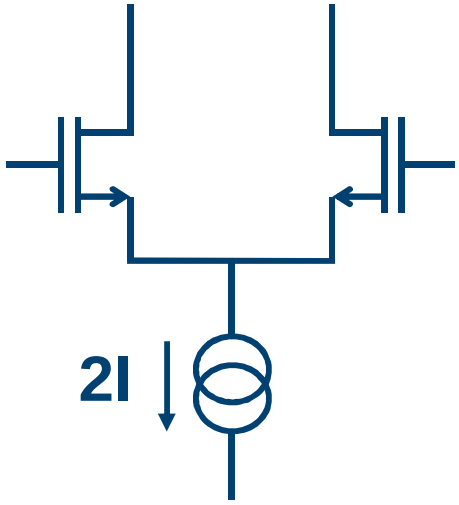
} From the literature

Mismatch can be treated as another source of noise. As in the noise case, different "mismatch" sources can be grouped into one adding the variances (not the standard deviations)

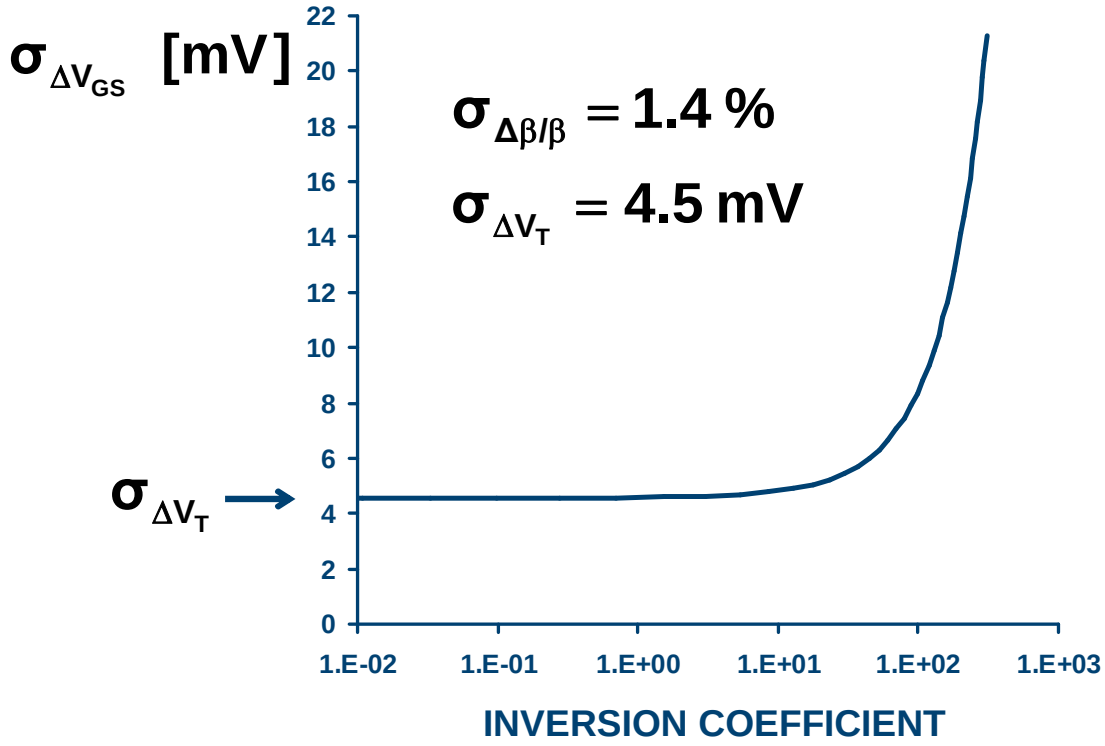
Differential pair mismatch

The two transistors have the same drain current



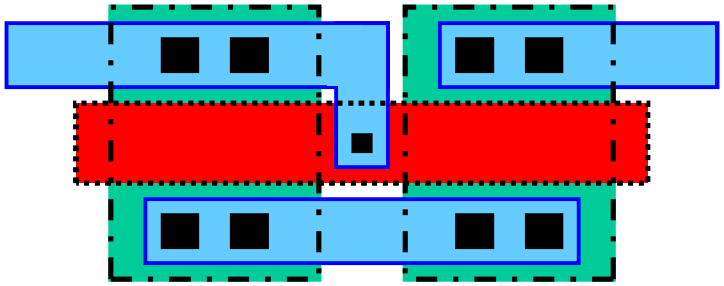


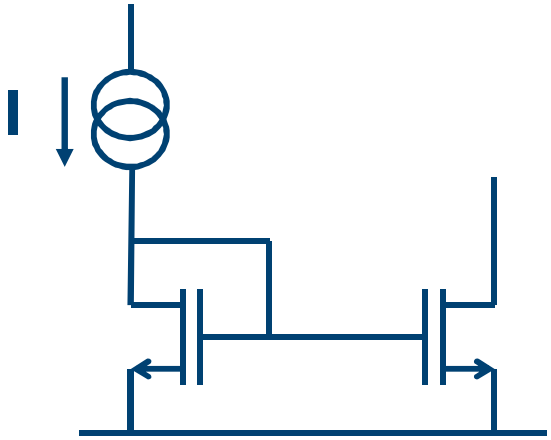
$$\sigma_{\Delta V_{GS}} = \sqrt{\sigma^2_{\Delta V_{th}} + \left(\frac{I}{g_m}\sigma_{\Delta\beta/\beta}\right)^2}$$



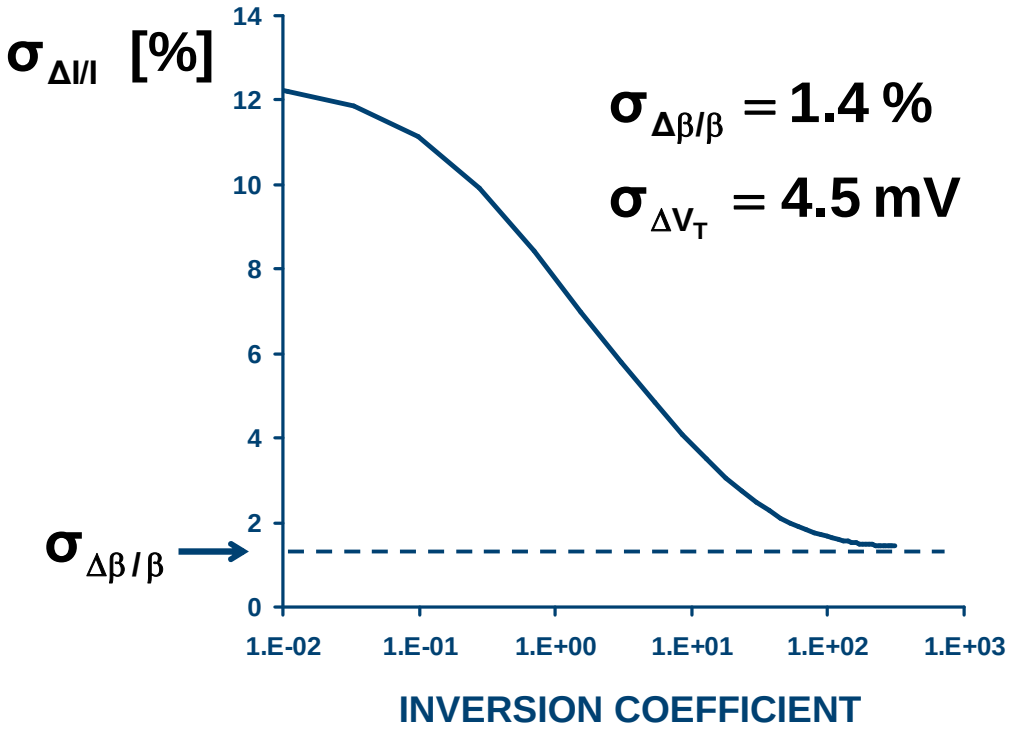
Current mirror mismatch

The two transistors have the same gate voltage

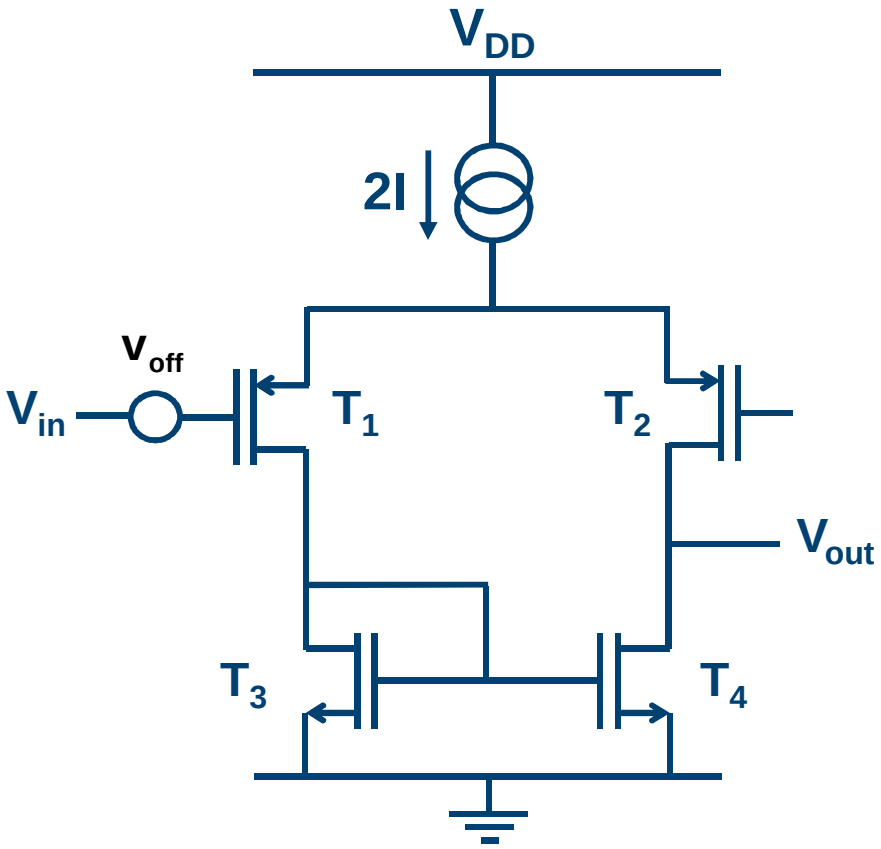




$$\sigma_{\Delta I/I} = \sqrt{\sigma^2_{\Delta\beta/\beta} + \left(\frac{g_m}{I}\sigma_{\Delta V_{th}}\right)^2}$$



Offset of a DP + Active CM



RANDOM OFFSET (WORST CASE)

$$v_{off} = \Delta V_{T1,2} + \frac{I}{g_{m1,2}}\left(\frac{\Delta\beta_{1,2}}{\beta_{1,2}} + \frac{\Delta\beta_{3,4}}{\beta_{3,4}} + \frac{g_{m3,4}}{I}\Delta V_{T3,4}\right)$$

SYSTEMATIC OFFSET

The difference in the drain voltages of T1 and T2 gives origin a difference in the DC currents in the two branches.

“COMMON MODE” OFFSET

Due to mismatches in the transistors, a common mode signal at the input gives a non zero output voltage signal.

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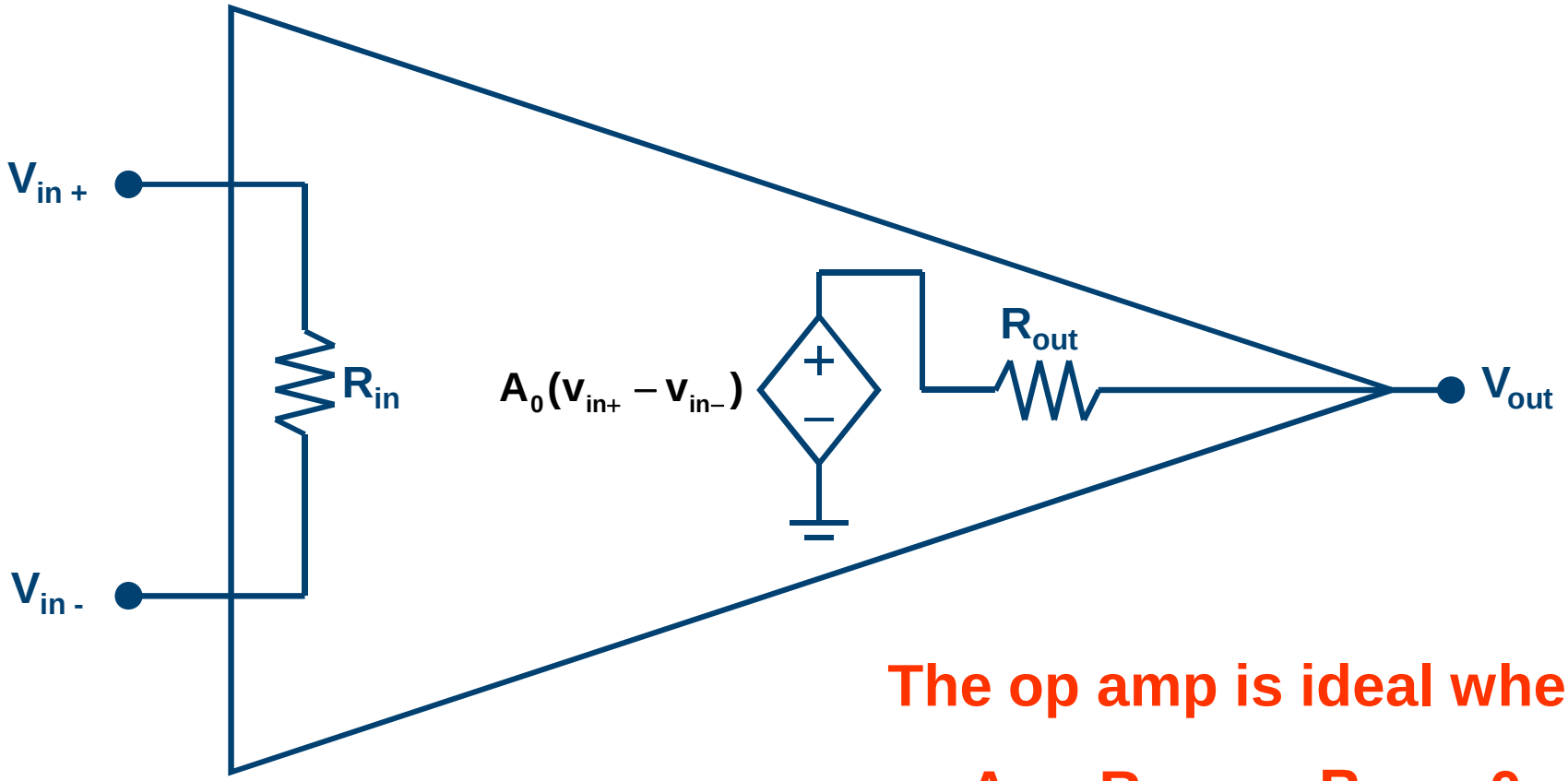
- Operational Amplifier design examples
  - Op Amp application examples
  - Single-Stage Op Amps
  - Two-Stage Op Amps
  - Fully Differential Op Amps
  - Feedback and frequency compensation
- Analog design methodology

The ideal op amp

An op amp is basically a voltage-controlled voltage source

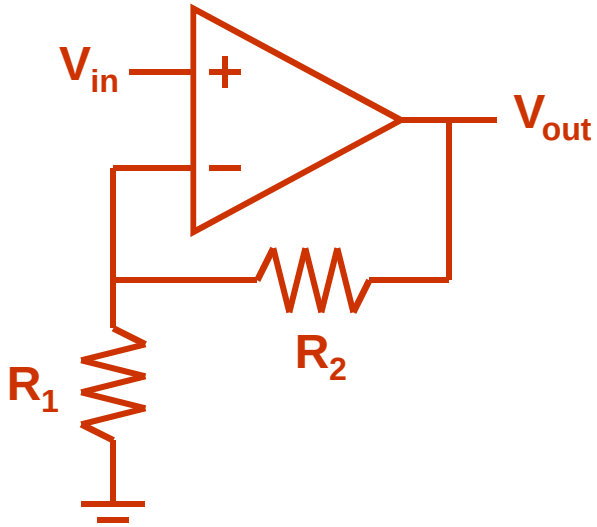


The op amp is ideal when

$$A_0 = R_{in} = \infty,\ R_{out} = 0$$

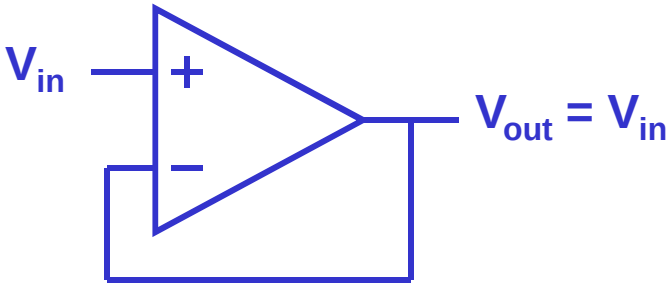
Op amp application examples

NONINVERTING CONFIGURATION



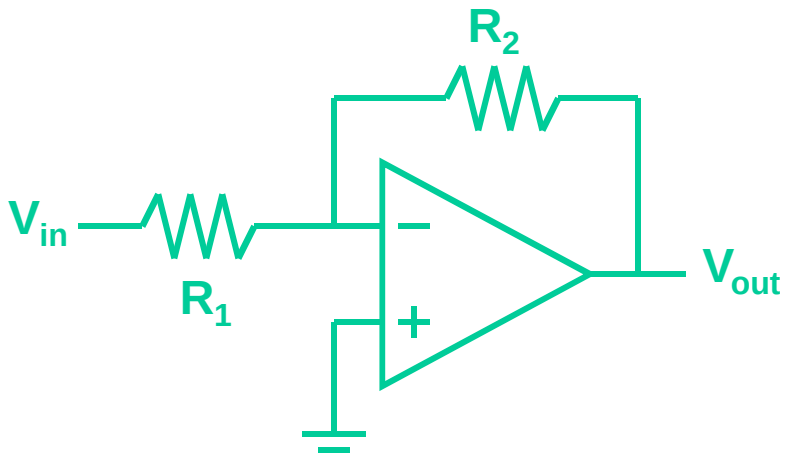
$$G = 1 + \frac{R_2}{R_1}$$

BUFFER



$$G = 1$$

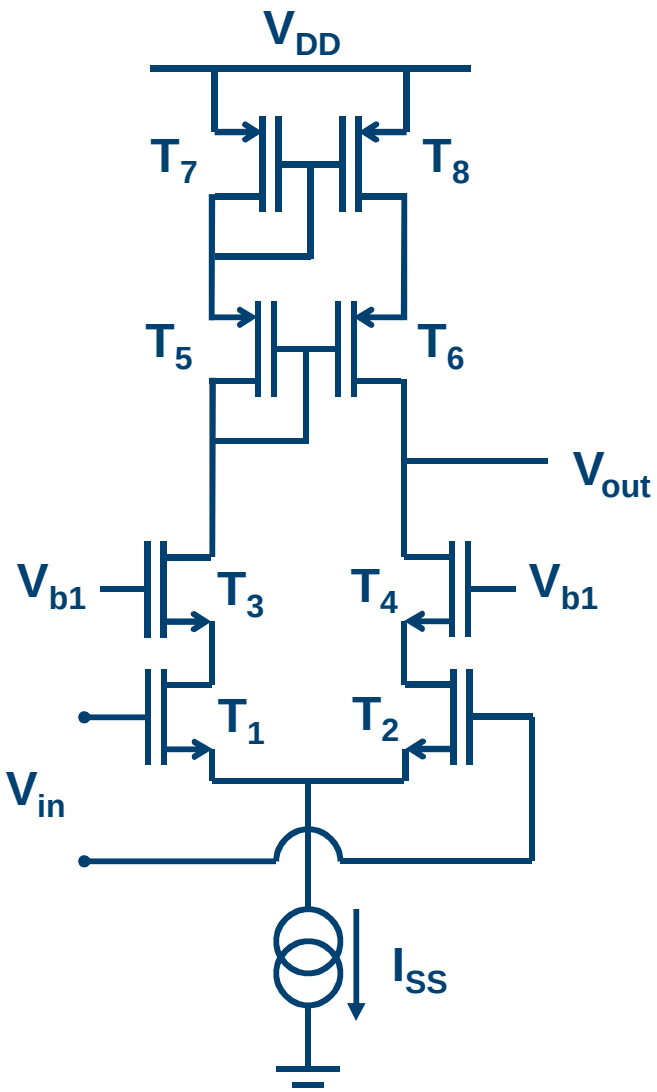
INVERTING CONFIGURATION



$$G = -\frac{R_2}{R_1}$$

The above equations are valid only if the gain A_0 of the op amp is very high!

Single-stage Op Amp



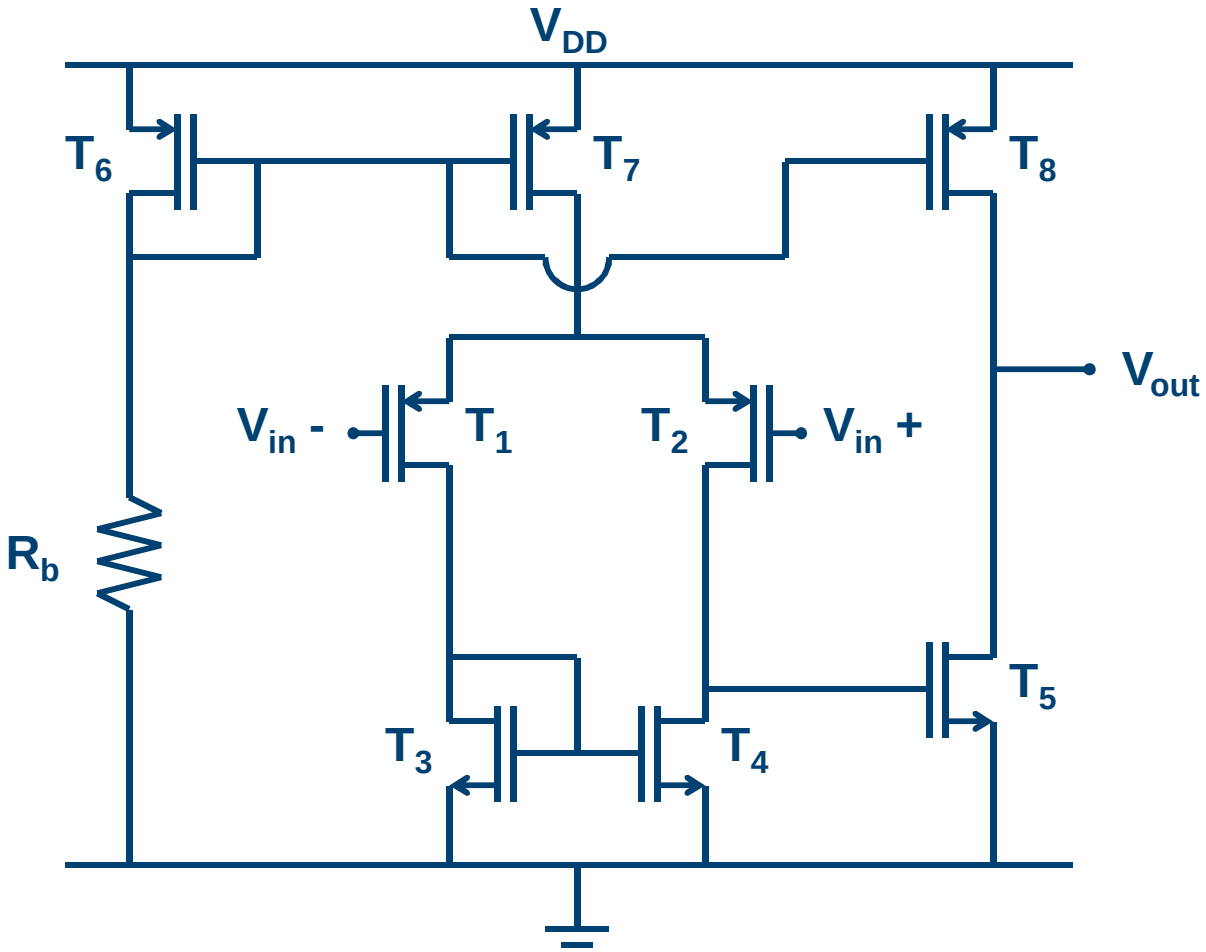
The differential pair + active current mirror scheme we have already seen is a single stage op amp. Several different solutions can be adopted to make a Single-stage amplifier. If high gains are needed, we can use, for example, cascode structures.

With single-stage amplifiers it is difficult to obtain at the same time high gain and voltage excursion, especially when other characteristics are also required, such as speed and/or precision.

Two-stage configurations in this sense are better, since they decouple the gain and voltage swing requirements.

Two-stage Op Amp

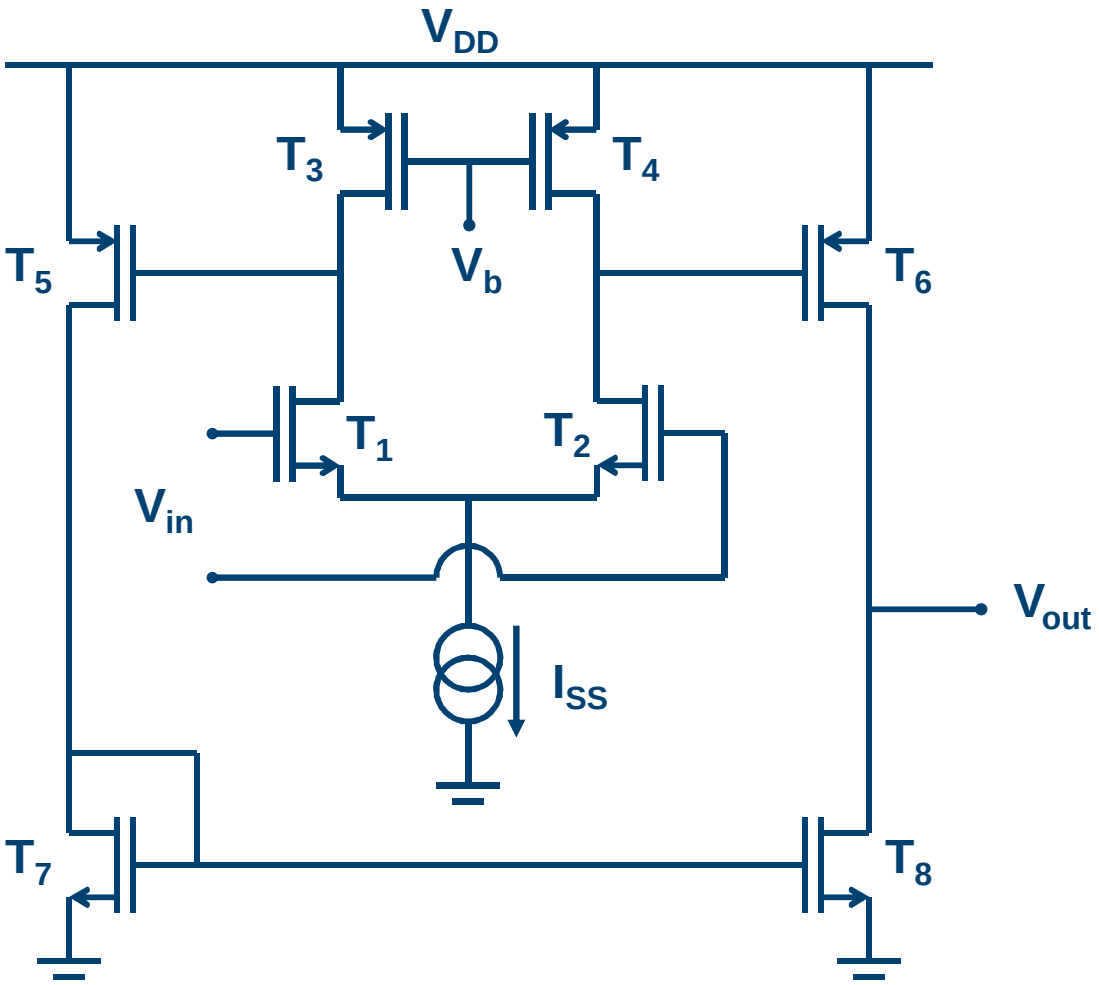
$$G = g_{m2}(r_{02} \,//\, r_{04}) \cdot g_{m5}(r_{05} \,//\, r_{08})$$



The second stage is very often a CSS, since this allows the maximum voltage swing.
The output voltage swing in this case is $V_{DD} - |2V_{DS\_SAT}|$

Two-stage Op Amp

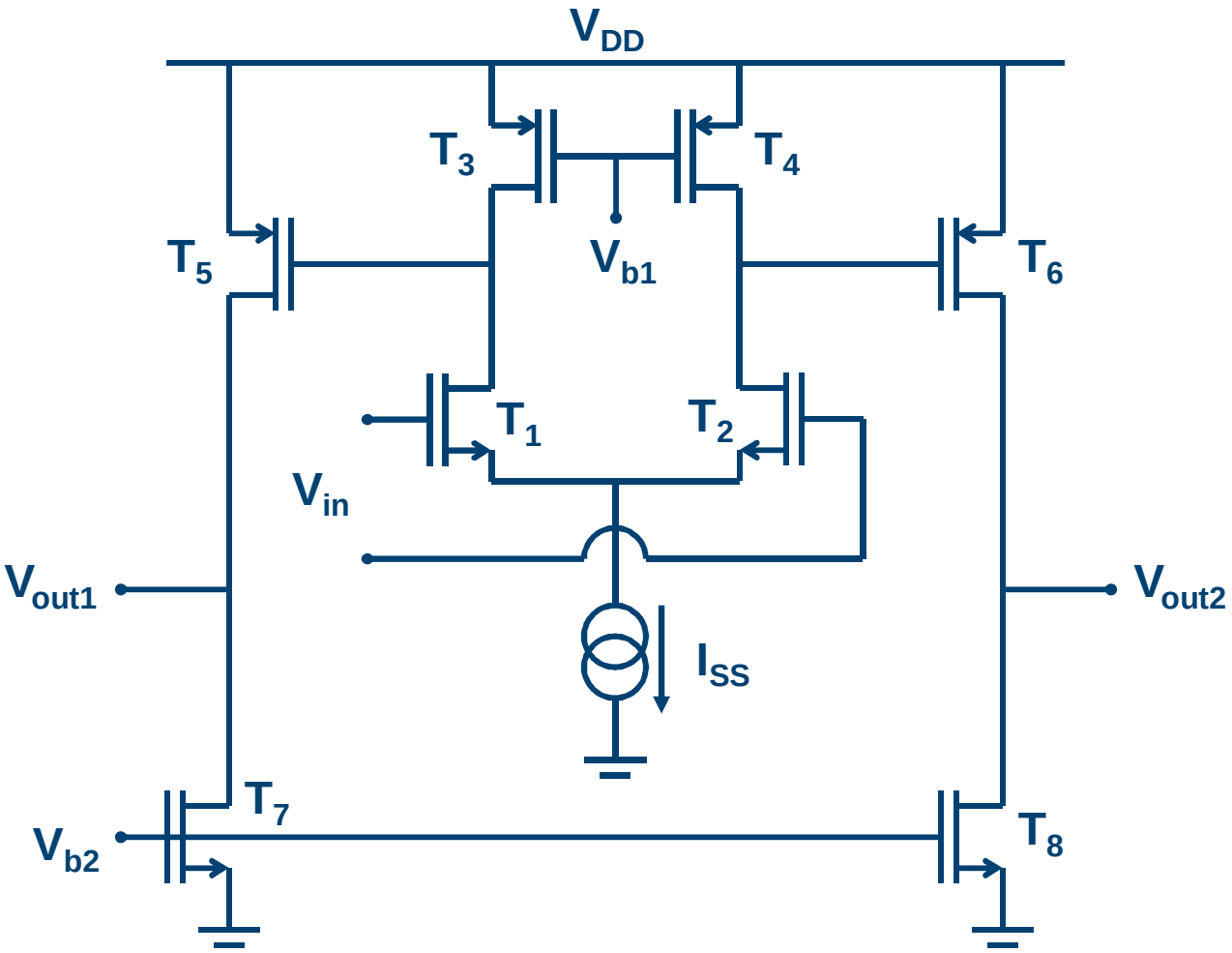
$$G = g_{m1,2}(r_{01,2} \,//\, r_{03,4}) \cdot g_{m6}(r_{06} \,//\, r_{08})$$



In this case we kept the differential behavior of the first stage, and is the current mirror T7-T8 which does the differential-to-single ended conversion. The output is still a CSS.

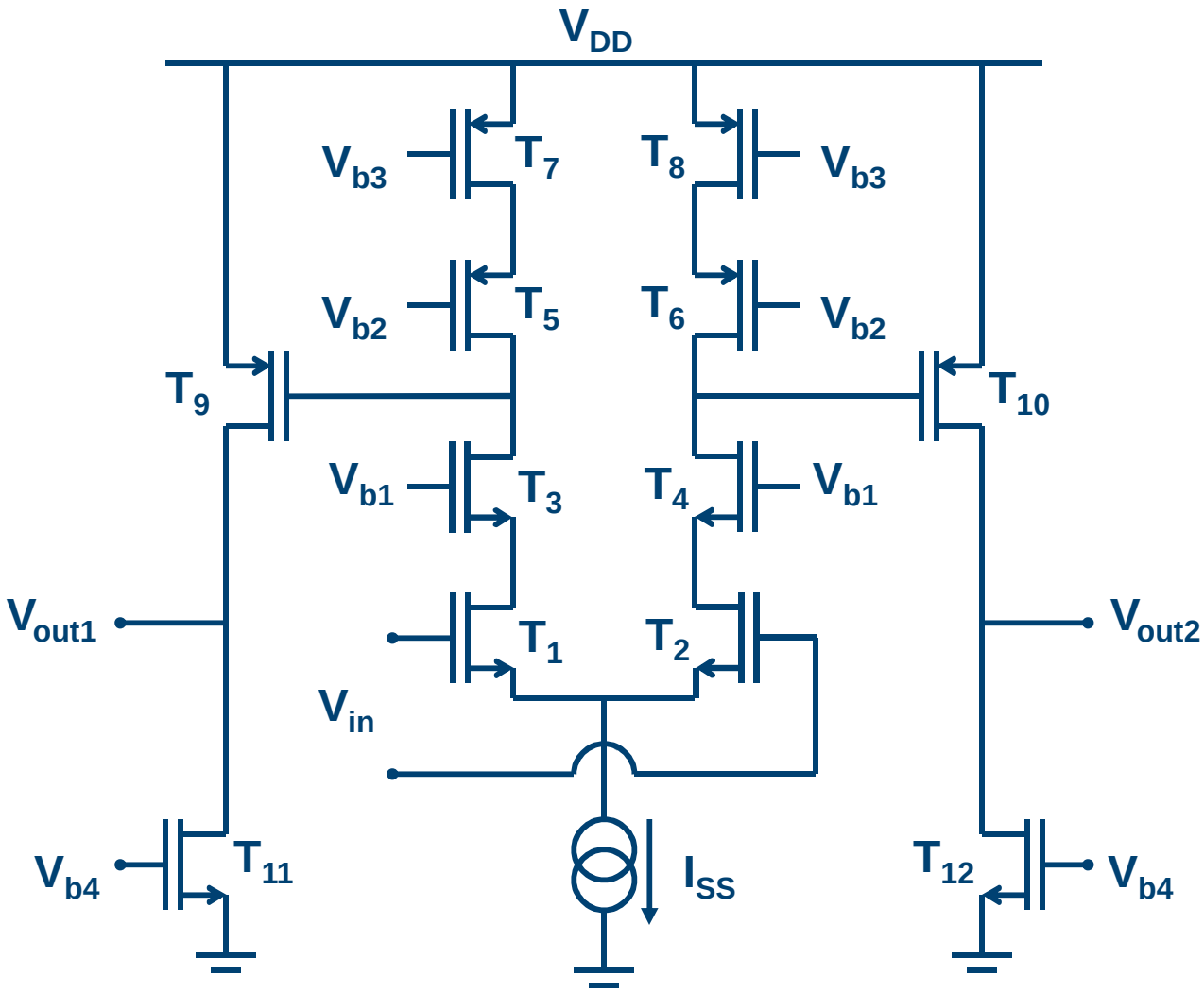
Fully Differential Op Amp

$$G = g_{m1,2}(r_{01,2} \,//\, r_{03,4}) \cdot g_{m5,6}(r_{05,6} \,//\, r_{07,8})$$



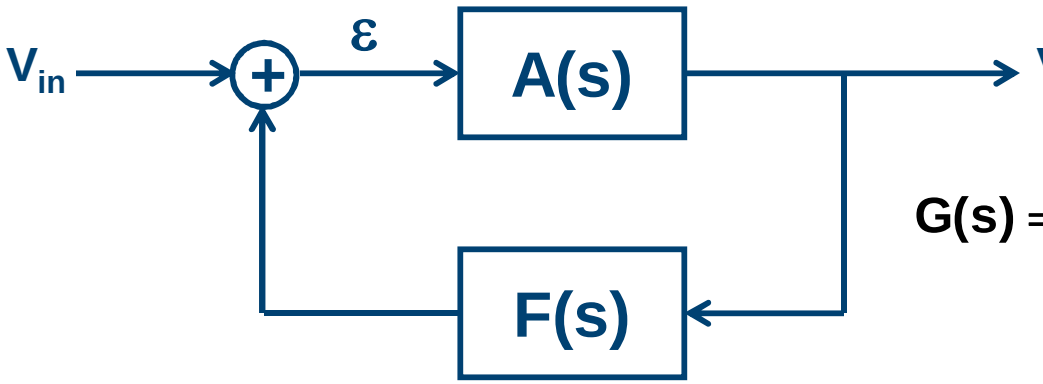
Fully Differential Op Amp

$$G = \left\{ g_{m1,2}\left[(g_{m3,4} + g_{mb3,4})r_{03,4}r_{01,2}\right] /\!/ \left[(g_{m5,6} + g_{mb5,6})r_{05,6}r_{07,8}\right] \right\} \cdot g_{m9,10}\left(r_{09,10} /\!/ r_{011,12}\right)$$



To increase the gain, we can again make use, in the first stage, of cascode structures.

Feedback



$$G(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{A(s)}{1 - A(s)F(s)} = \frac{A(s)}{1 - G_{loop}(s)}$$

- A(s) is the open loop transfer function
- F(s) is the feedback network transfer function
- G(s) is the closed loop transfer function
- A(s)F(s) is the loop gain
- If the feedback is negative, the loop gain is negative
- For $|G_{loop}(s)| >> 1$, we have that $G(s) = -\frac{1}{F(s)}$

Properties of negative feedback

Negative feedback reduces substantially the gain of a circuit, but it improves several other characteristics:

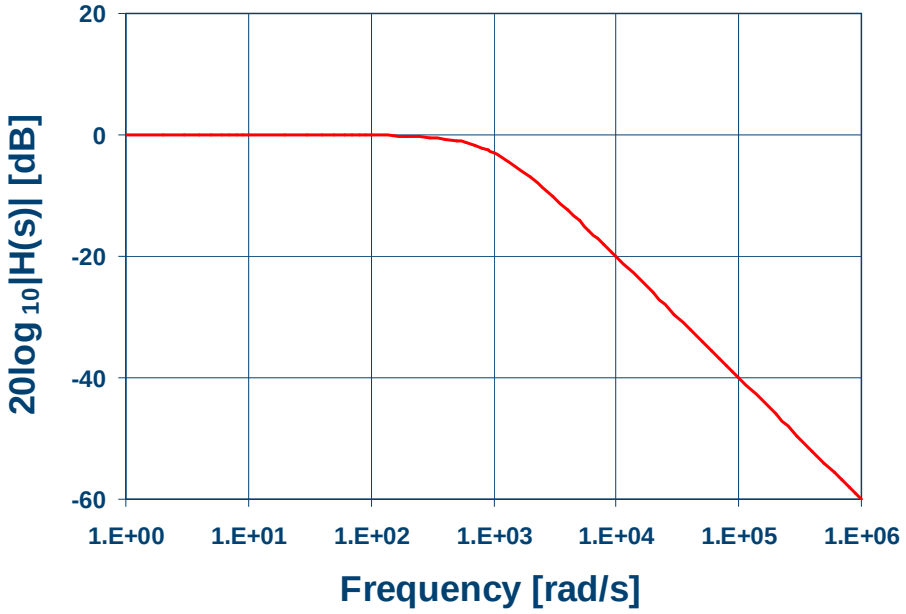
- **Gain desensitization: the open loop transfer function is generally dependent on many varying quantities, given by the active components in the circuit. Using a passive feedback network, we can reduce the dependence of the gain variation on the variations of the open loop transfer function.**

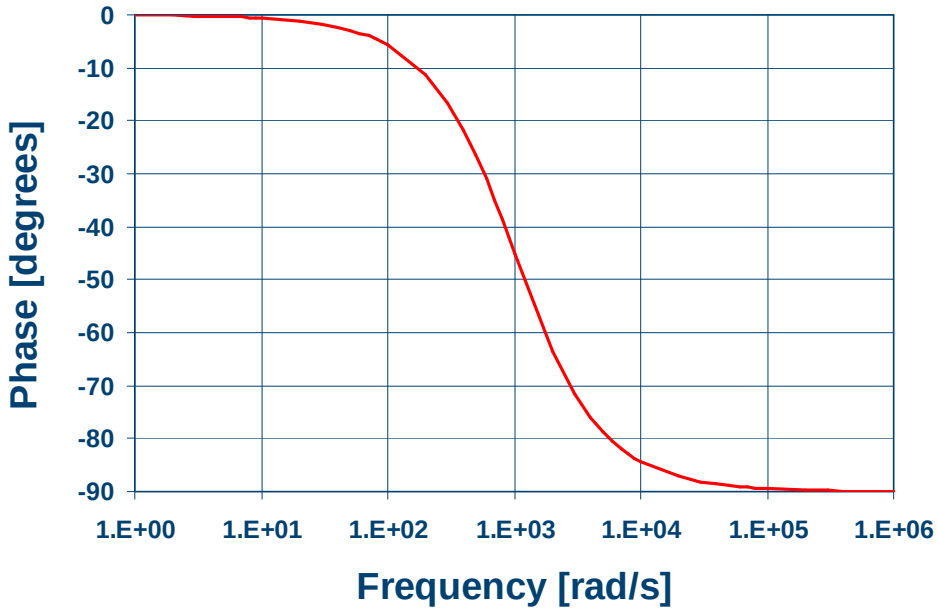
$$\frac{dG}{G} = \frac{dA}{A}\frac{1}{1 - G_{loop}}$$

- **Reduction of nonlinear distortion**
- **Reduction or increase (depending on the feedback topology) of the input and output impedances by a factor $1-G_{loop}$.**
- **Increase of the bandwidth**

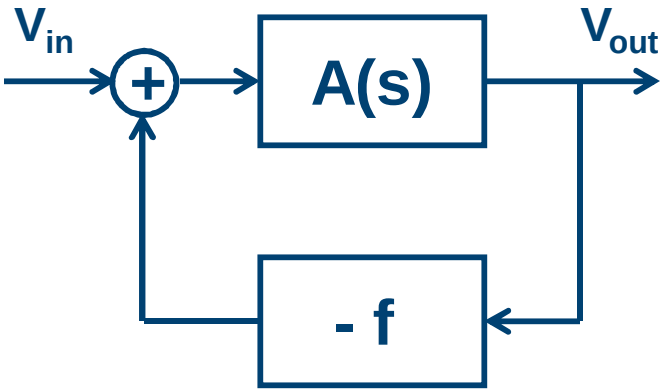
Bode diagrams

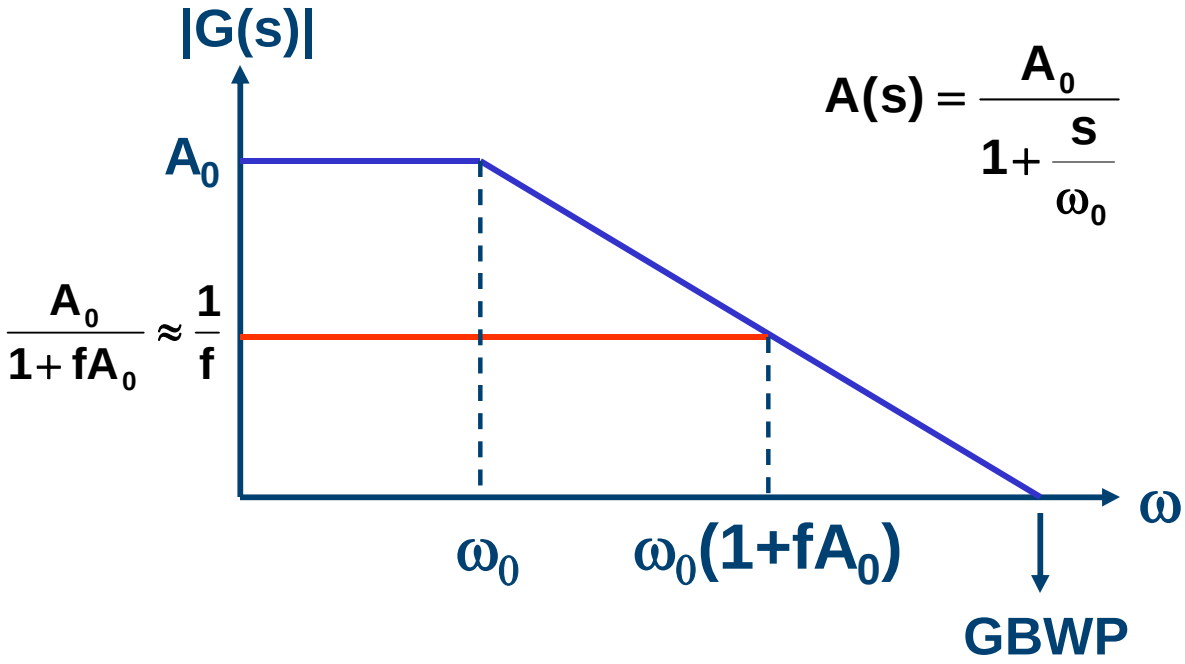
Many interesting properties of the frequency behavior of a given circuit can be obtained plotting the module and the phase of the Transfer Function as a function of the frequency. These plots are called Bode diagrams. In the general case, a transfer function is given by the ratio between two polynomials. The roots of the numerator polynomial are called zeros, the roots of the denominator polynomials are called poles. For example, in the case of a low-pass filter with RC = 1 ms, the Bode diagrams look like:





Bandwidth increase with feedback

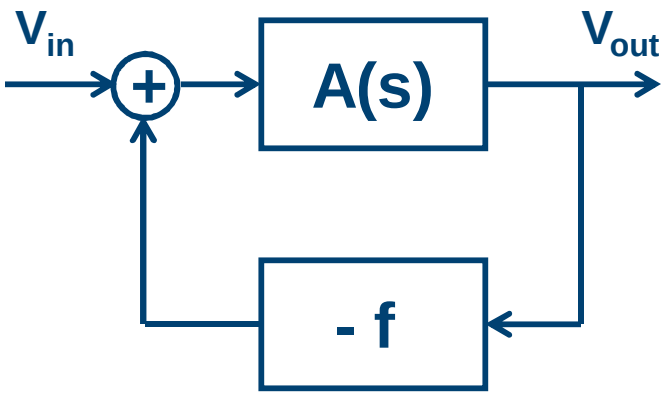




$$G(s) = \frac{A(s)}{1 + f \cdot A(s)} = \frac{\frac{A_0}{1+fA_0}}{1 + \frac{s}{(1+fA_0)\omega_0}}$$

The gain-bandwidth product does not change with feedback!

Stability Criteria



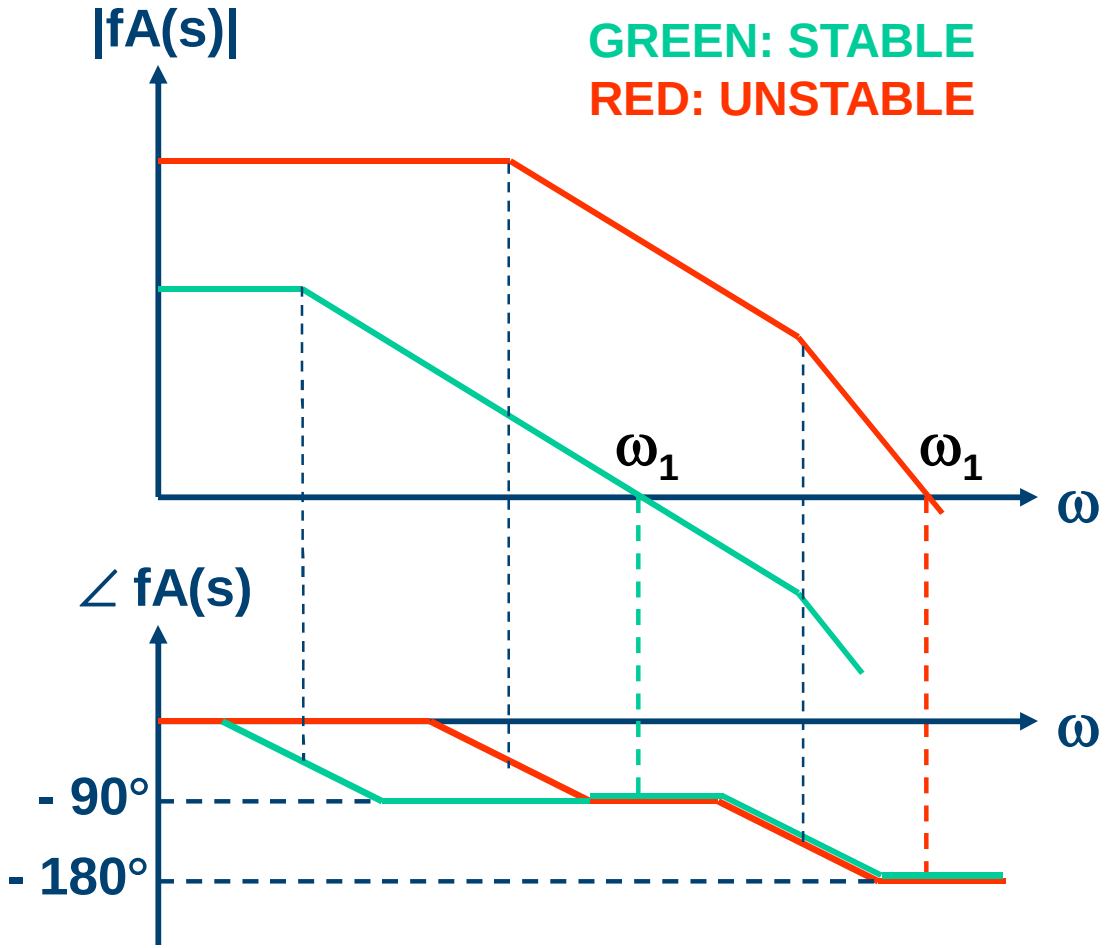
$$G(s) = \frac{A(s)}{1 + f \cdot A(s)}$$

$$1 + f \cdot A(s) = 0$$

Barkhausen's Criteria

$|fA(j\omega_1)| = 1$

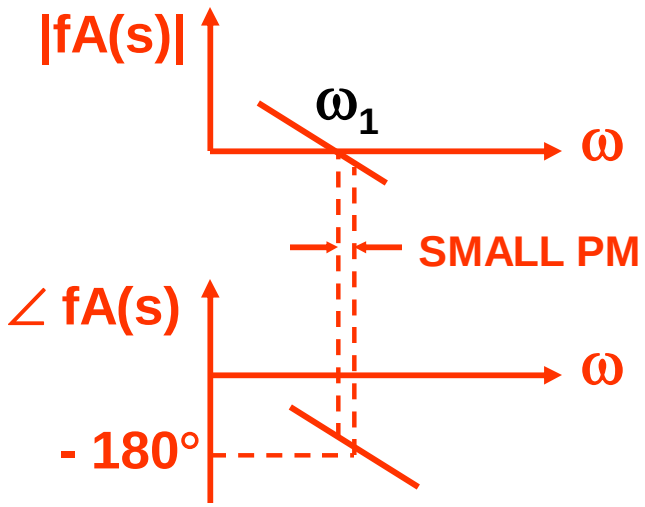
$\angle\, fA(j\omega_1) = -180°$

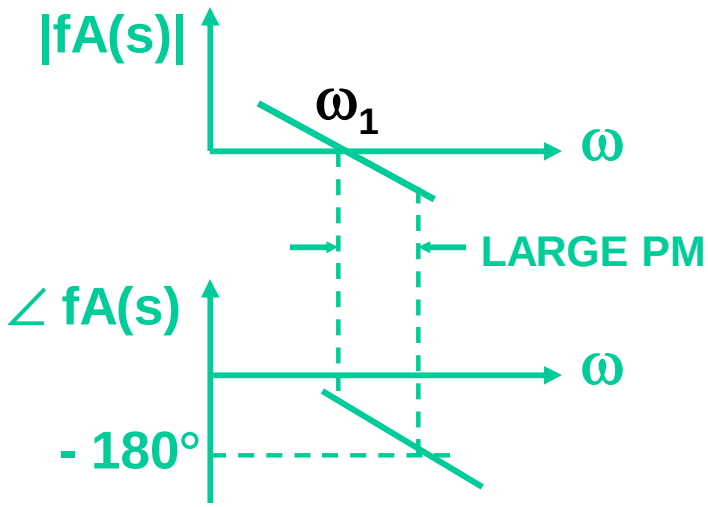


Phase Margin

We have seen that to ensure stability |fA(s)| must be smaller than 1 before ∠ fA(s) reaches - 180°. But, in fact, to avoid oscillation and ringing, we must have a bit more margin.

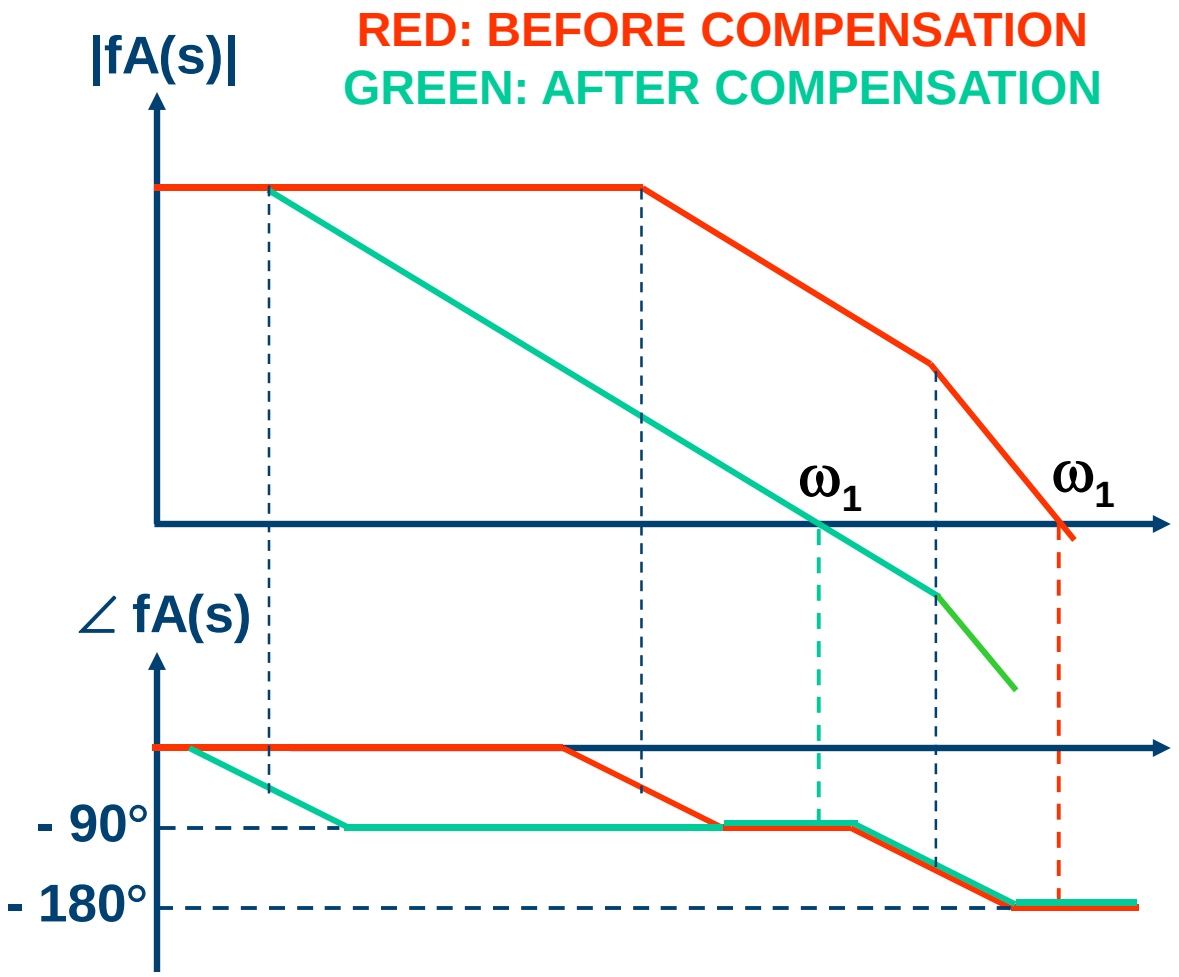
We define phase margin (PM) the quantity 180° + ∠ fA(ω_1), where ω_1 is the gain crossover frequency. It can be shown that, to have a stable system with no ringing (for small signals) we must have PM > 60°. If we want to have an amplifier which responds to a large input step without ringing, PM must be even higher.



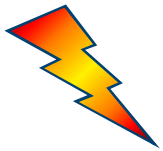


Frequency Compensation

Single-pole op-amps would always be stable (the phase does not go below - 90°). But a typical op-amp circuit always contains several poles (and zeros!). These op-amps can easily be unstable, and they need therefore to be compensated. This is generally done lowering the frequency of the dominant pole.

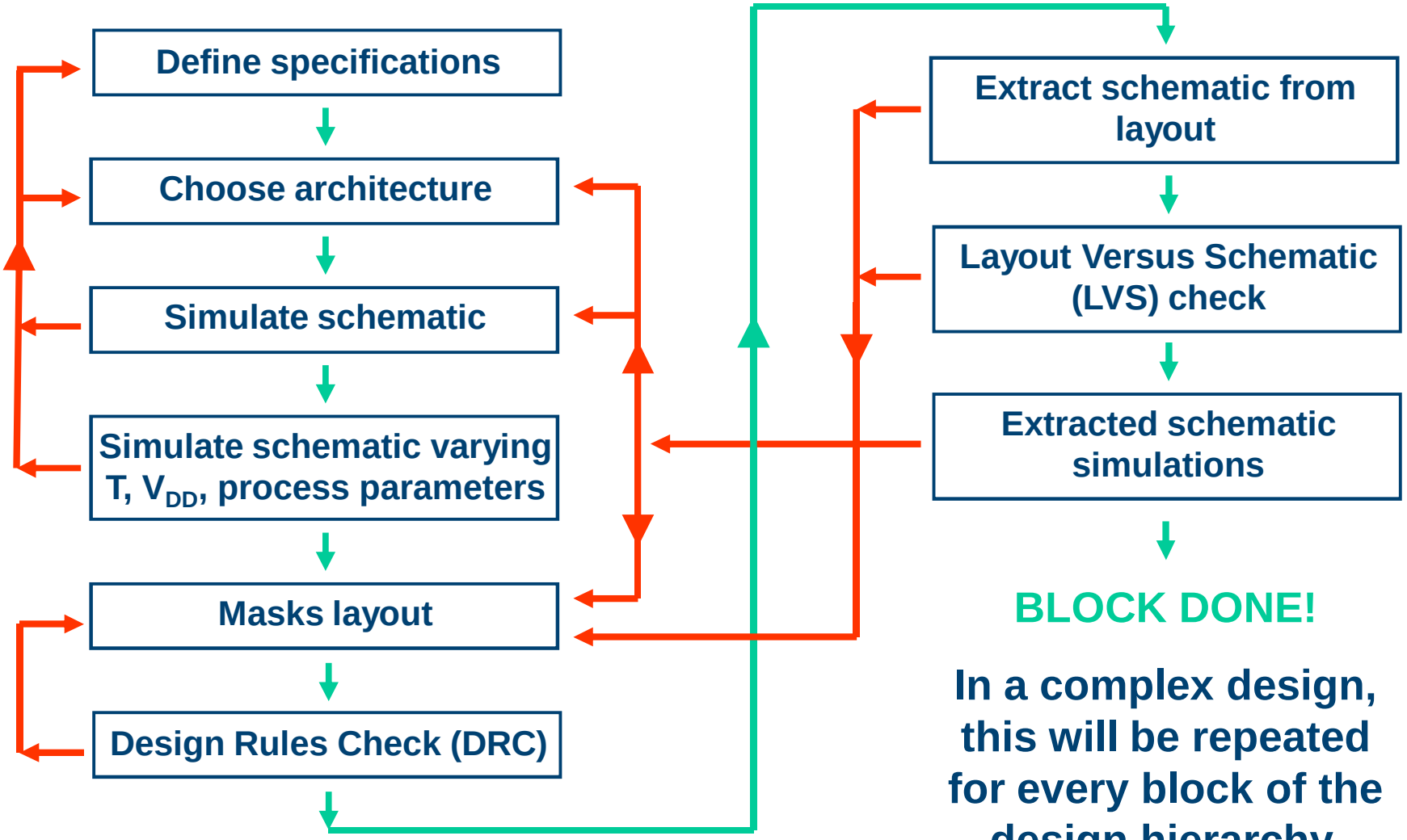


Outline – Part II



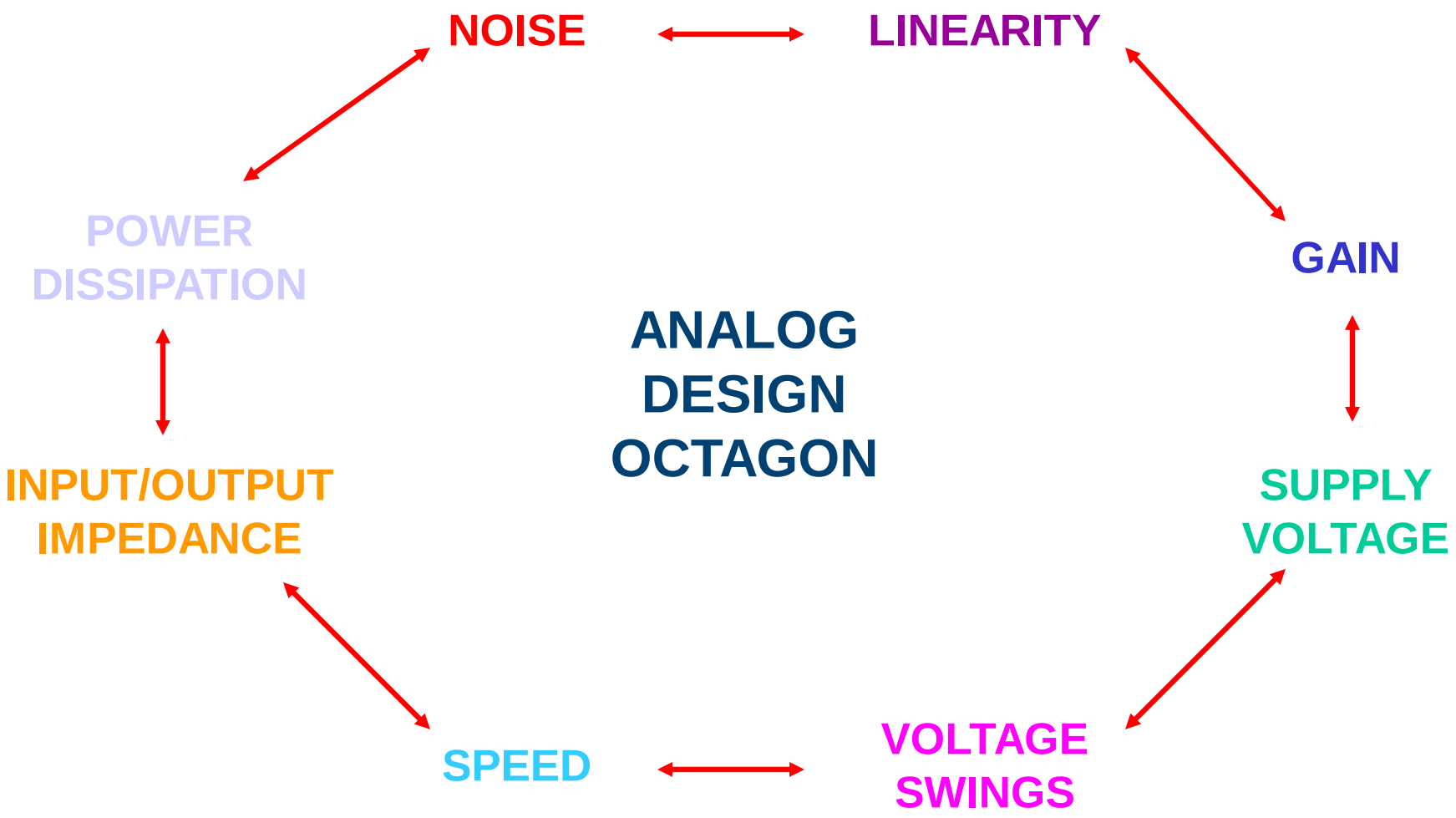
- Noise in analog ICs
- Matching in analog ICs
- Operational Amplifier design examples
- Analog design methodology

Analog design methodology



In a complex design, this will be repeated for every block of the design hierarchy.

Analog design trade-offs



Unit II: **HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS**

Presentation Agenda

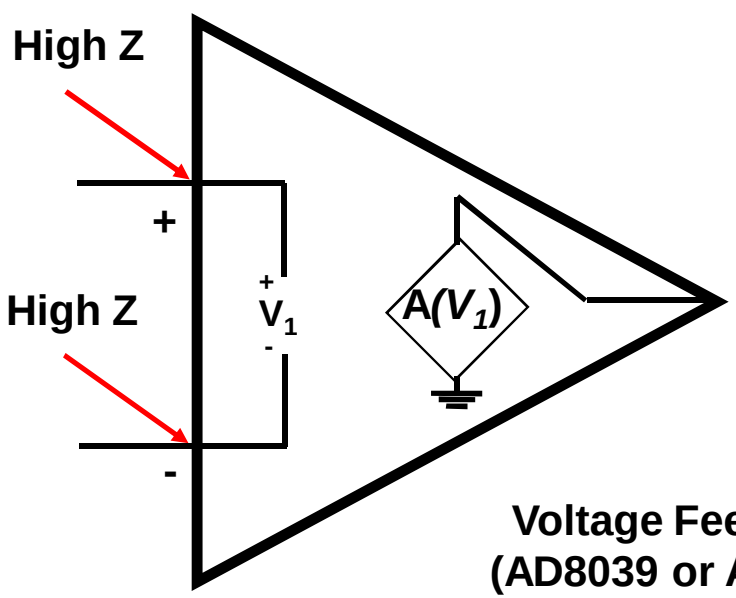
- High-Speed Amplifiers
  - Voltage Feedback vs. Current Feedback
  - Differential Amplifiers
- Precision Amplifiers
  - AutoZero
  - Digitrim
- Instrumentation and Industrial
  - High CMRR
  - VGA

High-Speed Amplifiers

- Voltage Feedback vs. Current Feedback
  - Simplified Architecture
  - Relationship Between Feedback and Bandwidth
  - Stability

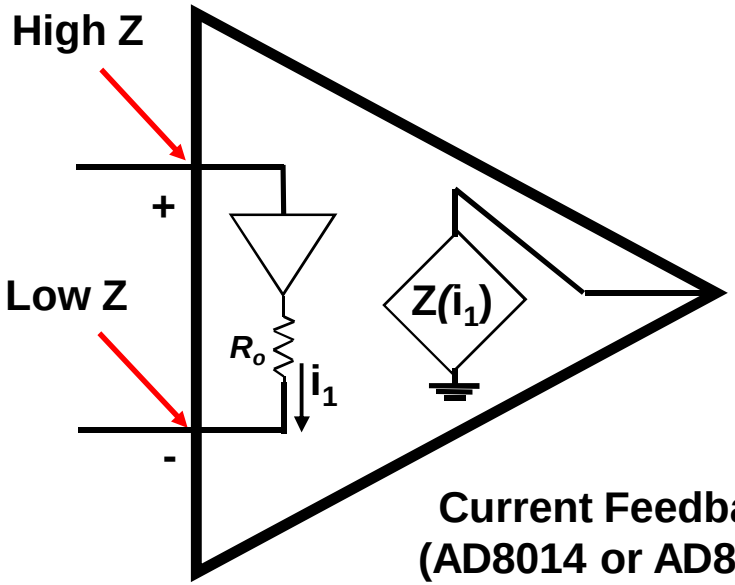
Simplified Block Diagrams

Voltage Feedback vs. Current Feedback



Voltage Feedback
(AD8039 or AD8092)

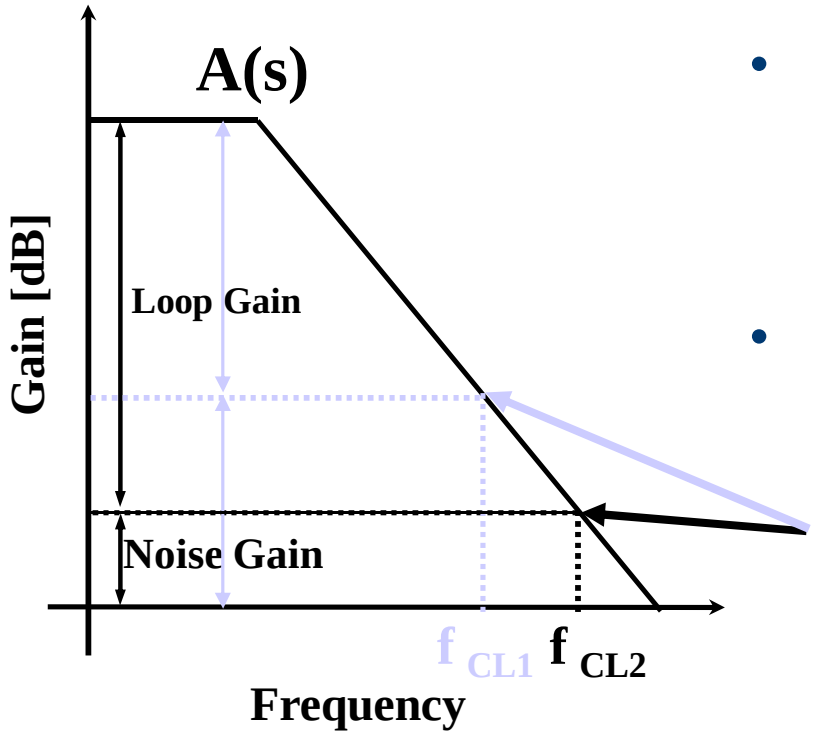
- Error Voltage (V_1) Amplified by the Open loop Gain (A)
- Closed Loop forces Error Voltage to be zero



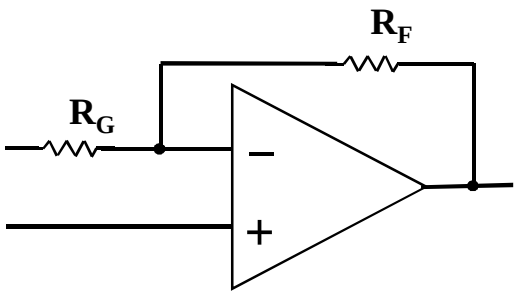
Current Feedback
(AD8014 or AD8007)

- Error Current (i_1) Amplified by the Transimpedance Gain (Z)
- Closed Loop forces the Error Current to be zero making the Input Voltages equal

Voltage Feedback Frequency Response



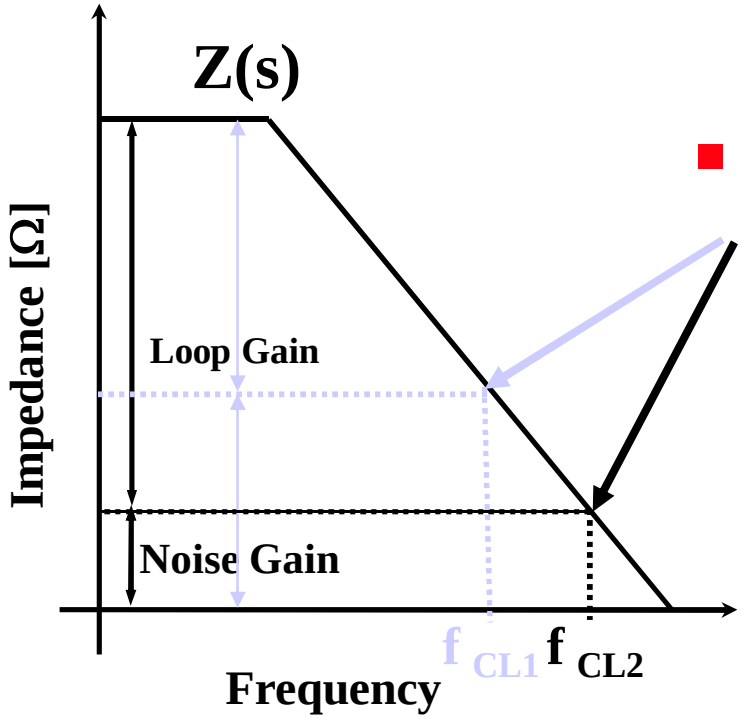
- Ideally Gain Bandwidth Product is constant
  - GBWP is more accurate for Higher Gains
  - GBWP is less accurate at Lower Gains due to peaking in the AC response
- Intersection of Noise Gain and Open loop gain is the bandwidth of closed loop amplifier



$$\text{Noise Gain} = 1 + \frac{R_F}{R_G}$$

$$\text{Loop Gain} = \frac{A(S)}{1 + \frac{R_F}{R_G}}$$

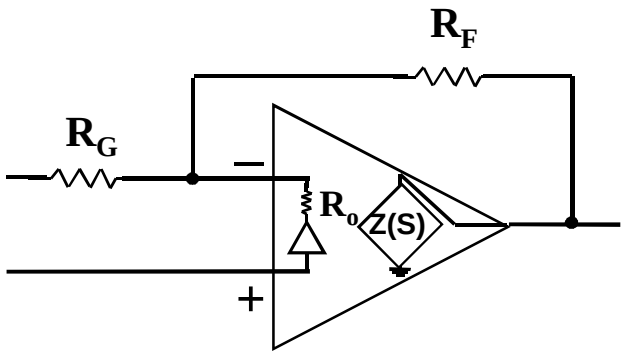
Current Feedback Frequency Response



- **Intersection of Noise Gain and Open loop gain is the bandwidth of closed loop amplifier**
  - **Bandwidth is determined by the feedback network (R_F and R_O)**
    - **R_O is typically between 20 and 40Ω**

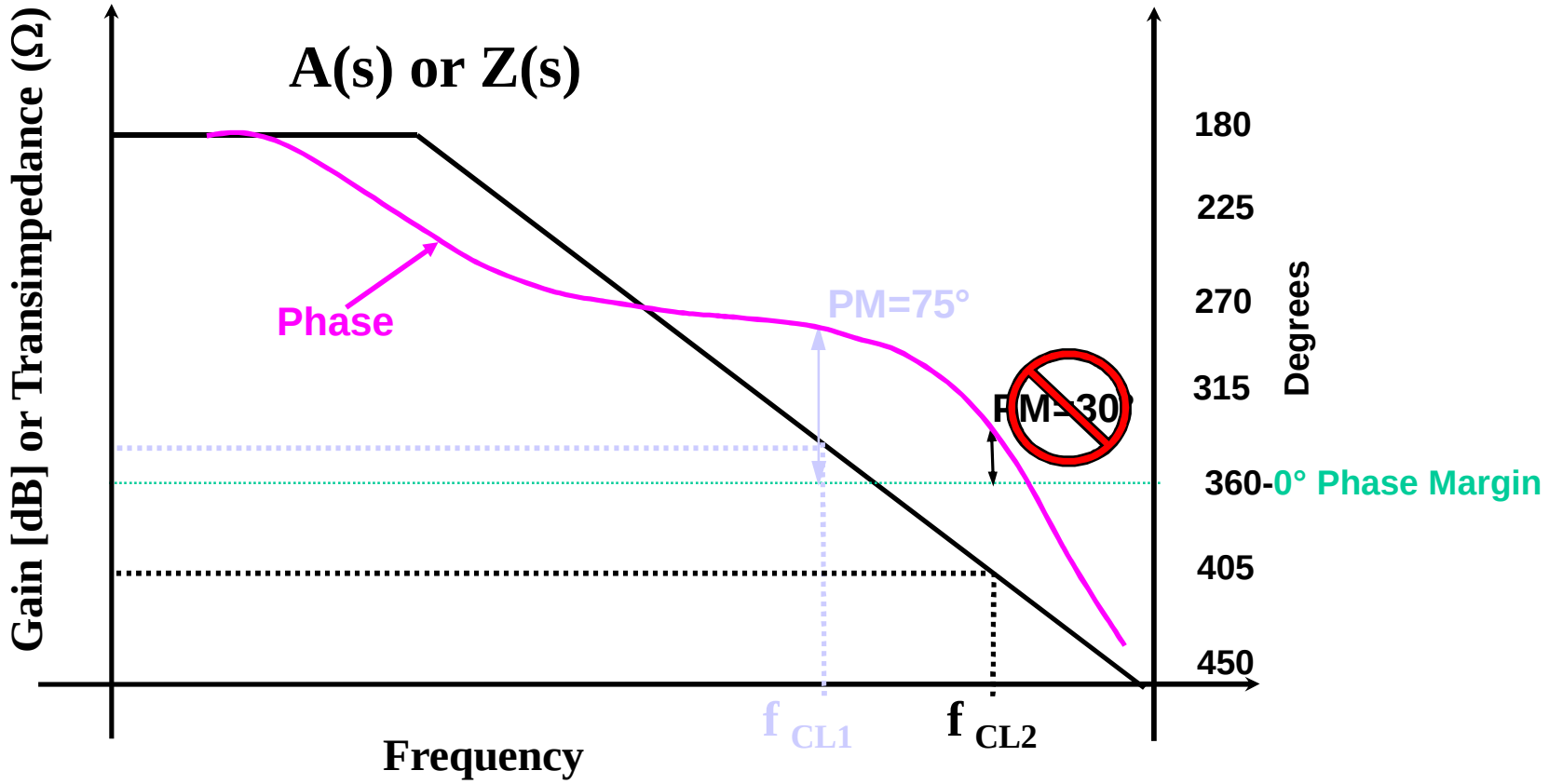
$$\text{Noise Gain} = 1 + \frac{R_F}{R_G}$$

$$\text{Loop Gain} = \frac{Z(s)}{R_F + R_O(1 + \frac{R_F}{R_G})}$$



Stability Analysis

Same for Voltage and Current Feedback



- Adjust Gain for phase margin > 45° for optimal operation
- < 30° is unsafe

Differential Amplifiers

- Benefits of Differential Amplifiers
- Architectures of Differential Amplifiers
- Applications of Differential Amplifiers

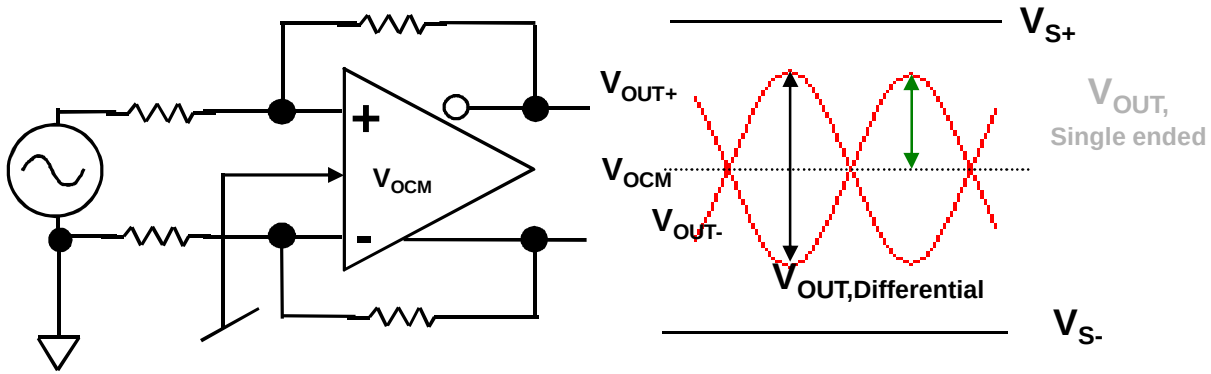
Primary Uses for Differential Amps

- Differential Signal Processing
  - Avoid Ground Noise
  - High Dynamic Range on Low Supplies
  - Differential Filters
- High Speed ADC Driving
  - All High Speed ADC Perform Better when Driven Differentially
  - Amplify and Buffer DAC outputs
  - Differential Amplifiers Reduce Clock Jitter
- Twisted-pair Line Driving/Receiving
  - Simplifies circuit design
  - Balanced Outputs Minimize EMI
  - High CMRR Reduces EMI Susceptibility

Benefits of Differential Signal Processing

- Maximize Speed and Resolution with Differential Amps
  - Avoid Grounding/Return Noise Problems
  - Analog Signals in High-performance Systems Start and End Differential
    - Almost Always the Signal Source from the Real World is Differential
    - High-speed ADCs Have Differential Inputs
  - Better Distortion/Dynamic Range than Single-Ended Op-Amps
    - More Output Headroom for the same Signal Amplitude
    - Or Lower Distortion for the same output swing especially the 2nds

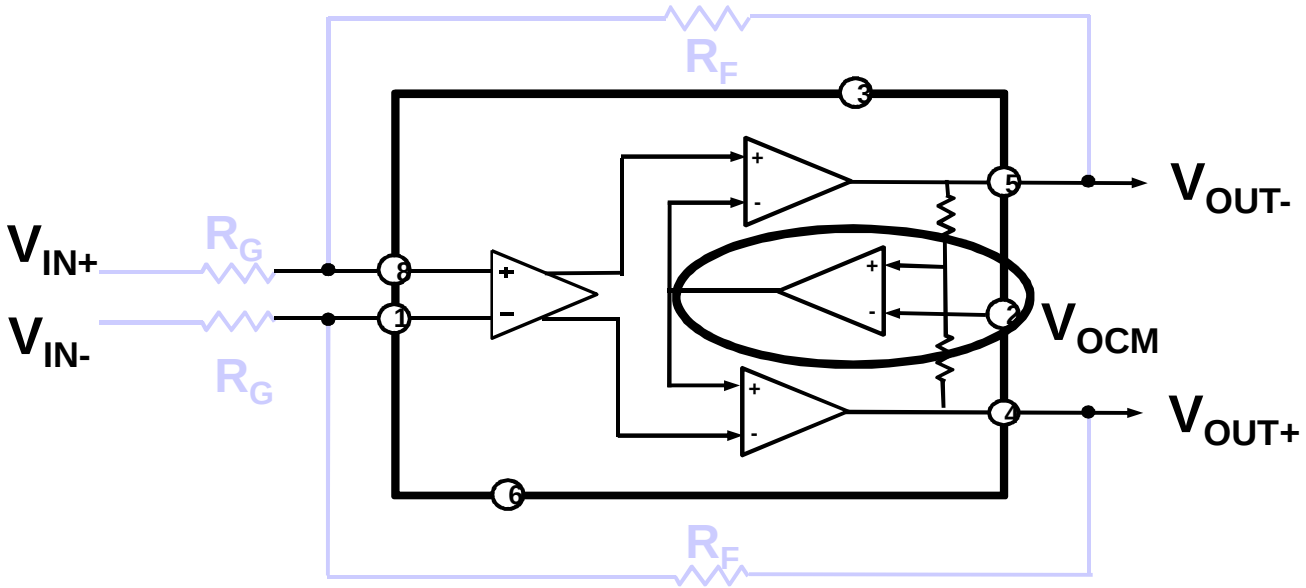
High Speed Differential Amps for Challenging Designs



- **3 Main Signal Characteristics of Differential Signals**
  - **Equal in amplitude, and opposite in phase**
  - **Differential Amplitude = 2x either Single Ended output**
  - **Centered at common voltage, V_{OCM}**

What's Inside the Analog Devices Differential Amplifiers?

- **Internal CM Feedback forces Forces both outputs to be balanced**
  - **Equal in amplitude 180° out of phase: $V_{OUT, CM} = (V_{OUT+} + V_{OUT-})/2$)**
    - **Balance is unaffected by R_F/R_G matching**
- **Differential feedback effectively creates 2 summing nodes**
  - **Forces Both Inputs to the same voltage when the loop is closed**
    - **High Input Z, Low Output Z**

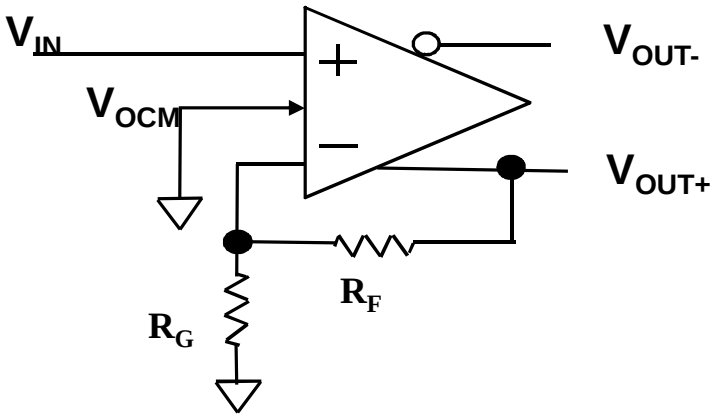


More About the V_{OCM} Pin

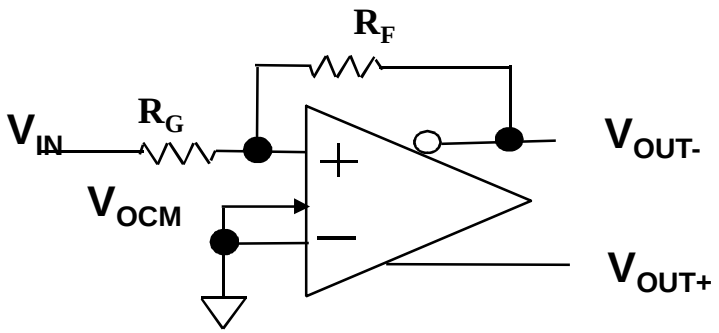
- V_{OCM} Pin
  - Creates Best Available Balance @ High Frequencies
    - By Forcing Outputs to be equal
  - For AC signals and DC Reference Voltages
  - For Easy Level Shifting
    - From Ground Referenced Signals (+/-5V supplies) to Single +5V Supply Signals

Understanding How They Work w/ Alternate Circuit Configurations

Like Non-inverting Op Amp



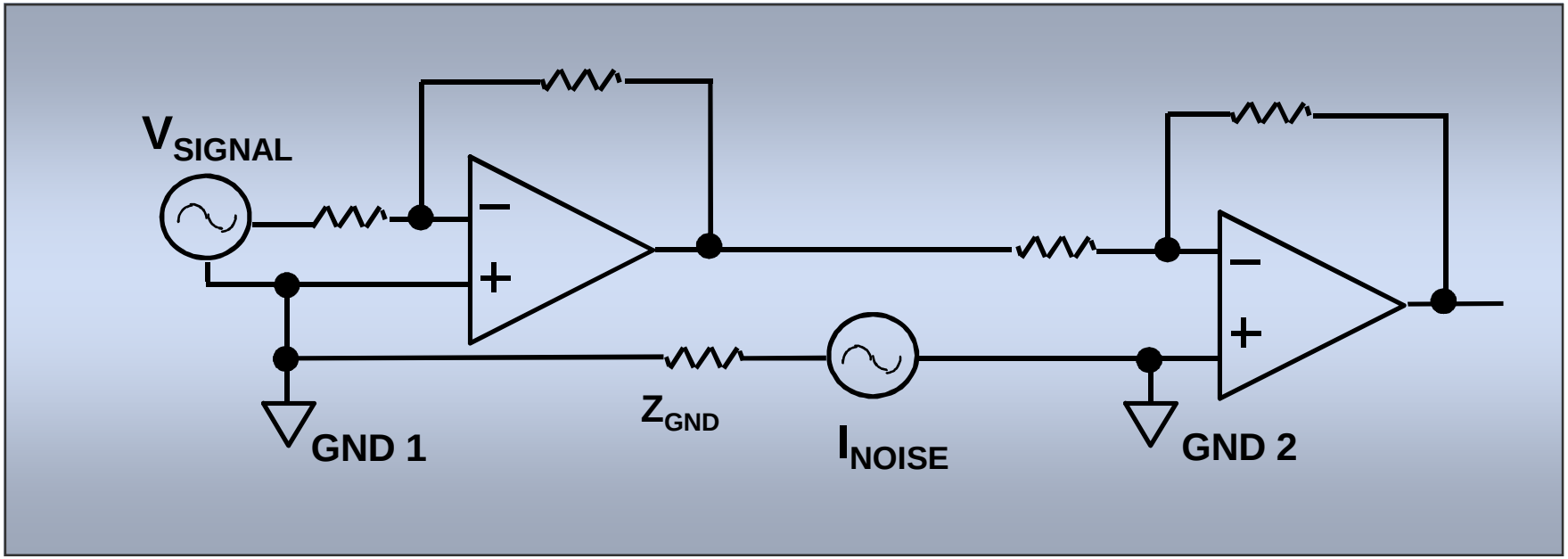
Like Inverting Op Amp



- **2 Feedback Loops**
  - **Differential feedback forces inputs to the same voltage**
  - **Common mode Feedback forces $V_{OUT-} = -V_{OUT+-}$**
- **Non-inverting example:**
  - **For $R_F = 0$**
    - **$V_{Out+} = V_{IN}$**
    - **Gain = 2**
- **Inverting example:**
  - **For $R_F = R_G$**
  - **High input Z summing node**
    - **$V_{out-} = -V_{IN}$**
    - **Gain = 2**

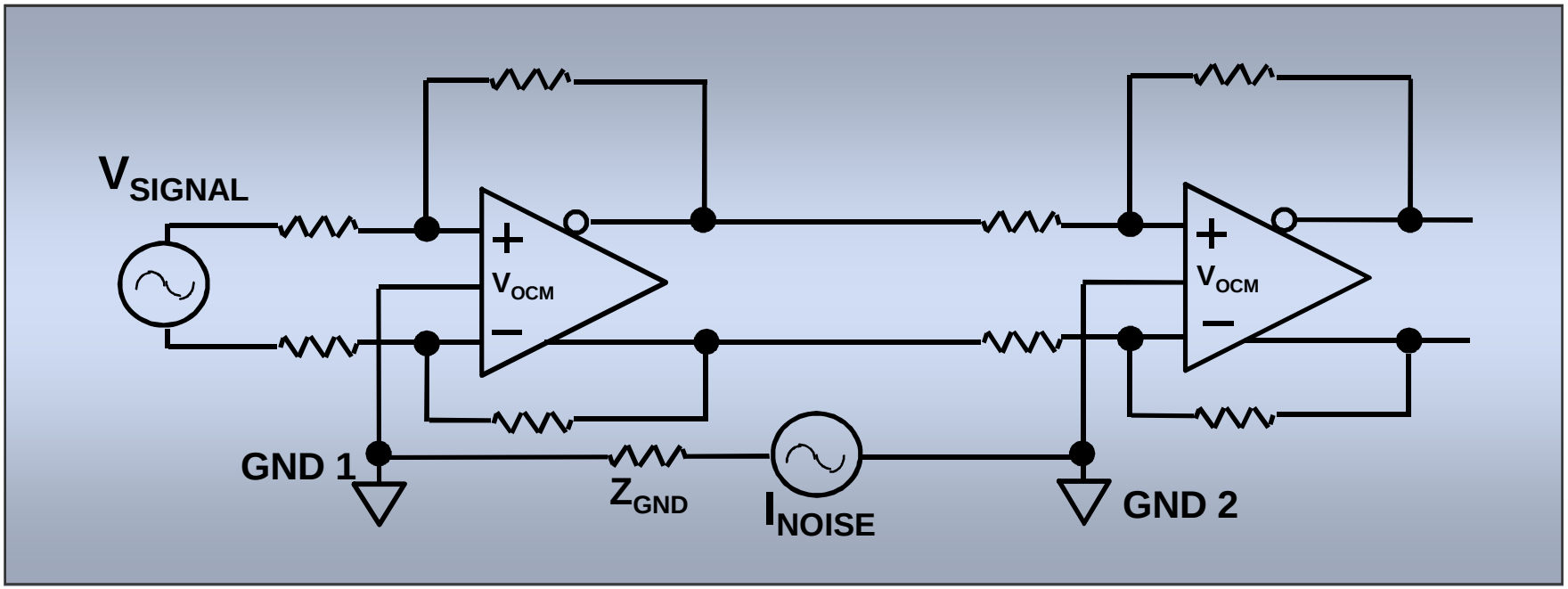
Single-ended Components Cannot Reject Ground Noise

- Each Part of the Circuit Has a Different Reference Point
- High Frequency Ground Currents will Cause Problems
- Op Amp Can not Reject This Ground Noise

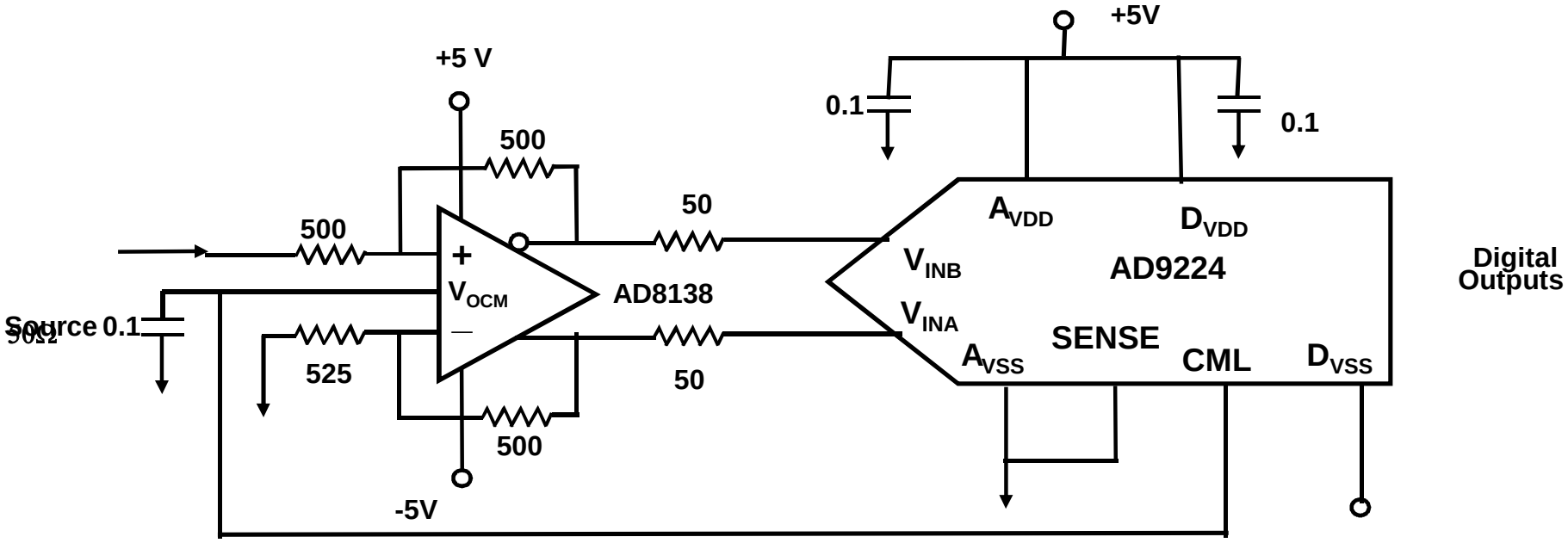


Differential Amps Have Effective CMRR

- Differential Signal does not Need a Reference
- Ground and Other Noise Sources are Common to Both Inputs
  - ➢ CMRR of Differential Amp is Effective

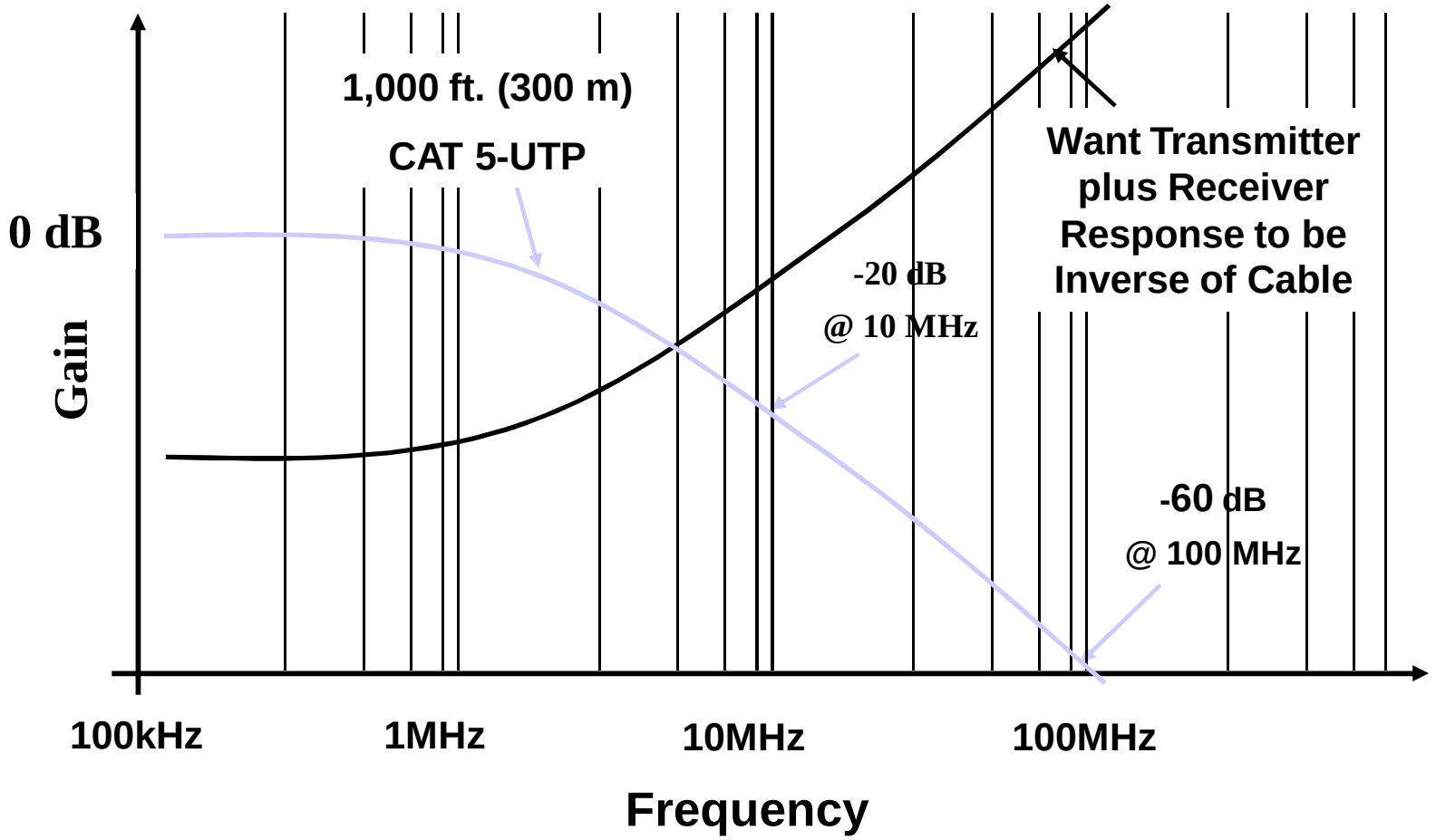


Driving High-Performance ADC on 5V Supply

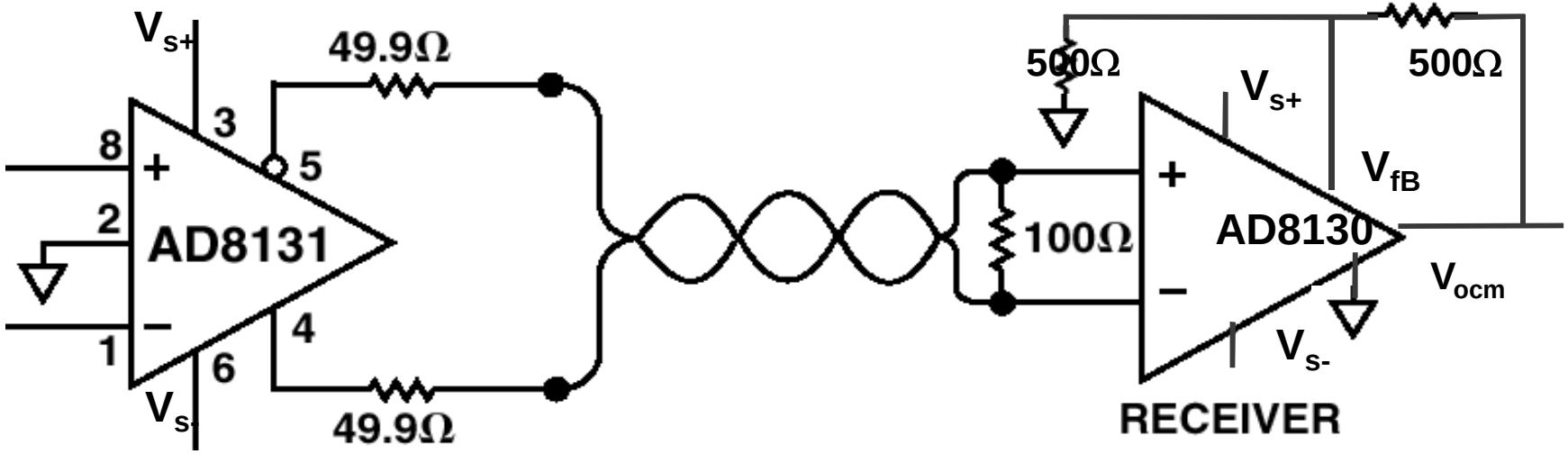


- ADC Reference CML output drives V_{OCM} to set optimum CM output
  - Easy level shift using V_{OCM}
  - Better Distortion in signal chain for +/-5V, than +5V
  - Connect to the ADC reference or any other reference voltage

Cable Driving Challenge



Differential Driver and Receiver



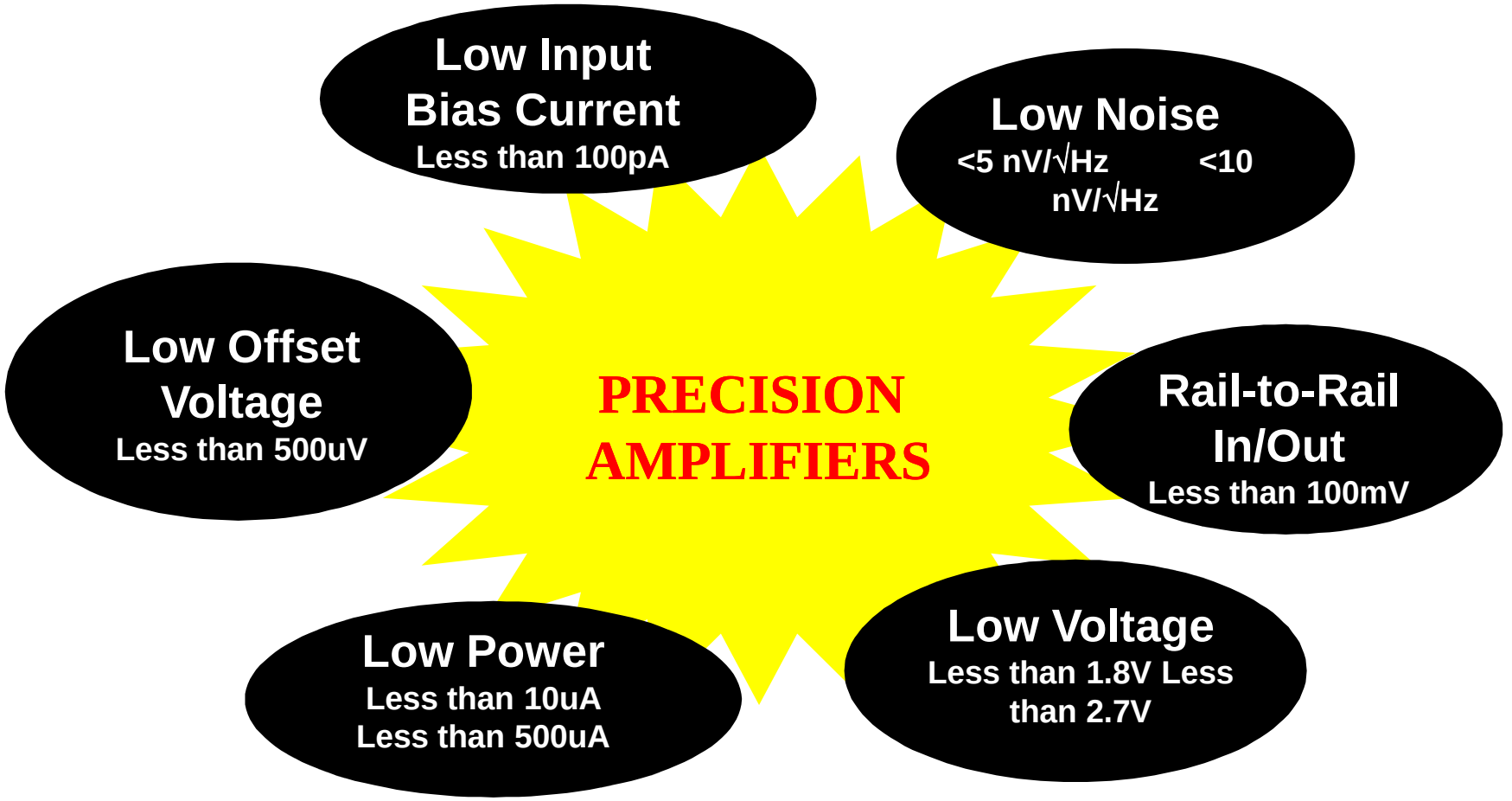
- Balanced Driver Minimizes EMI Generation
- High CMRR Receiver Minimizes EMI Pick-up

Precision Amplifiers

- Auto-Zero

Precision Amplifier Segments...

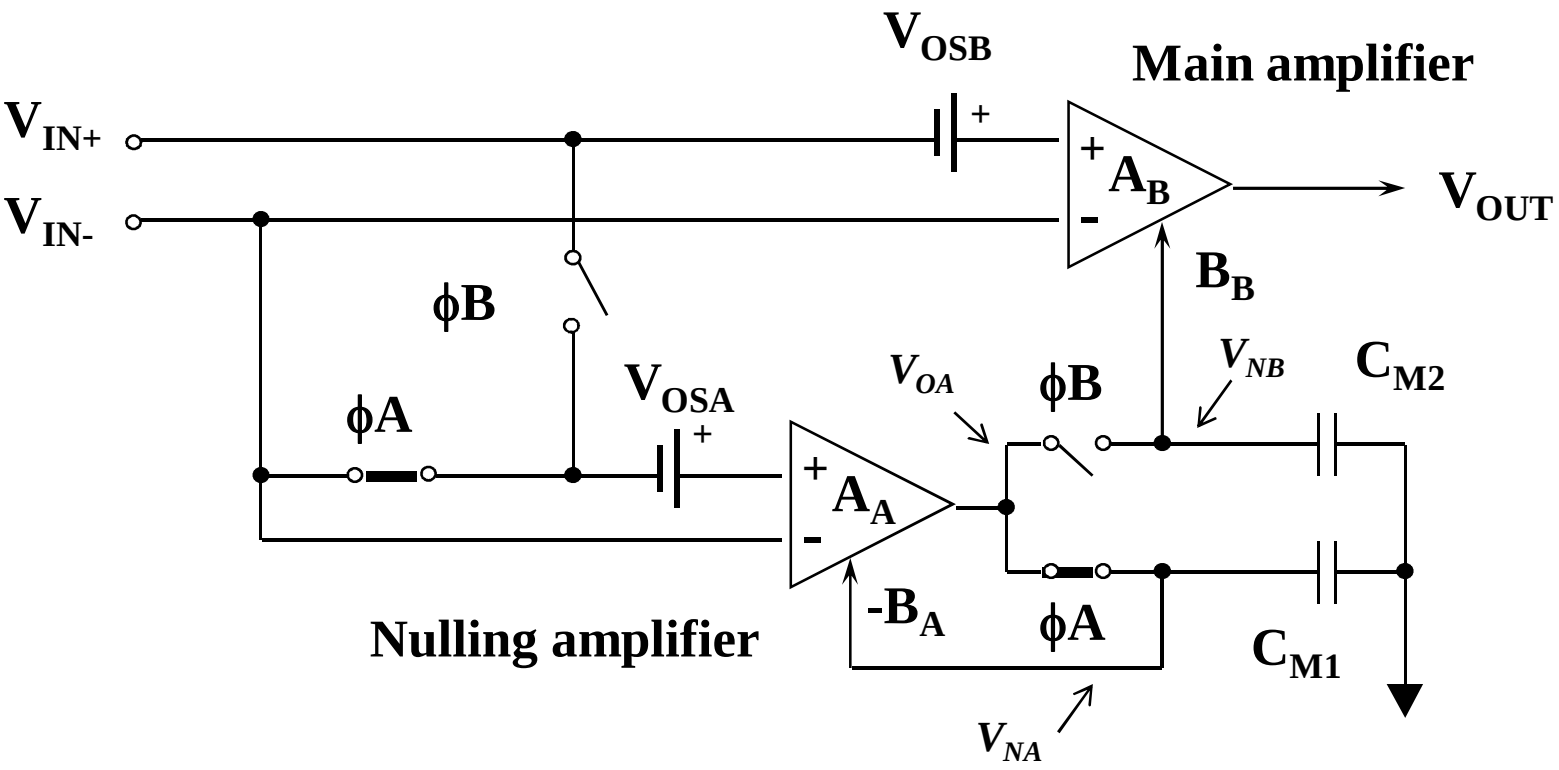
Amplifier Characteristics Define Market



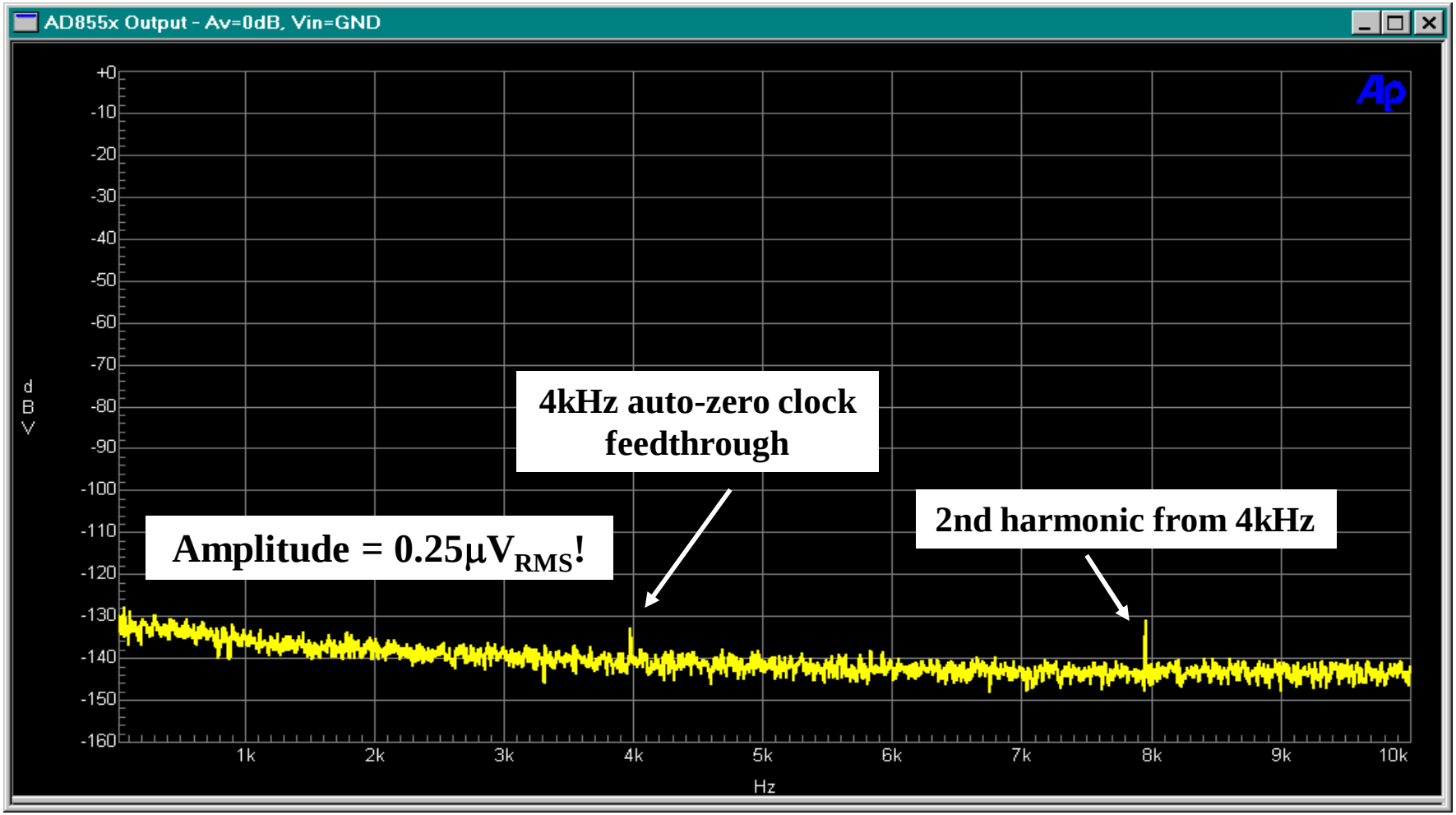
AutoZero Amplifiers: AD855x,AD857x families & AD8628

- 1μV of typical offset voltage (5μV max.)
- 5 nV/°C of TCV_{OS} from -40°C to +85°C
  - That's less than 600 nV of drift over the entire temp. range
- CMRR and PSRR are offset voltages due to changes in V_{CM} and V_{SY}
  - CMRR and PSRR are >135dB (or <0.3ppm)
- 1/f noise, which increases at 3dB per octave decrease, can also be viewed as an offset error
  - The AD855x, AD857x and AD8628 exhibit NO 1/f noise!

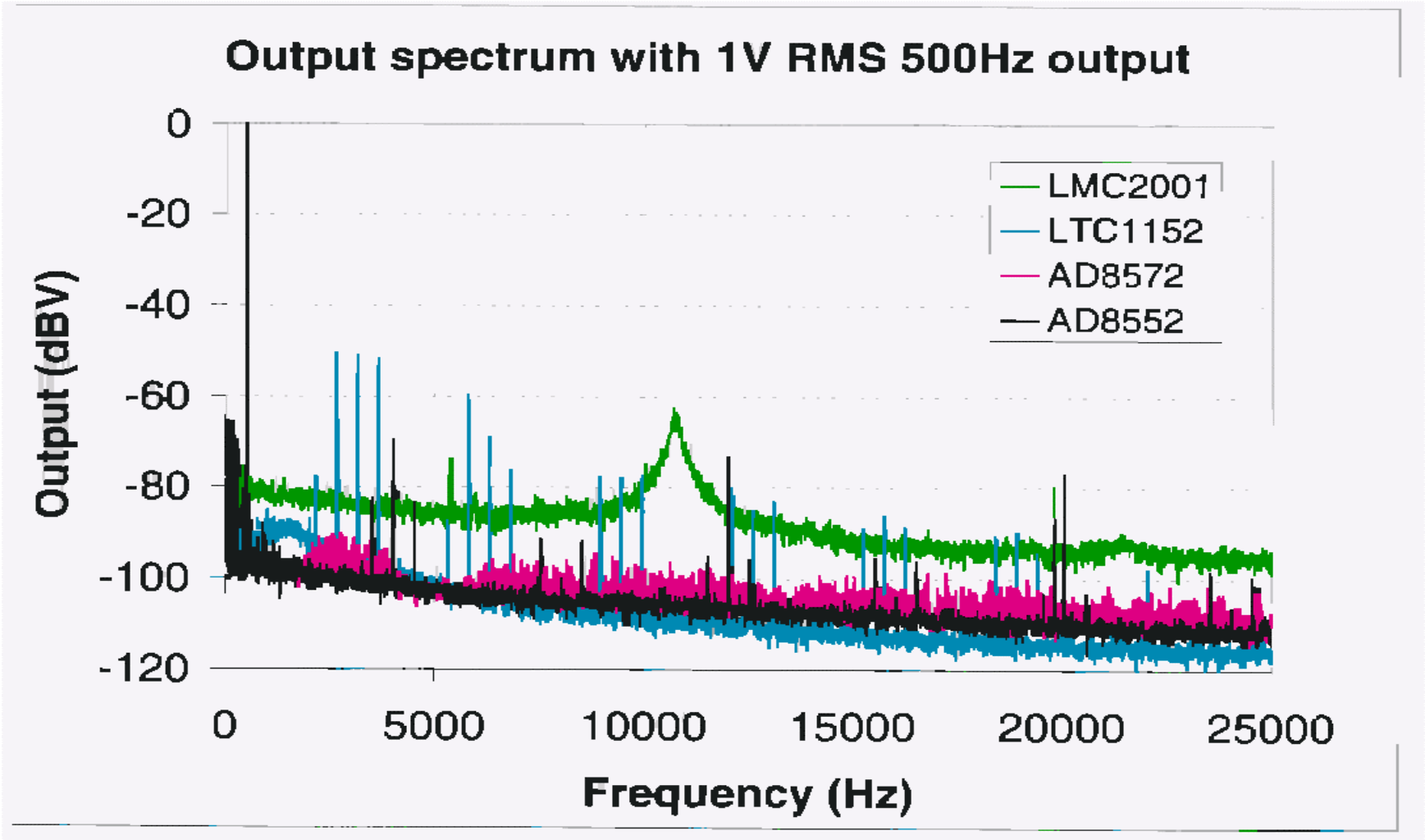
Simplified Schematic of AD855x



Spectral analysis of AD855x output in unity gain



IMD+Noise Comparison



2nd Generation Auto-zero amp

AD8628

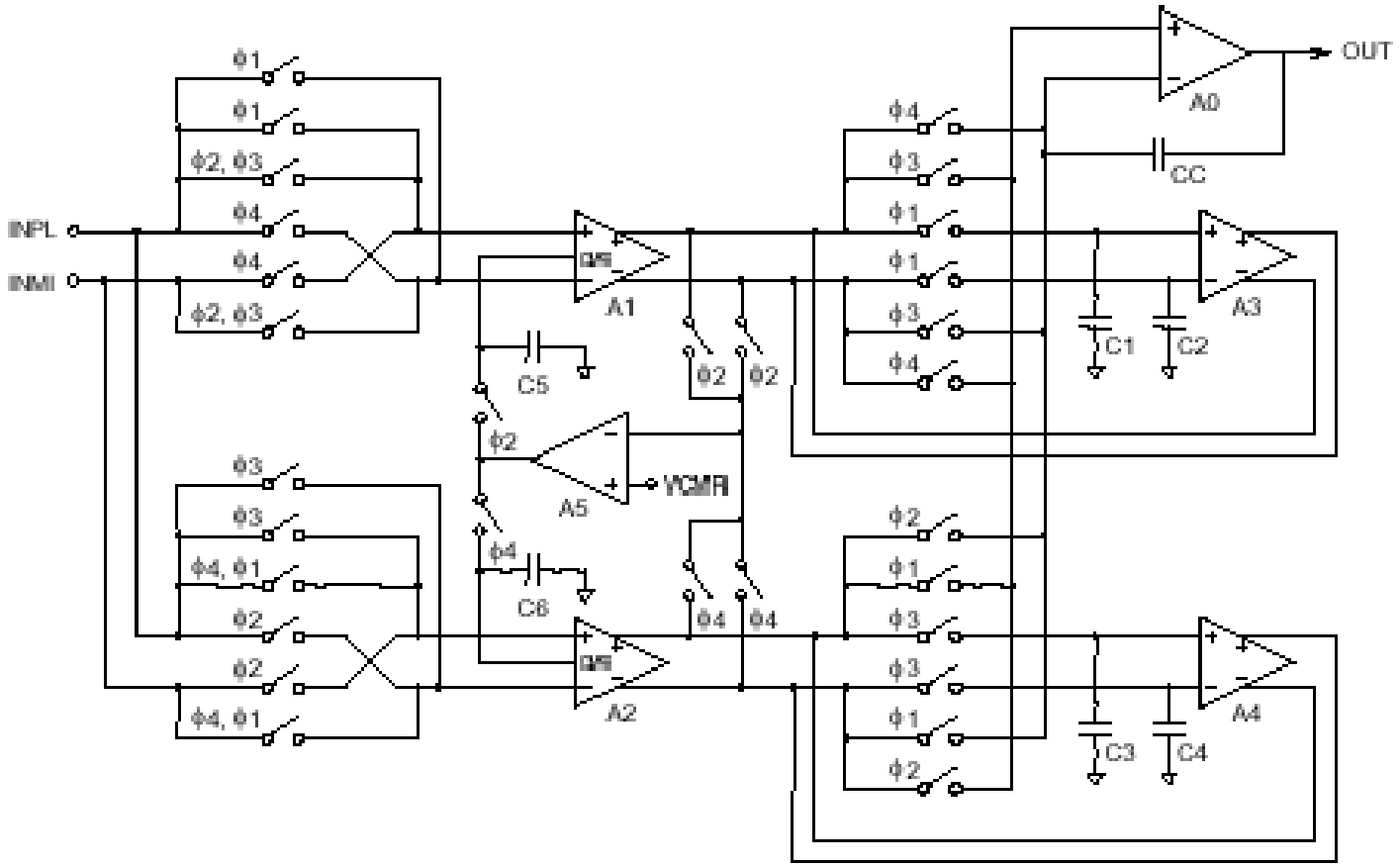
World's Highest Precision Amplifier

- ***SOT-23 package !!!***
- ***Best noise ever for auto-zero*****--20nV/√Hz**
  - Like non-auto-zero amplifiers
- **Low Clock noise**
- **2.2MHz Gain-Bandwidth**
- No Compromise in auto-zero DC precision
- *16 bits absolute accuracy*: **0-10kHz—including noise**

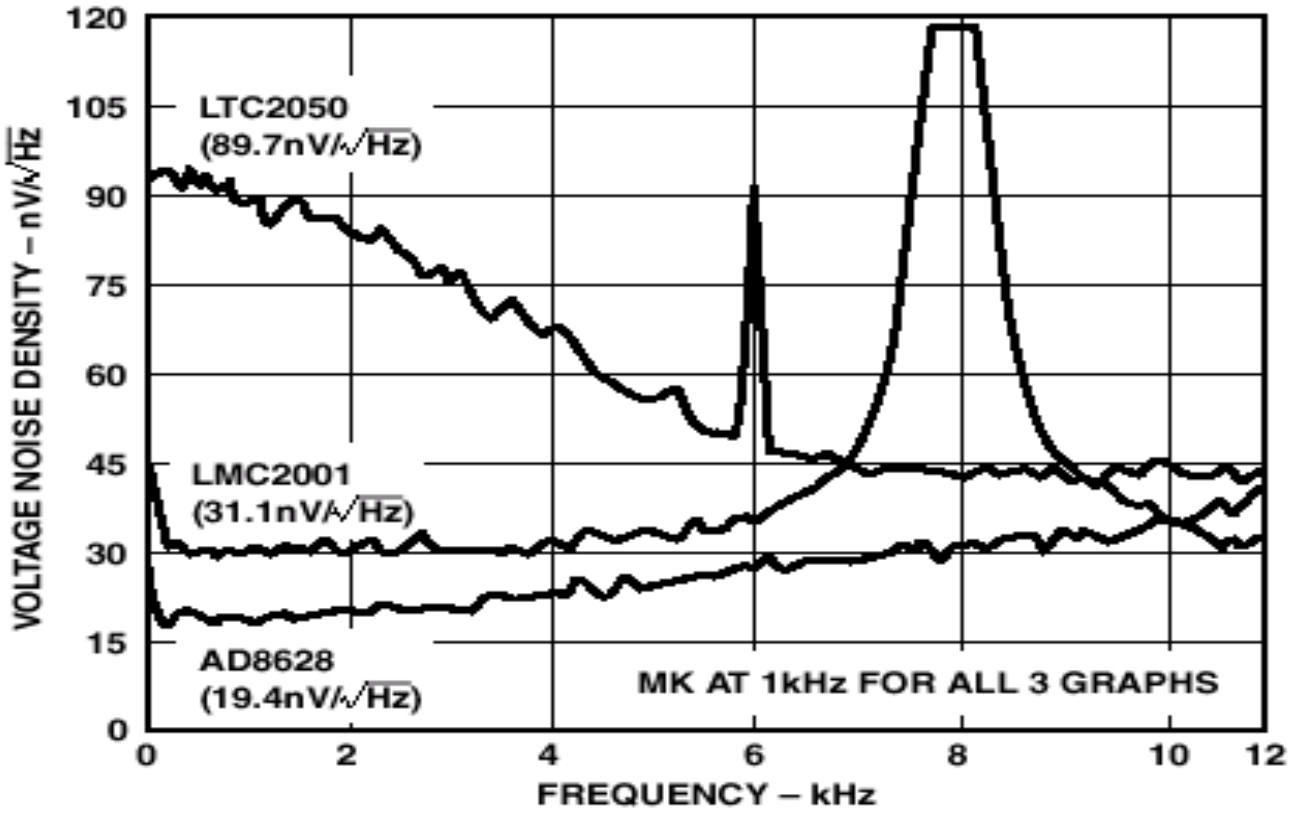
Photodiodes, Portable scales, current sensors, IR sensors, strain br mote sensors

Release in April 2002

“Simplified” diagram of AD8628 amplifier



AD8628 Noise Spectral Density Comparison



Precision Amplifiers

- Digitrim

DigiTrim Amplifiers

- Digitrim is a proprietary technology used to digitally adjust an in-package IC without adding any extra digital input pins
- On the AD8601/2/4 family, DigiTrim adjusts offset voltage to <500μV
- On the AD8603/7/9 family, DigiTrim adjusts offset voltage to <100μV
- On the AD8605/6/8 family, DigiTrim adjusts offset voltage to <65μV

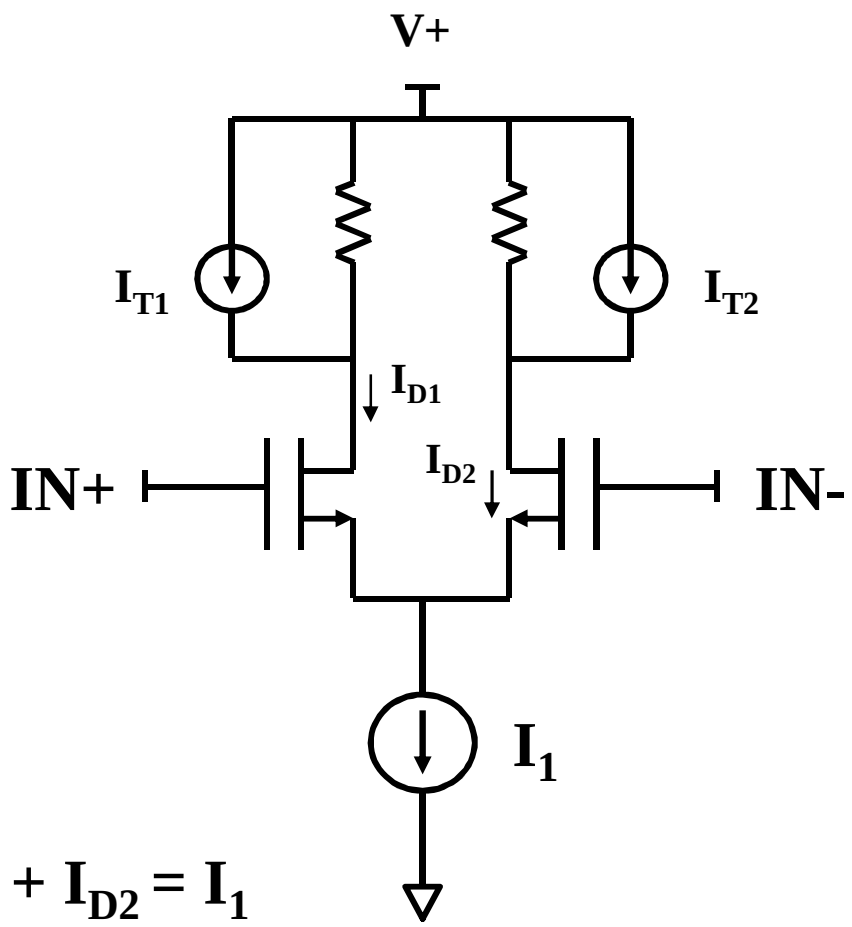
Advantages of DigiTrim®

- In-package trim
- Mechanical stress on the die causes V_{OS} errors
  - This can ruin any wafer trimming already done
  - **Lots** of stress on SOT23 and SC70 packages
- By trimming in-package you trim out post-stress V_{OS}!
- No special processing - Foundry OK
- As processing shrinks, trim area is smaller too
- No extra pads required
- Higher test throughput

All this adds up to LOWER COST

How is V_{OS} trimmed?

- Extra current is put into one side (or the other) of the input diff pair
- This current difference creates an offset voltage between the diff pair transistors



$$I_{D1} + I_{D2} = I_1$$

I_{T1} or I_{T2} is adjusted to minimize V_{OS}

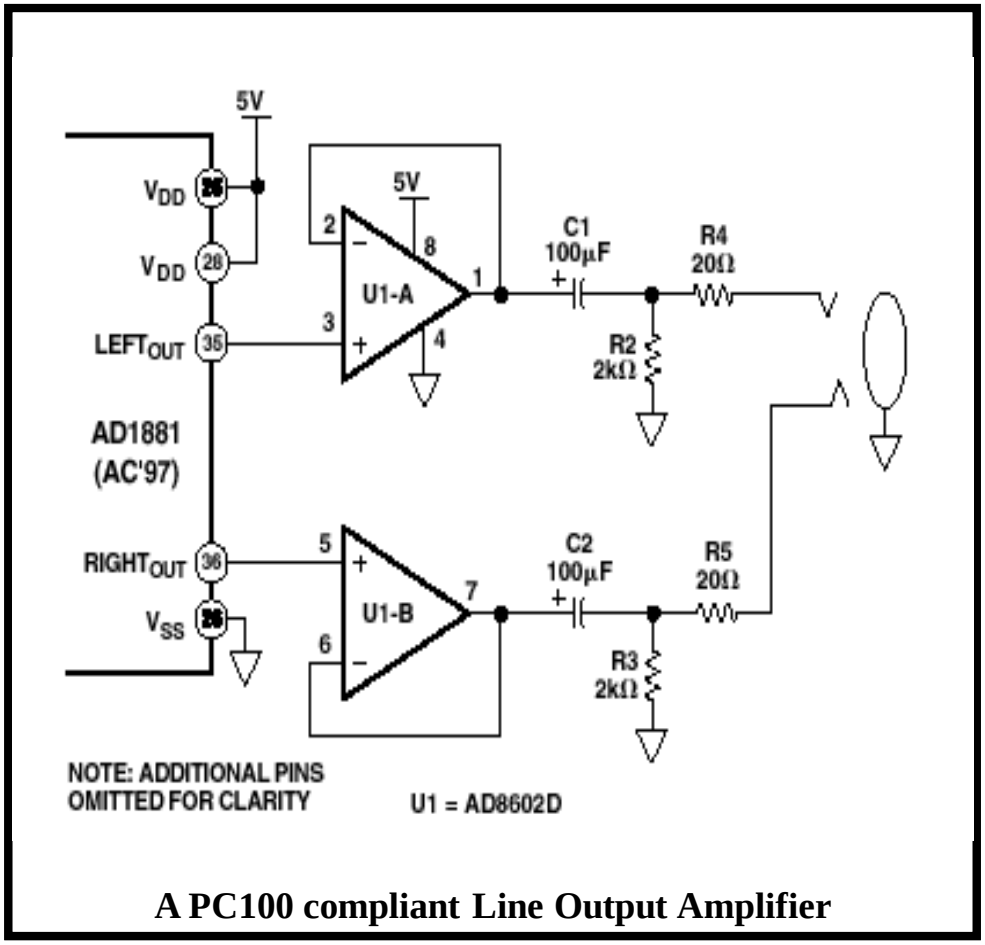
Some Trim Comparisons

	Trimmed at:	**Special Processing**	**Resolution**
Laser	Wafer	Thin Film	Continuous
Zener Zap	Wafer	None	Discrete
Link	Wafer	TFR or Poly	Discrete
EEPROM	Wafer or FT	EEPROM	Discrete
Chopper	N/A	CMOS	Continuous
DigiTrim	Wafer or FT	None	Discrete

AD8601/2/4 DigiTrim® Amplifiers

- V_{OS} - < 500μV
- Bandwidth - 8MHz
- Input Bias Current - <60pA max. (<1pA typ)
- $\Delta V_{OS}/\Delta T$ - 2μV/°C typ
- Supply Current - 840μA/amplifier
- SOT23 package (single)

10X Better than Standard CMOS!!



A PC100 compliant Line Output Amplifier

Next Generation DigiTrim®

- **AD8605/6/8 Low noise DigiTrim ®**
  - ***Low noise—8*nV/√Hz**
  - ***Low offset*--65μV max!**
  - **Very low input bias current– 1pA max!**
  - **Fast--10MHz bandwidth**
  - **High CMRR, PSRR and Gain**
  - **Single in SOT23 and Wafer Level Chip-scale!**
- **AD8603/7/9 Low power/low noise DigiTrim ®**
  - ***Low Power*--60μA per amplifier**
  - ***Low offset*--<100μV max**
  - ***Low noise*--30nV/√Hz**
  - **350kHz bandwidth**
  - **1.8V to 5V operation**

Low Noise CMOS

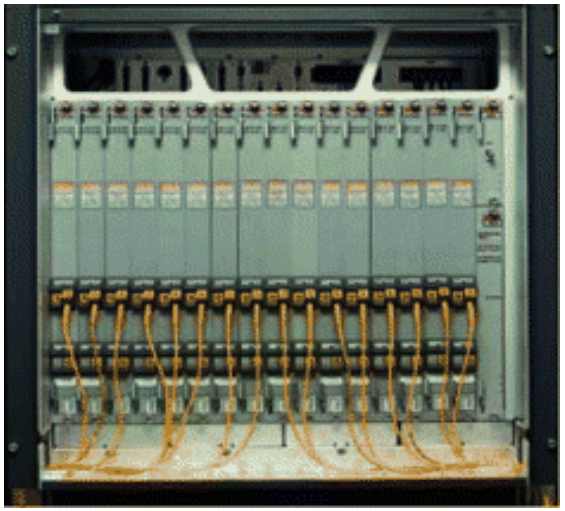
Release in April

High Precision Low Power

Photodiodes, Portable scales, current sensors, strain bridges (pressure), remote sensors

Top Core Applications

- Photo-diode amp
- Thermal sensing
  - Infrared
  - Thermocouples
  - RTD
- Current sensing
  - Motor controls
  - Laser Diode Power Controls
  - Battery Controls
- Strain Bridges
- Level setting and detecting
- Integrator



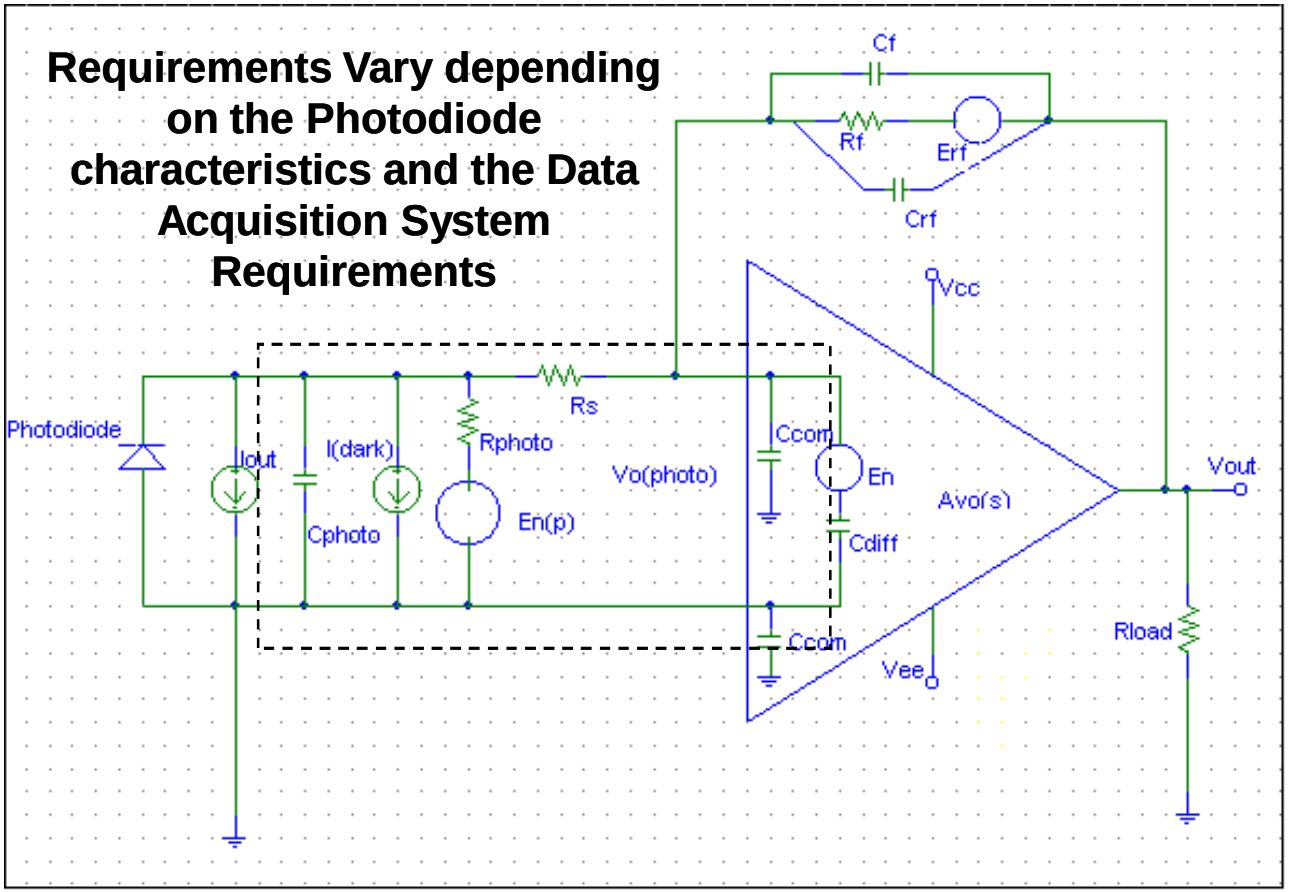
Photodiode trans-impedance amplifier

Key Requirements
Low input bias current
Low Offset Voltage
Low Drift
Low Cin
Bandwidth (Varies)
Wide Dynamic Range

Key Parts

CMOS AD855X
AD857X
AD8601/2/4
AD8605/6/8
AD8628 AD8651

Requirements Vary depending on the Photodiode characteristics and the Data Acquisition System Requirements

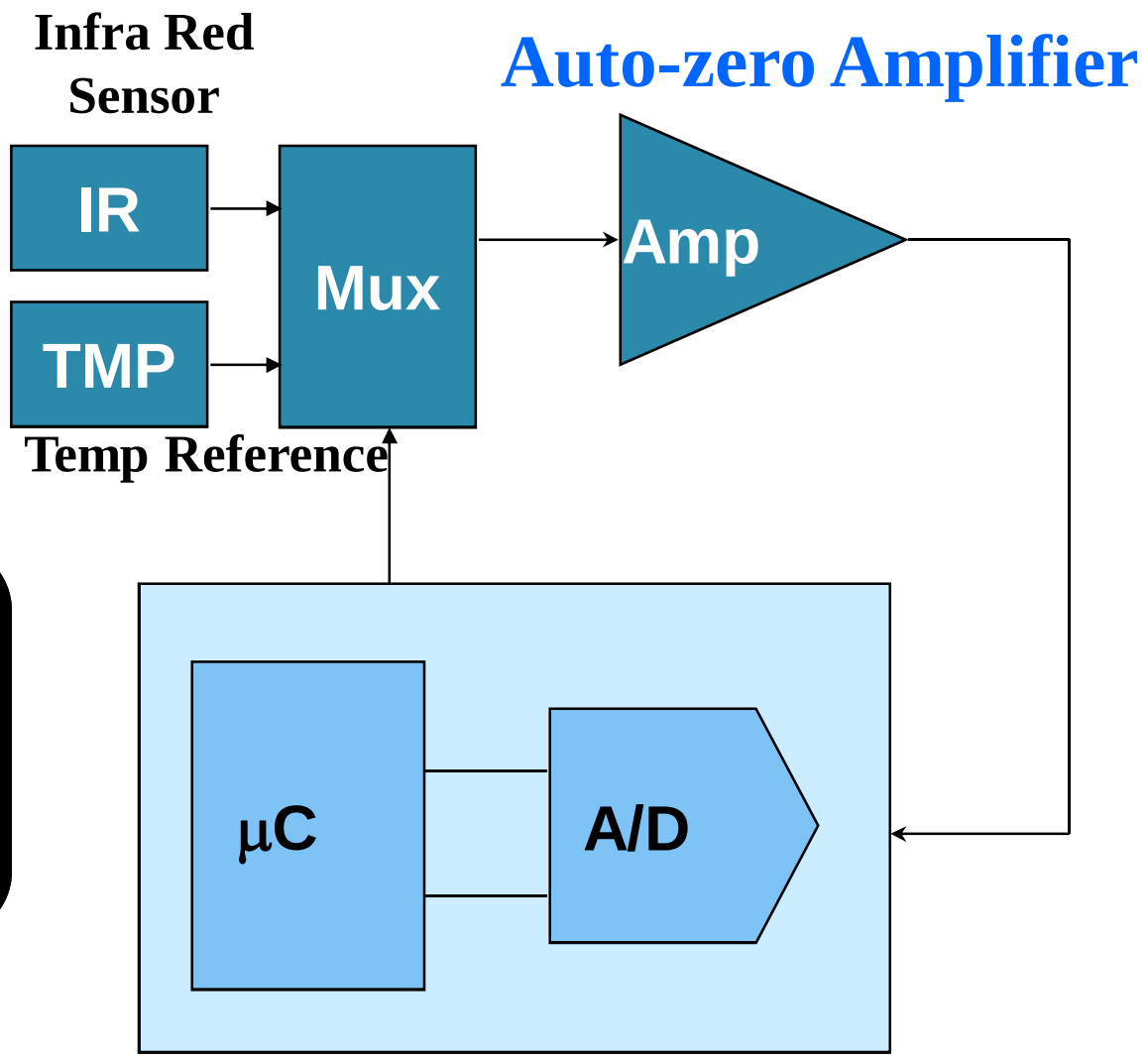


IR Thermal Sensing

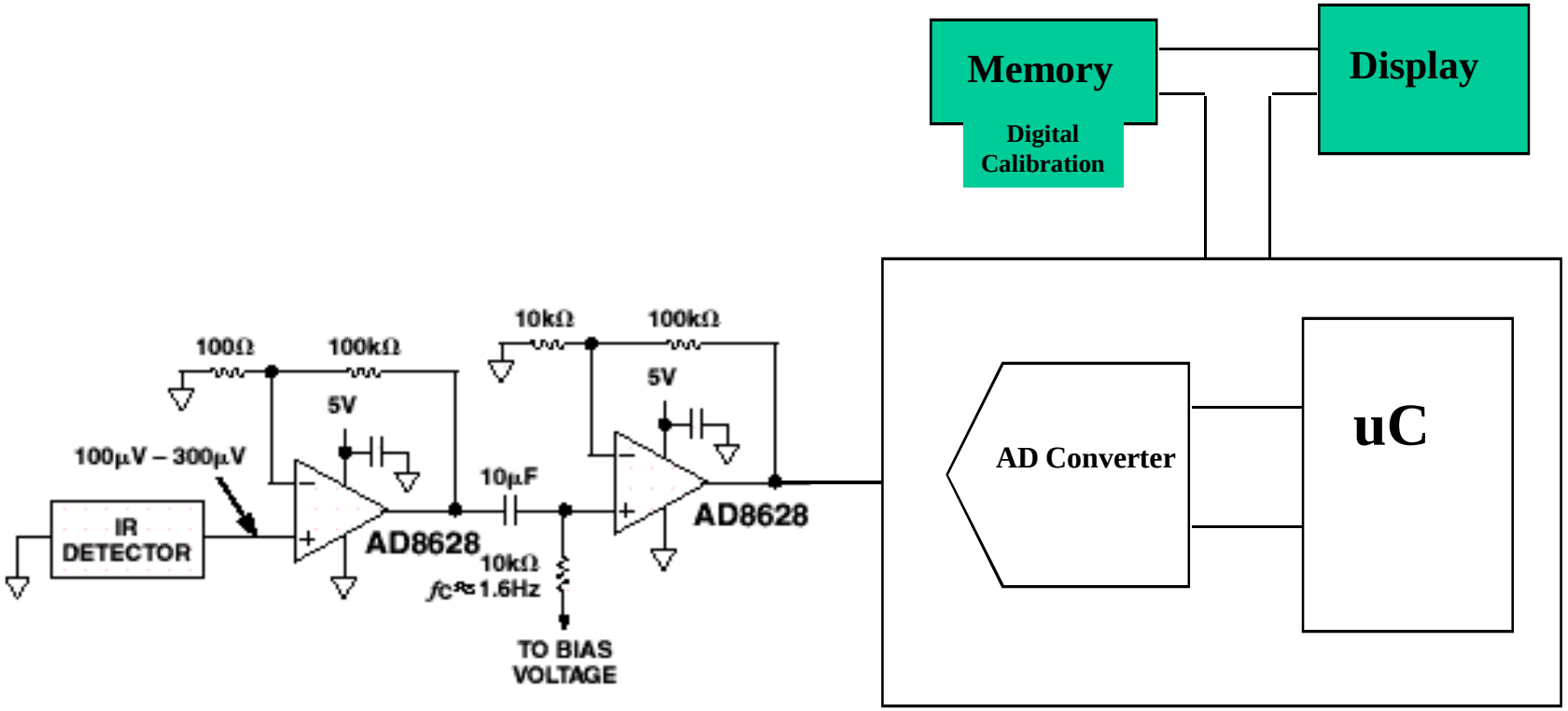
Key Parts

CMOS
AD855X
AD857X
AD8628

Key Requirements
Low Offset Voltage
Low Input Current
Low Drift
High Input Impedance
High Gain

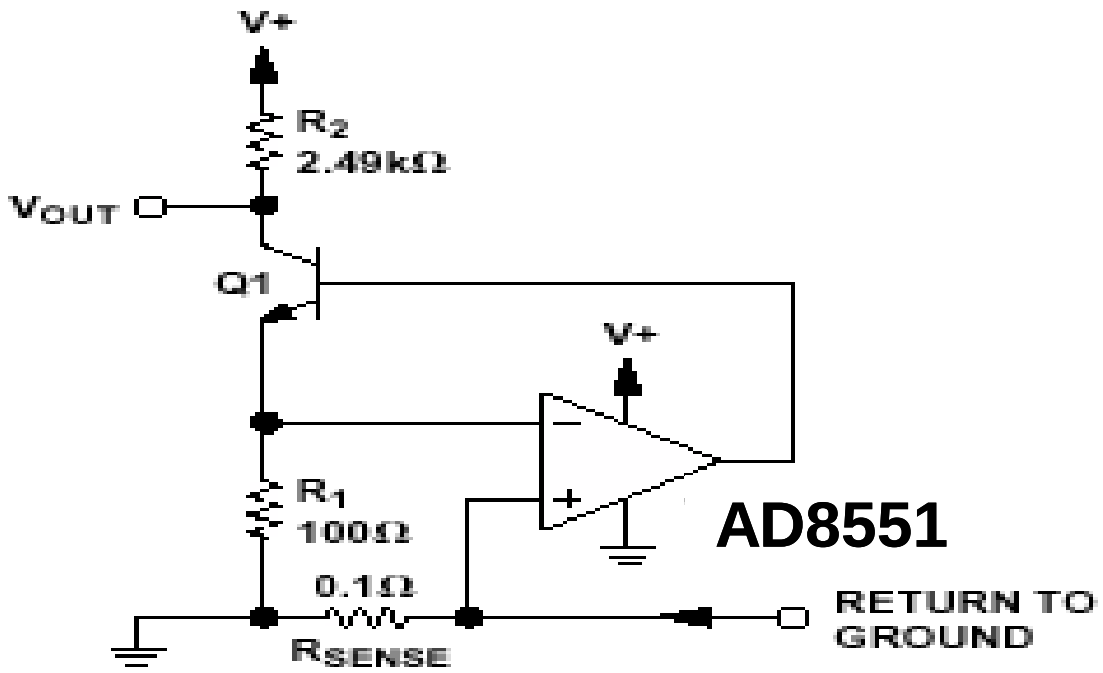


Typical implementation (IR Thermal Sensing)



Micro-Controller

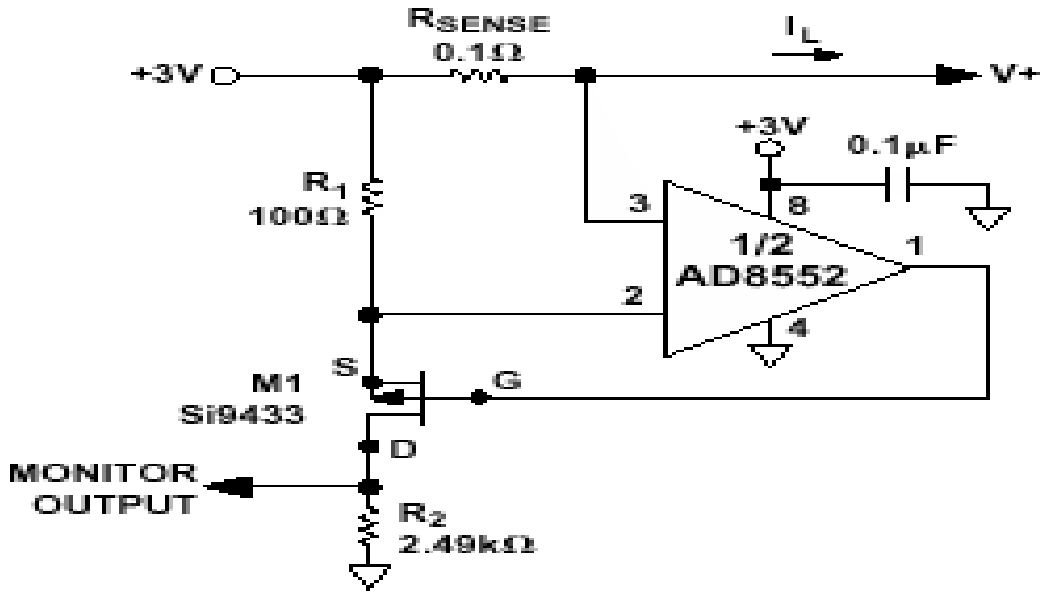
Low Side sensing with I sink



V(out) = (V+)- (R2/R1 * Rsense * IL)

Features: Allows Sinking of current

High Side Sensing with current sink



Monitor Output = R2 *(Rsense /R1) * IL

Features : Great CMRR, very Low Vos ,Allows Sinking of Current

Analysis of Low Side sensing circuit

Parameter	AD8565	AD8551	OP777
Vcc Range	4.5V to 16V	2.7V to 5V	2.7V to 30V
Rail To Rail	I/O	I/O	-Rail only/O
Vos	10mV	5μV	100μV
TcVos	5μV/C	10nV/C	1.3μV/C
IB	600nA	50pA	11nA
CMRR	54dB	110dB	110dB
Isy	850μA	600μA	230μA

Minimum measured I_{Return} based on Amplifier Errors

	AD8565	AD8551	OP777
Vos contribution	100mA	50μA	1mA
TcVos contribution	5mA	40μA	1.3mA
Bias Current contribution	600μA	40nA	11μA
Min I_{Return}	110mA	100μA	2.5mA

Instrumentation and Industrial

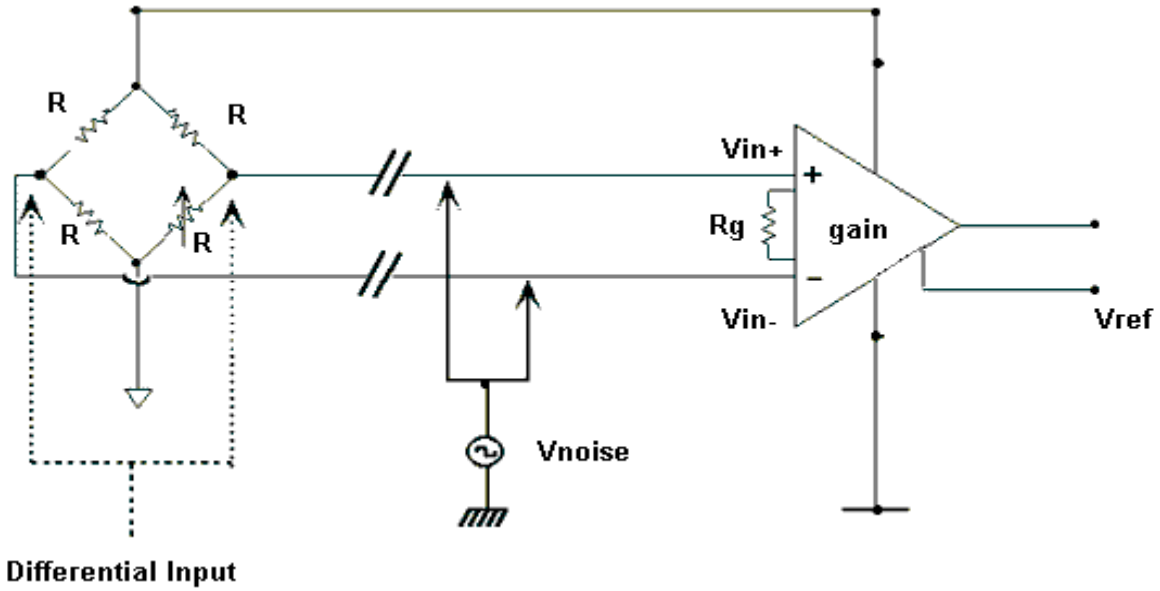
- Instrumentation Amplifiers
- Variable Gain Amplifiers

What is an Instrumentation Amplifier

- It has many applications beyond instrumentation
- Under the category of instrumentation amplifier, there are also: **difference amplifier**, **HCMV amplifier, and differential-to-single ended amplifier**
- It could also be thought of as an IC with multiple op amps and laser trimmed resistors

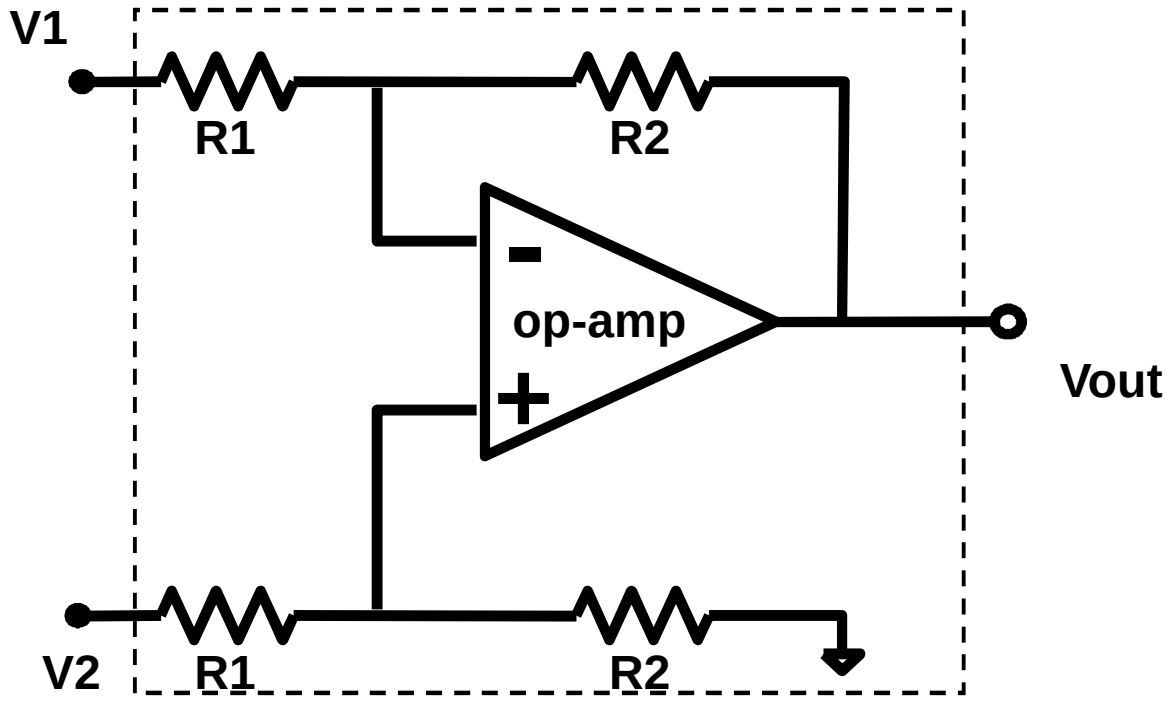
What Does an Instrumentation Amplifier Do

- **Measures small precision signals in noisy environments**
- **Rejects common mode voltage (noise)**



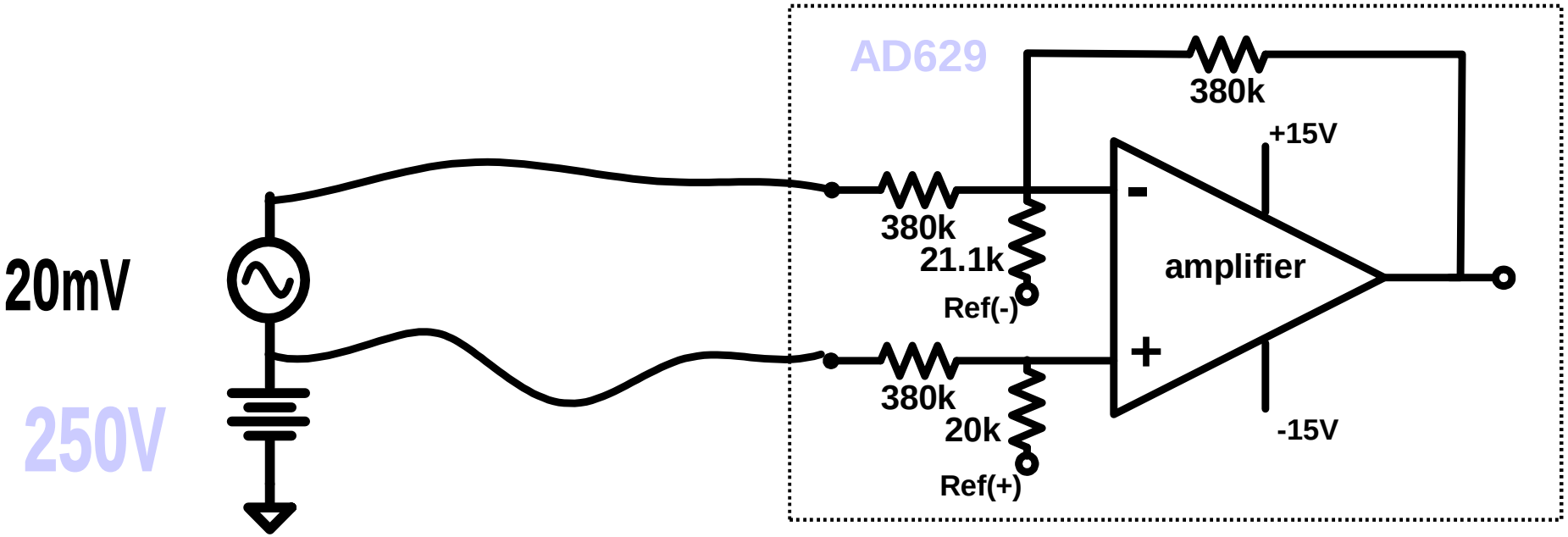
$V_{out} = (V_{in+} - V_{in-}) * gain$

Understanding the Difference Amplifier Architecture



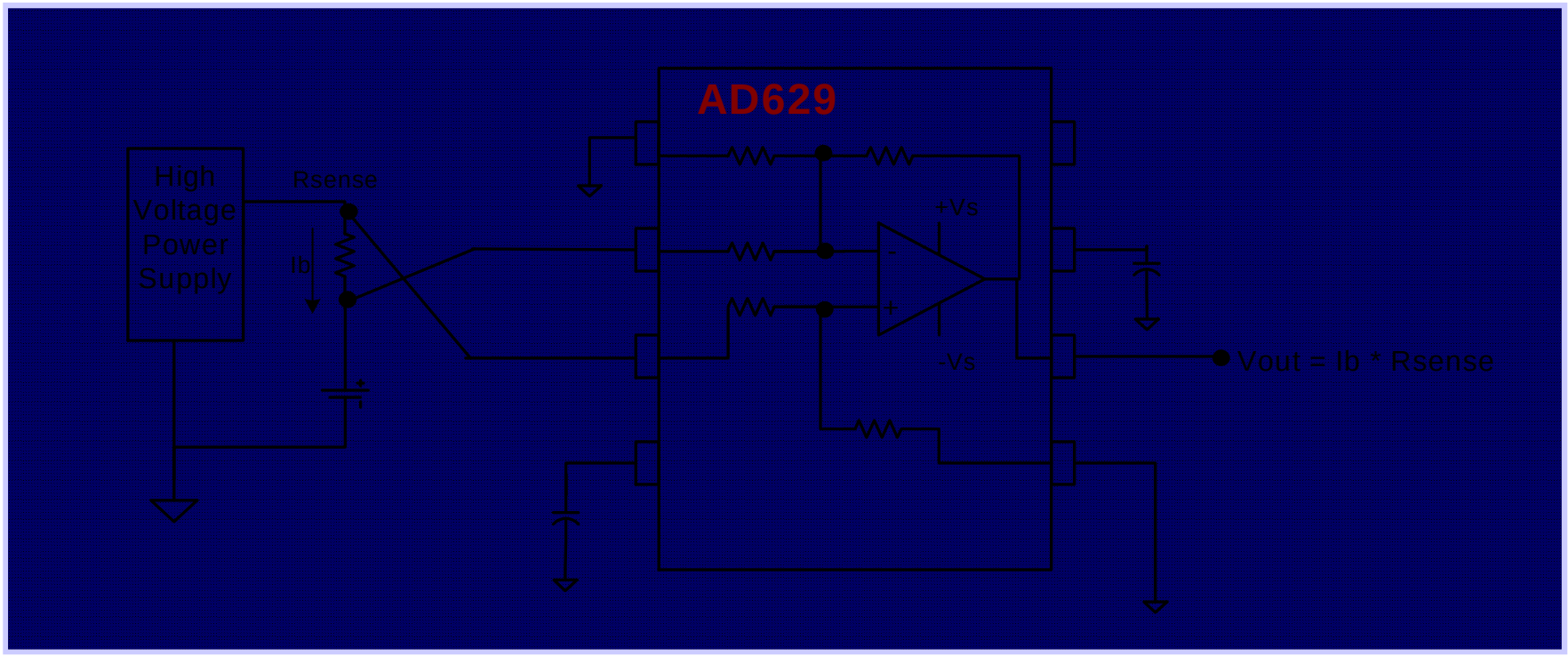
- **When R1=R2** — **Vout = V2-V1**
- **When R1≠ R2** — **Vout = (V2-V1)*R2/R1**

Difference Amplifiers Have High Common Mode Voltage Range



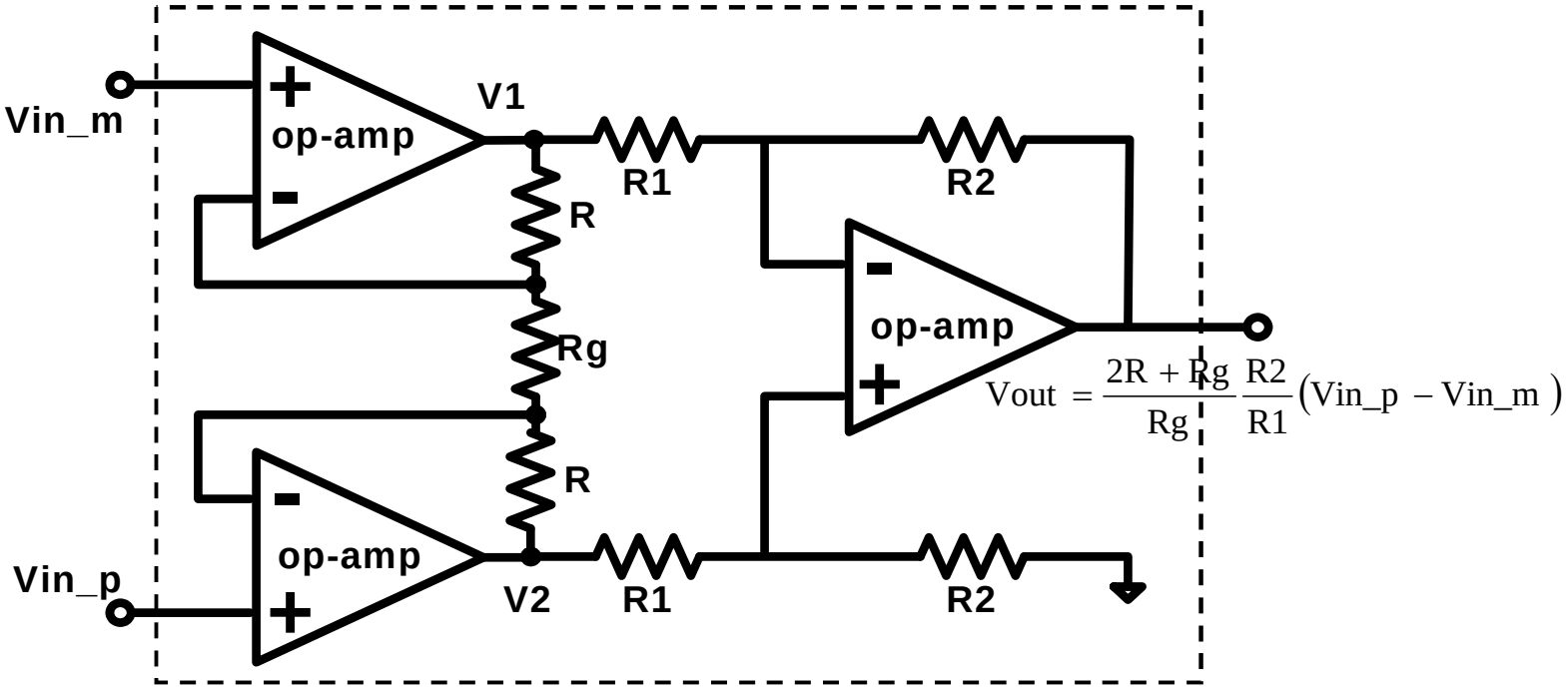
- **With Difference Amplifiers, the input voltage can be higher than the supply voltage.**
- **This Difference Amplifier operates on +/-15V, gains the 20mV signal and rejects the +/-250V common-mode signal.**

Difference Amplifier Application for Battery Charger



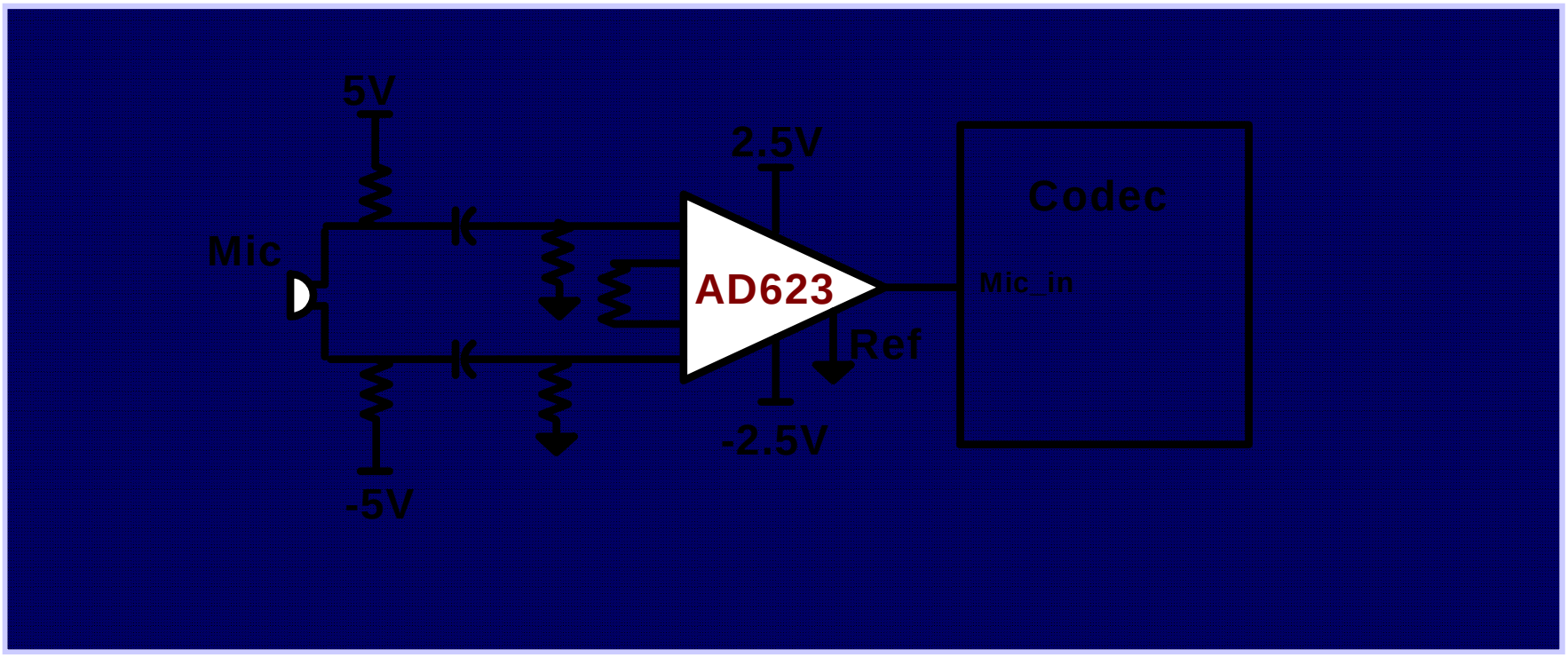
- +/-500V Input Voltage Protection

Understanding the Instrumentation Amplifier Architecture



- **Difference Amplifier**
- **Buffered Inputs**

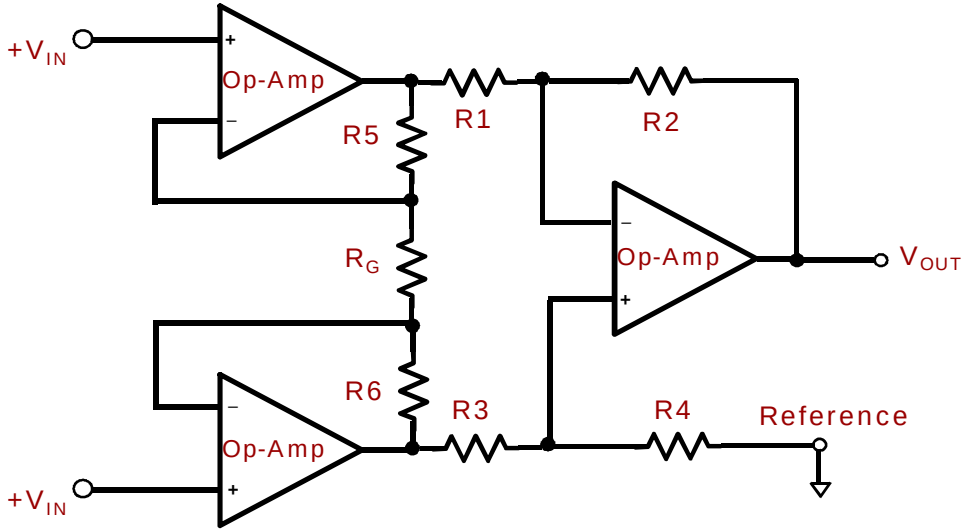
Instrumentation Amplifier Application for PDA



- Instrumentation Amplifier removes 60Hz noise from the body and surroundings to provide a clear signal into the Codec.

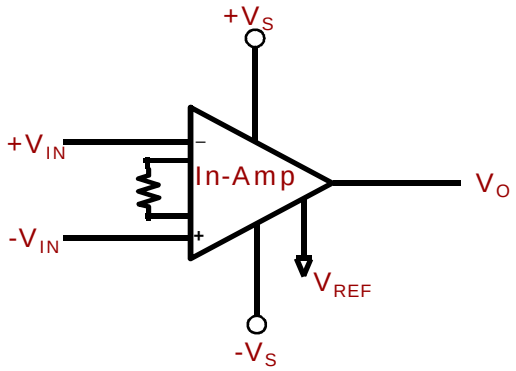
Monolithic vs. Discrete Designs for Instrumentation Amplifiers

Discrete



- 3 op amps
- 7-9 resistors
- More board space
- Higher cost
- 250% more error than monolithic solutions

Monolithic



- 1 instrumentation amplifier
- 1 resistor
- Less board space
- Lower cost
- Better performance

What is a Variable Gain Amplifier

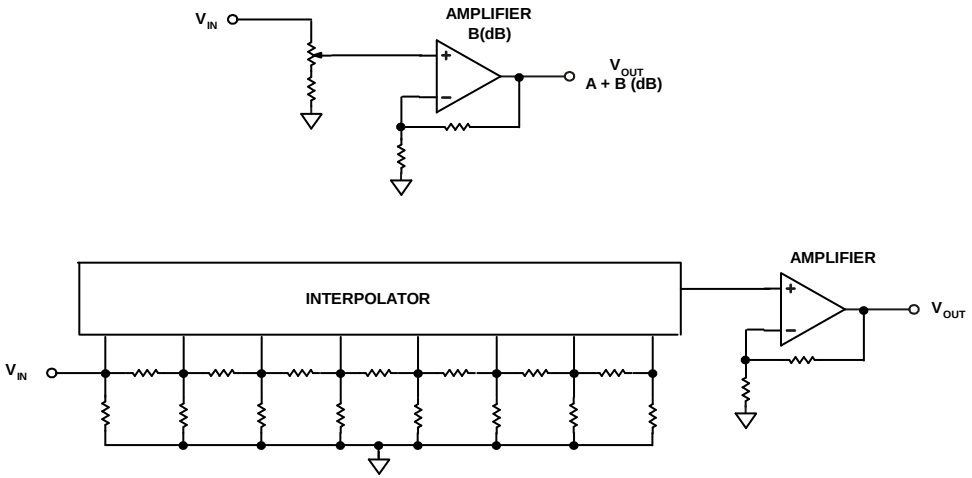
- A variable gain amplifier is a special kind of amplifier whose gain can be dynamically controlled in ‘real-time’ by an externally applied control voltage. In its simplest form, it can be visualized as an amplifier with an electronic gain control.
- Analog Devices makes variable gain amplifiers that cover frequencies ranging up to 1GHz. The variable gain amplifiers covered in this presentation are the low speed ones <250MHz

How do Variable Gain Amplifiers Work?

- Analog Devices builds two basic styles of VGAs, the X-Amp and the translinear core (aka analog multiplier.) X-Amps are complex and expensive to manufacture but have low noise. Translinear cores are simpler structures and thus lower cost, but more noisy. The block diagrams of the two styles are shown below:

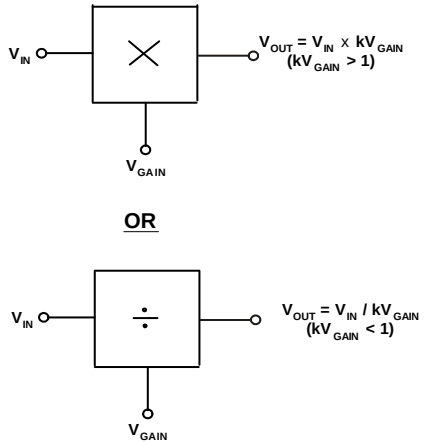
X-Amp

The X-amp (exponential) uses a resistor ladder as the gain element. An array of special amplifiers (interpolator)steer current among the taps.



Translinear Core

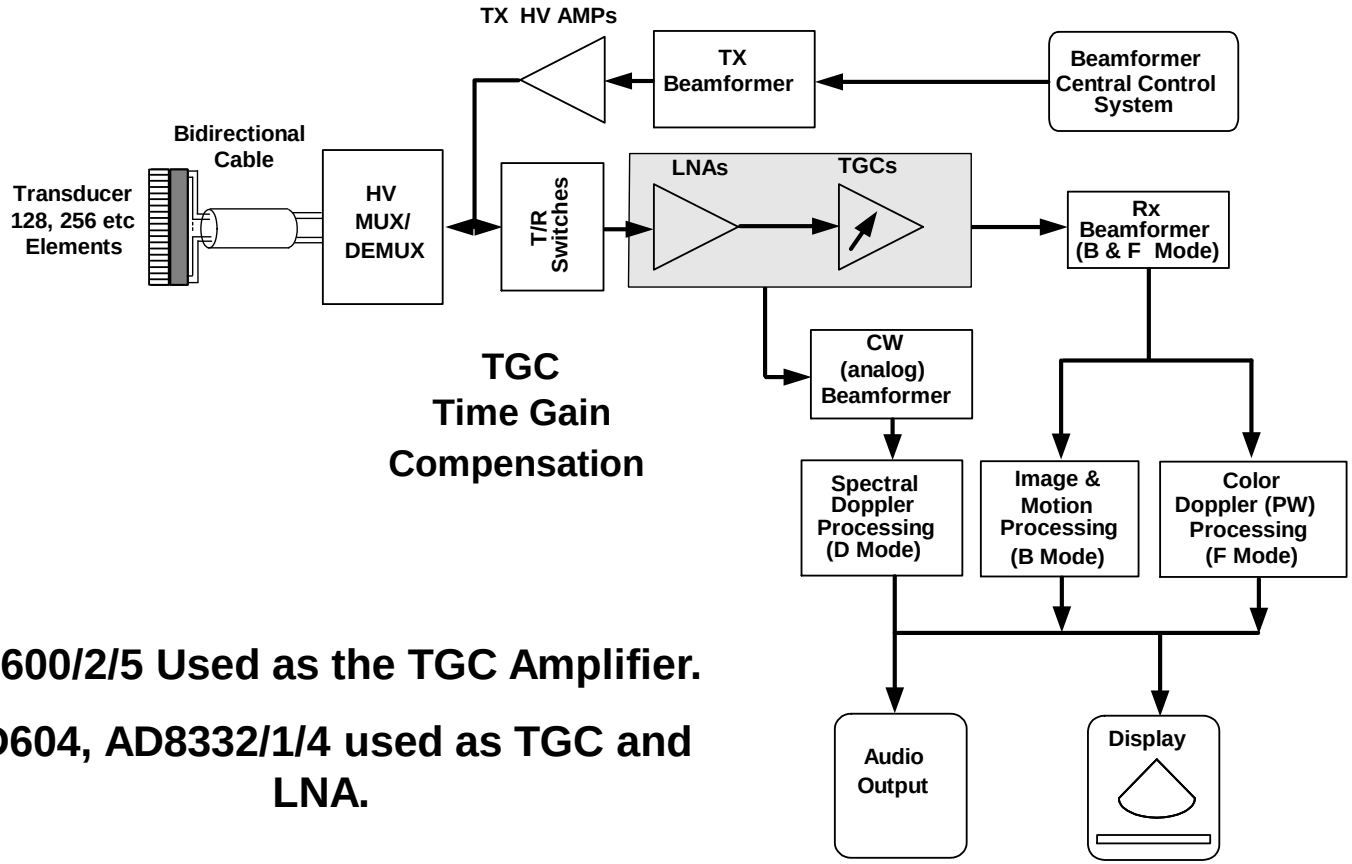
Translinear cores can be configured as a multiplier or divider. A VGA can operate in either mode.



When Do You Use a VGA?

- In certain applications, the information of interest is contained within a widely-changing dynamic signal. Examples of these kinds of signals are an returning ultrasound echo and a communications signal (Intermediate Frequency) in a receiver. An amplifier with fixed gain (including a PGA,) will operate linearly (i.e. without distortion or saturation) for low-level or high-level signals, but **not** both.
- A VGA provides a means of amplifying such signals, without distortion or saturation, and can be used as the controlled element of an Automatic Gain Control (AGC) circuit in a receiver, or as the controlling amplifier in a Timed-Gain-Control circuit of an Ultrasound system.

VGAs Used in an Ultrasound System



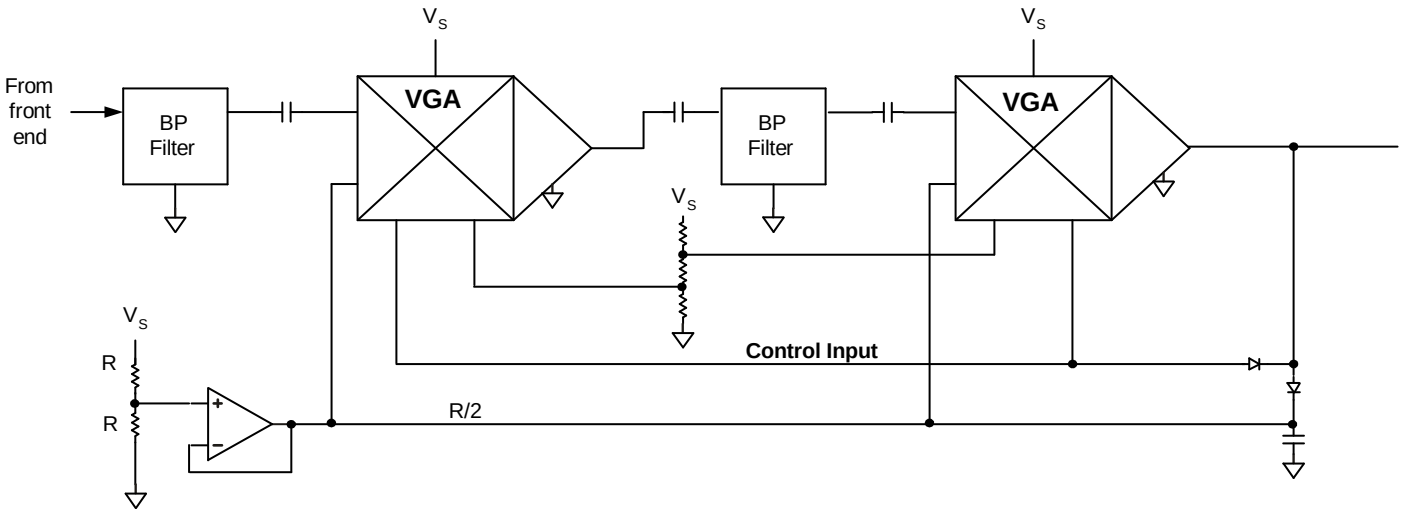
TGC
Time Gain
Compensation

AD600/2/5 Used as the TGC Amplifier.

AD604, AD8332/1/4 used as TGC and LNA.

VGAs Used in Communications Systems

- Simplified Block Diagram, IF Amplifier



Typical IF Frequency is 10.7 MHz, however our VGAs have also been used at 455 kHz, 44MHz, and higher (at the users peril.) The AD8330 should be ideal for such circuits thanks to low cost and good high-frequency performance.

Unit - III

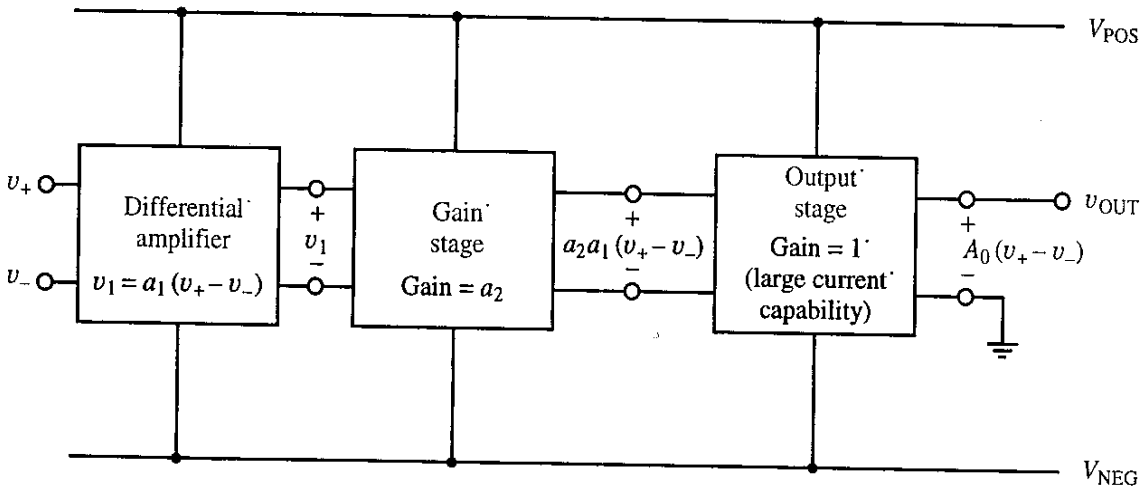
FEEDBACK AND OPERATIONAL AMPLIFIERS

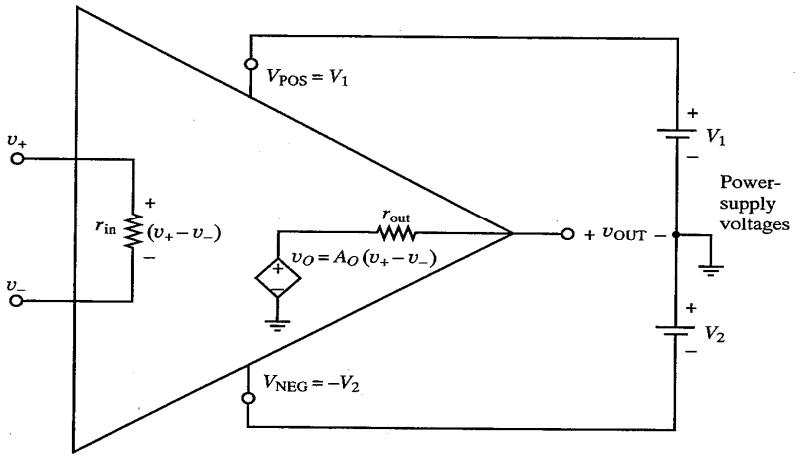
Operational Amplifiers

- An operational amplifier (called op-amp) is a specially-designed amplifier in bipolar or CMOS (or BiCMOS) with the following typical characteristics:
  - Very high gain (10,000 to 1,000,000)
  - Differential input
  - Very high (assumed infinite) input impedance
  - Single ended output
  - Very low output impedance
  - Linear behavior (within the range of $V_{NEG} < v_{out} < V_{POS}$
- Op-amps are used as generic “black box” building blocks in much analog electronic design
  - Amplification
  - Analog filtering
  - Buffering
  - Threshold detection
- Chapter 2 treats the op-amp as a black box; Chapters 8-12 cover details of op- amp design
  - Do not really need to know all the details of the op-amp circuitry in order to use it

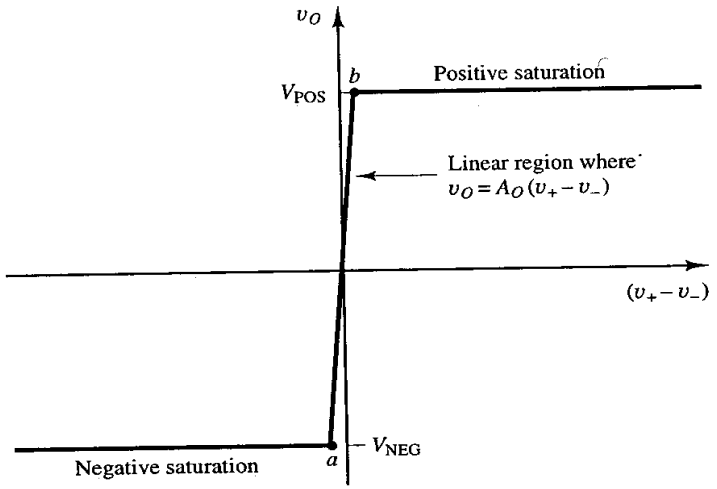
Generic View of Op-amp Internal Structure

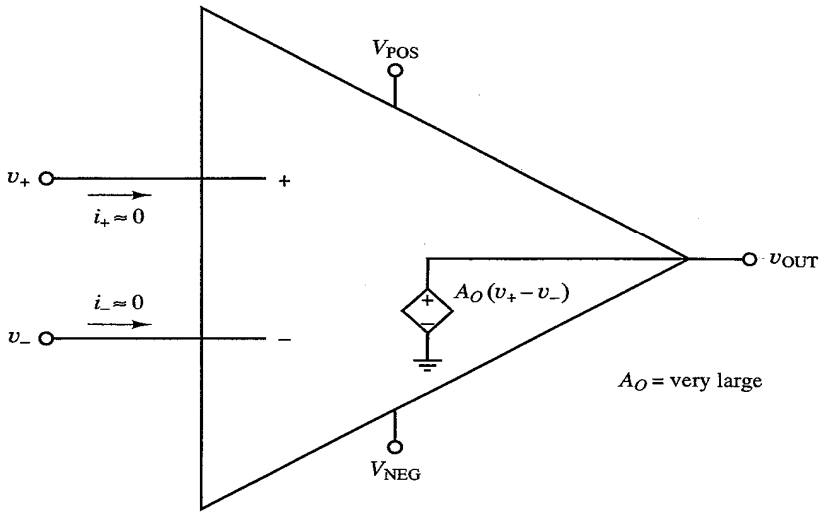
- An op-amp is usually comprised of at least three different amplifier stages (see figure)
  - Differential amplifier input stage with gain $a_1(v_+ - v_-)$ having inverting & non-inverting inputs
  - Stage 2 is a "Gain" stage with gain a_2 and differential or singled ended input and output
  - Output stage is an emitter follower (or source follower) stage with a gain = ~1 and single-ended output with a large current driving capability
- Simple Op-Amp Model (lower right figure):
  - Two supplies V_{POS} and V_{NEG} are utilized and always assumed (even if not explicitly shown)
  - An input resistance r_{in} (very high)
  - An output resistance r_{out} (very low) in series with output voltage source v_o
  - Linear Transfer function is $\mathbf{v_o = a_1\, a_2(v_+ - v_-) = A_o(v_+ - v_-)}$ where A_o is open-loop gain
  - v_o is clamped at V_{POS} or V_{NEG} if $A_o\,(v_+ - v_-) > V_{POS}$ or $< V_{NEG}$, respectively





Ideal Op-amp Approximation

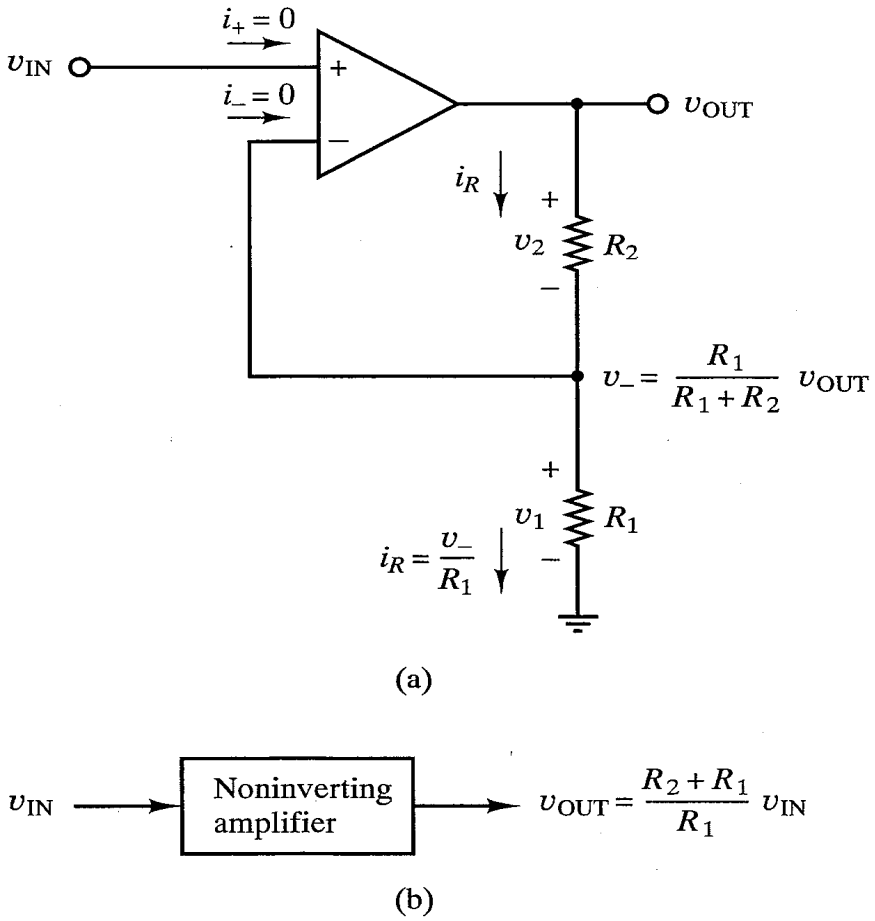




- Because of the extremely high voltage gain, high input resistance, and low output resistance of an op-amp, we use the following ideal assumptions:
  - The saturation limits of v_0 are equal V_{POS} & V_{NEG}
  - If **(v_+ - v_-)** is slightly positive, v_0 saturates at V_{POS}; if **(v_+ - v_-)** is slightly negative, v_0 saturates at V_{NEG}
  - If v_0 is not forced into saturation, then **(v_+ - v_-)** must be very near zero and the op-amp is in its linear region (which is usually the case for negative feedback use)
  - The input resistance can be considered **infinite** allowing the assumption of zero input currents
  - The output resistance can be considered to be **zero**, which allows v_{out} to equal the internal voltage v_0
- The idealized circuit model of an op-amp is shown at the left-bottom figure
- The transfer characteristic is shown at the left-top
- Op-amps are typically used in negative feedback configurations, where some portion of the output is brought back to the negative input v_-

Linear Op-amp Operation: Non-Inverting Use

Fig. 2.5 **(a) Noninverting amplifier configuration; (b) block diagram of circuit's operational function.**



- An op-amp can use ***negative feedback*** to set the closed-loop gain as a function of the circuit external elements (resistors), independent of the op-amp gain, as long as the internal op-amp gain is very high
- Shown at left is an ideal op-amp in a non-inverting configuration with negative feedback provided by voltage divider R1, R2
- Determination of closed-loop gain:
  - Since the input current is assumed zero, we can write $\mathbf{v_- = R1/(R1 + R2)v_{OUT}}$
  - But, since $v_+ =\sim v_-$ for the opamp operation in its linear region, we can write

    $v_- = v_{IN} = R1/(R1 + R2)v_{OUT}$

    or, $\mathbf{v_{OUT} = ((R1 + R2)/R1)v_{IN}}$
- We can derive the same expression by writing

  $v_{OUT} = A(v_+ - v_-) = A\{v_{IN} – [R1/(R1 + R2)]\ v_{OUT}\}$

  and solving for v_{OUT} with A>>1

  Look at Example 2.1 and plot transfer curve.

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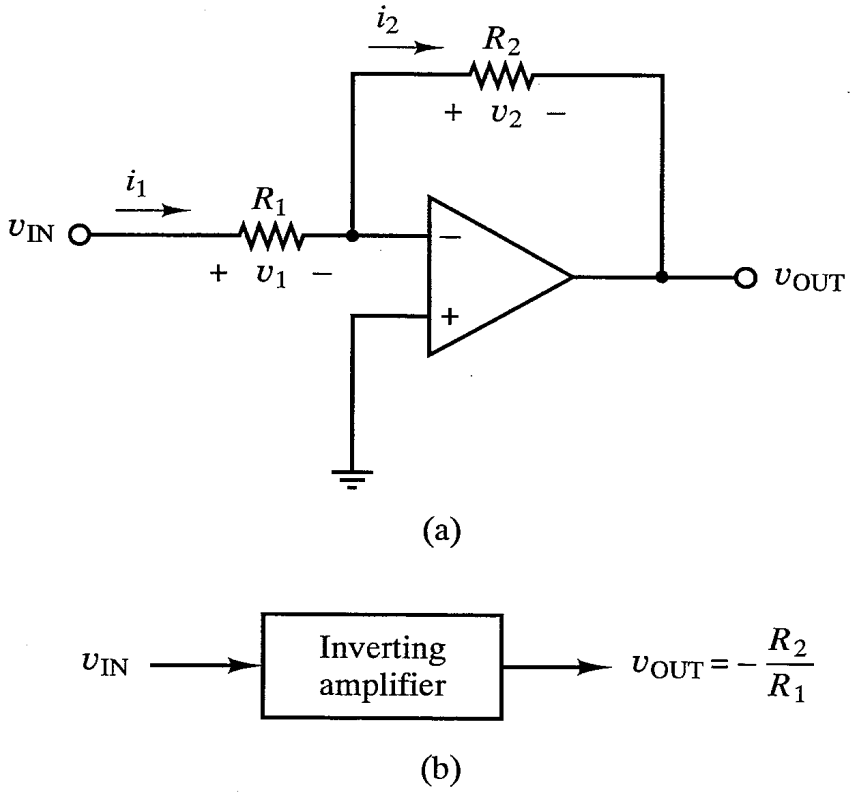
The Concept of the Virtual Short

- The op-amp with negative feedback forces the two inputs v+ and v- to have the same voltage, even though no current flows into either input.
  - This is sometimes called a **"virtual short"**
  - As long as the op-amp stays in its linear region, the output will change up or down until v- is almost equal to v+
  - If v_{IN} is raised, v_{OUT} will increase just enough so that v_- (tapped from the voltage divider) increases to be equal to v_+ (= v_{IN})
    - In v_{IN} is lowered, v_{OUT} lowers just enough to make v- = v+
  - The negative feedback forces the "virtual short" condition to occur
- Look at Exercise 2.4 and 2.5
- For consideration:
  - What would the op-amp do if the feedback connection were connected to the v+ input and v_{IN} were connected to the v- input?
    - Hint: This connection is a positive feedback connection!

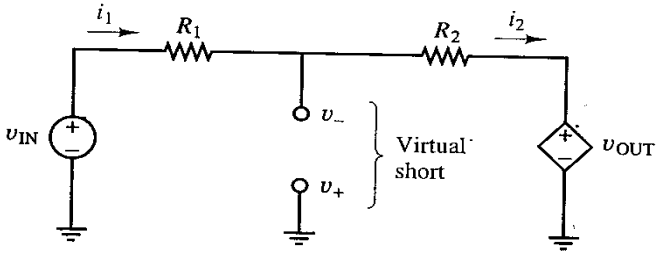
Linear Op-amp Operation: Inverting Configuration

Fig. 2.8 **(a) Inverting amplifier configuration; (b) block diagram of circuit's operational function.**



- An op-amp in the inverting configuration (with negative feedback) is shown at the left
  - Feedback is from v_{OUT} to v- through resistor R2
  - v_{IN} comes in to the v- terminal via resistor R1
  - v+ is connected to ground
- Since v- = v+ = 0 and the input current is zero, we can write
  - $i_1 = (v_{IN} - 0)/R1 = i_2 = (0 - v_{OUT})/R2$ or,

    $v_{OUT} = - (R2/R1)\ v_{IN}$
- The circuit can be thought of as a resistor divider with a virtual short (as shown below)
  - If the input v_{IN} rises, the output v_{OUT} will fall just enough to hold v- at the potential of v+ (=0)
  - If the input v_{IN} drops, v_{OUT} will rise just enough to force v- to be very near 0
- Look at Example 2.2 and Exercises 2.7-2.10



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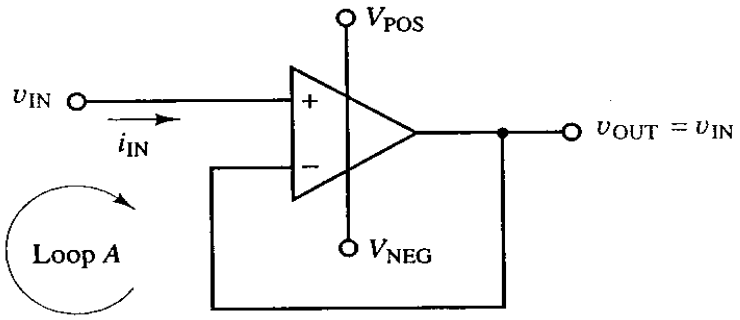
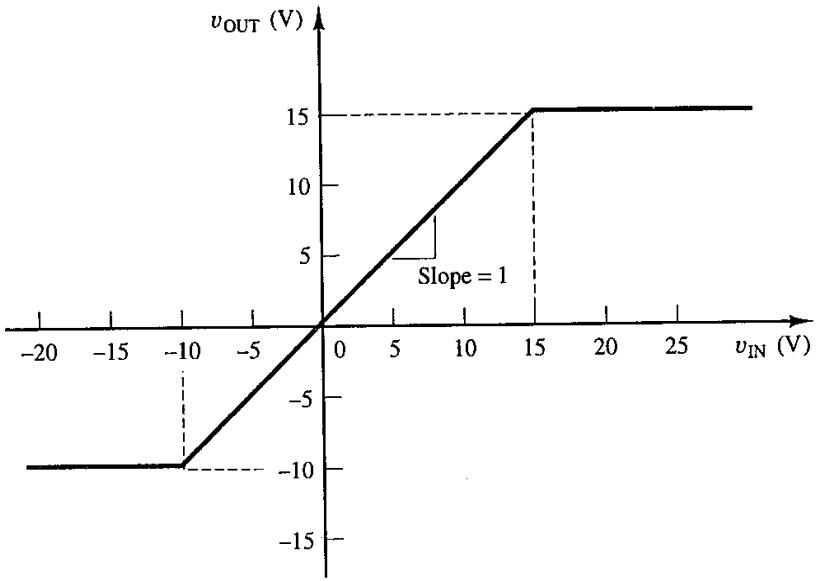
Input Resistance for Inverting and Non-inverting Op-amps

- The non-inverting op-amp configuration of slide 2-4 has an apparent input resistance of infinity, since $i_{IN} = 0$ and $\mathbf{R_{IN} = v_{IN}/i_{IN} = v_{IN}/0 = infinity}$
- The inverting op-amp configuration, however, has an apparent input resistance of R1
  - since $\mathbf{R_{IN} = v_{IN}/i_{IN} = v_{IN}/[(v_{IN} - 0)/R1] = R1}$

Op-amp Voltage Follower Configuration



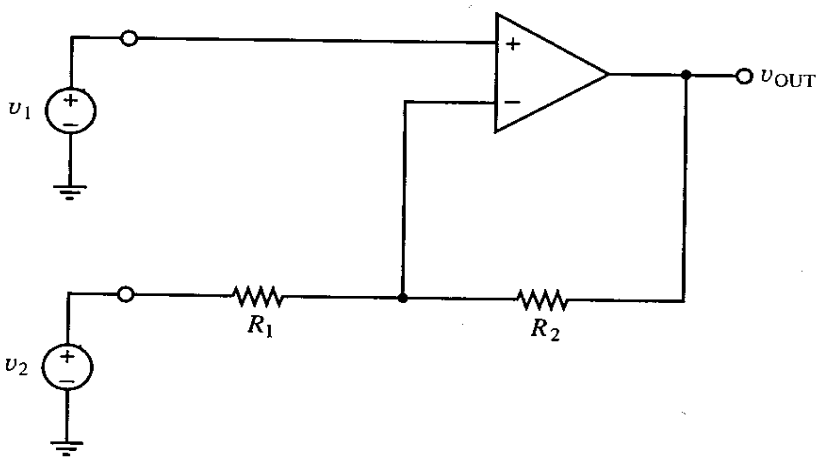


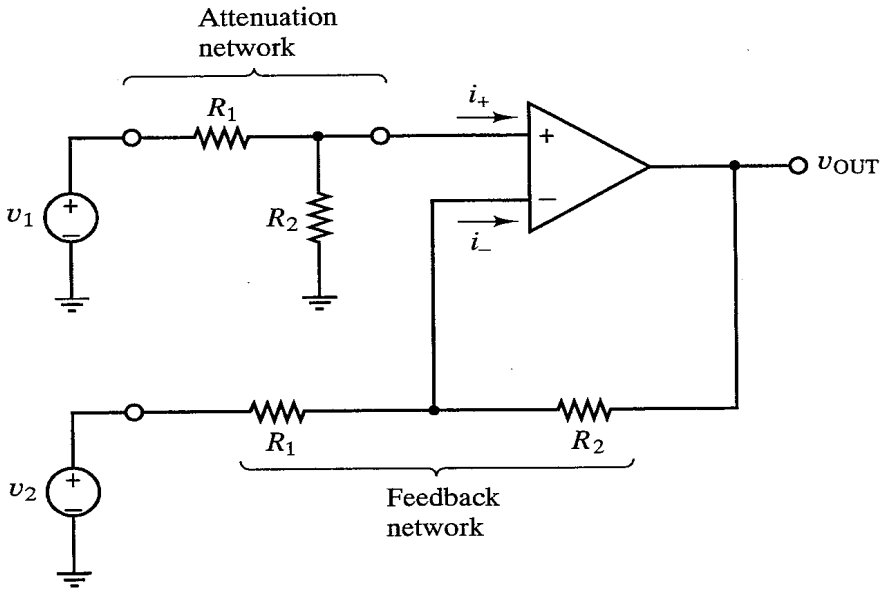
- The op-amp configuration shown at left is a voltage-follower often used as a buffer amplifier
  - Output is connected directly to negative input (negative feedback)
  - Since v+ = v- = v_{IN}, and v_{OUT} = v-, we can see by inspection that the closed-loop gain $A_0 = 1$
  - We can obtain the same result by writing

    $v_{OUT} = A\,(v_{IN} - v_{OUT})$ or

    $\mathbf{v_{OUT}/v_{IN} = A/(1 + A) = 1}$ for A >> 1
- A typical voltage-follower transfer curve is shown in the left-bottom figure for the case V_{POS} = +15V and V_{NEG} = -10V
  - For v_{IN} between –10 and +15 volts, $v_{OUT} = v_{IN}$
  - If v_{IN} exceeds +15V, the output saturates at V_{POS}
  - If v_{IN} < -10V, the output saturates at V_{NEG}
- Since the input current is zero giving zero input power, the voltage follower can provide a large power gain
- Example 2.3 in text.

Op-amp Difference Amplifier

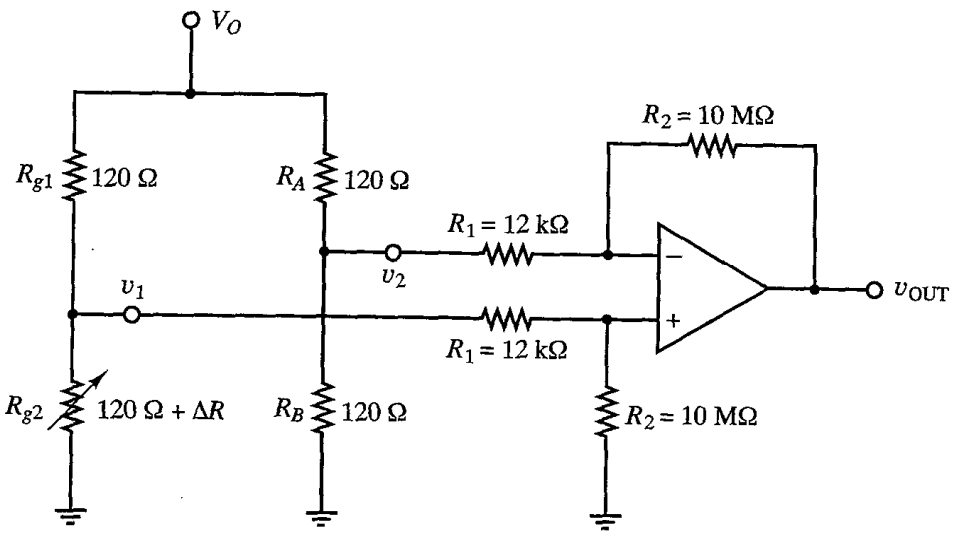




- The “difference amplifier” shown at the left-top combines both the inverting and non-inverting op-amps into one circuit
  - Using superposition of the results from the two previous cases, we can write
  - $v_{OUT} = [(R1 + R2)/R1]v_1 – (R2/R1)v_2$
  - The gain factors for both inputs are different, however
- We can obtain the same gain factors for both v_1 and v_2 by using the modified circuit below
  - Here the attenuation network at v_1 delivers a reduced input $v+ = v_1(R2/(R1 + R2))$
  - Replacing v_1 in the expression above by the attenuation factor, gives us

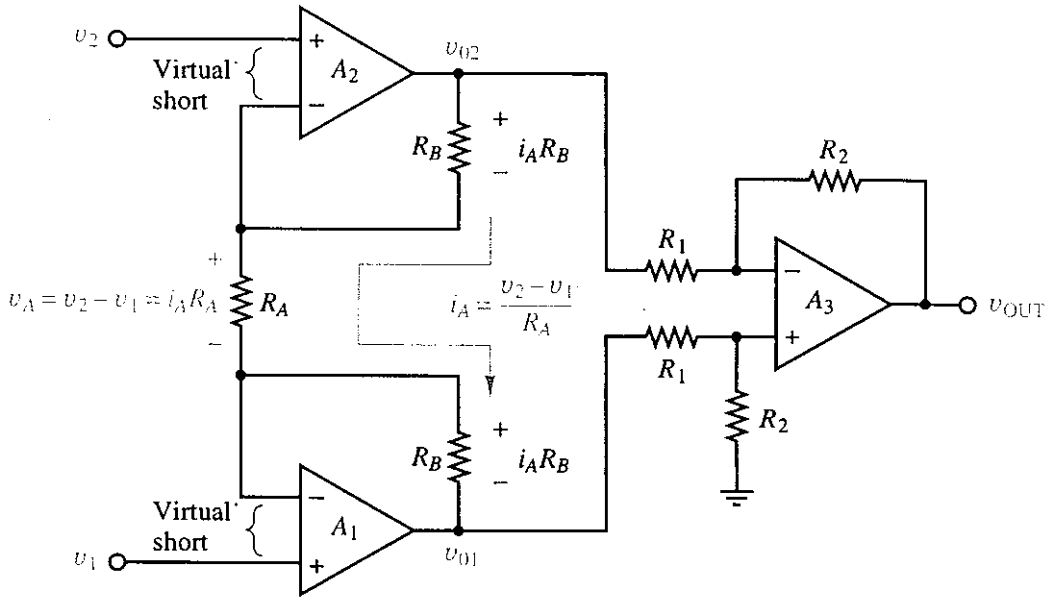
    $v_{OUT} = (R2/R1)(v_1 – v_2)$
- The difference amplifier will work properly if the attenuation network resistors (call them R3 & R4) are related to the feedback resistors R1 & R2 by the relation R3/R4 = R1/R2 (i.e. same ratio)

Ex. Difference Amplifier with a Resistance Bridge



- The example of Fig's 2.14 and 2.15 in the text shows a difference amplifier used with a bridge circuit and strain gauge to measure strain.
- Operation:
  - The amplifier measures a difference in potential between v1 and v2.
  - By choosing $R_A = R_B = Rg$ (unstressed resistance of Rg1 and Rg2), it is possible to obtain an approx linear relationship between v_{OUT} and ΔL, where ΔL is proportional to the strain across the gauge.
- Design:
  - In order for the bridge to be accurate, the input resistances of the difference op-amp must be large compared to R_A, $R_{B,}$, & Rg
    - Input resistance at v1 (with v2 grounded) is R1 + R2 =~ 10 Mohm
    - Input resistance at v2 (with v1 grounded) is just R1 = 12 K due to the v1-v2 virtual short

Instrumentation Amplifier



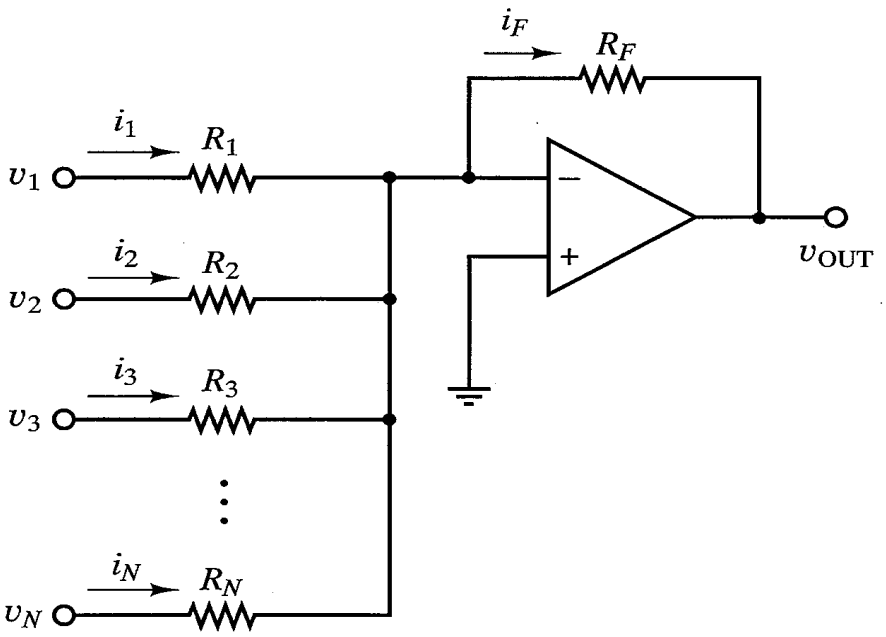
- Some applications, such as an oscilloscope input, require differential amplification with extremely high input resistance
- Such a circuit is shown at the left
  - A3 is a standard difference op-amp with differential gain R2/R1
  - A1 and A2 are additional op-amps with extremely high input resistances at v1 and v2 (input currents = 0)

- **Differential gain of input section:**
  - **Due to the virtual shorts at the input of A1 and A2, we can write $i_A = (v2 - v1) / R_A$**
  - **Also, i_A flows through the two R_B resistors, allowing us to write $v_{02} - v_{01} = i_A(R_A + 2 R_B)$**
    - **Combining these two equations with the gain of the A3 stage, we can obtain**

$$v_{OUT} = (R2/R1)(1 + [2R_B/R_A])(v1 - v2)$$

- **By adjusting the resistor R_A, we can adjust the gain of this instrumentation amplifier**

Summation Amplifier

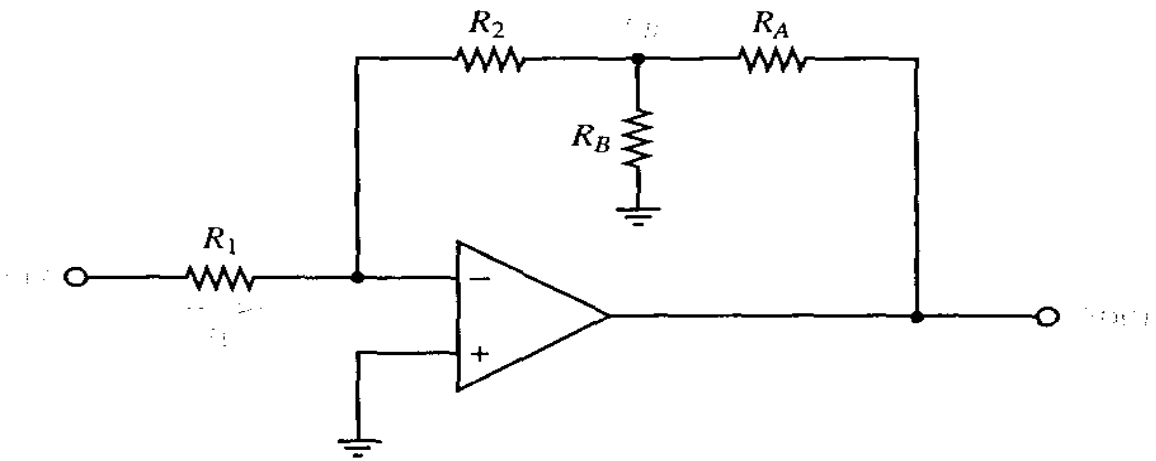


- A summation op-amp (shown at left) can be used to obtain a weighted sum of inputs v1…v_N
  - The gain for any input k is given by R_F/R_k
- If any input goes positive, v_{OUT} goes negative just enough to force the input v- to zero, due to the virtual short nature of the op-amp
  - Combining all inputs, we have

    $v_{OUT} = -R_F(v_1/R_1 + v_2/R_2 + .. + v_N/R_N)$
  - The input resistance for any input k is given by R_k due to the virtual short between v- and v+
- Example 2.5 – use as an audio preamp with individual adjustable gain controls
  - Note effect of microphone's internal resistance

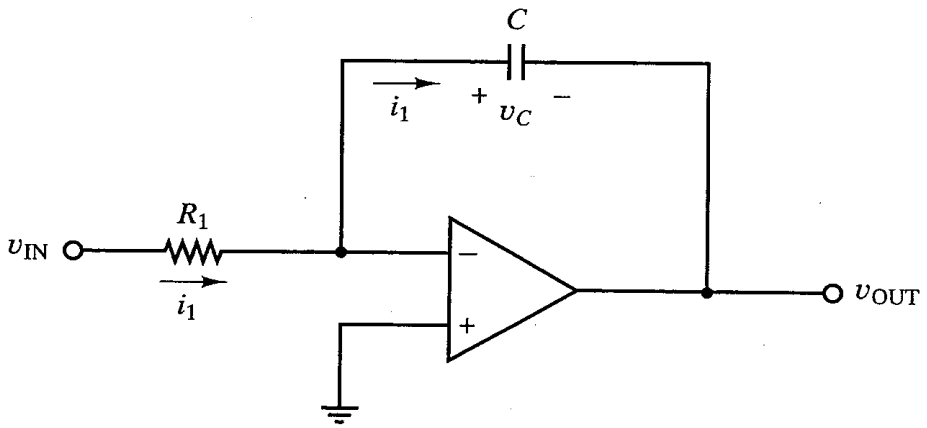
Op-amp with T-bridge Feedback Network

- To build an op-amp with high closed-loop gain may require a high value resistor R2 which may not be easily obtained in integrated circuits due to its large size
- A compromise to eliminate the high value resistor is the op-amp with T-bridge feedback network, shown below
  - R_A and R_B comprise a voltage divider generating node voltage $v_B = v_{OUT}\, R_B/(R_A + R_B)$, assuming that R2 >> $R_A||R_B$
  - Since v_B is now fed back to v-, an apparent gain v_B/v_{IN} = -(R2/R1) can be written
- Combining these two equations allows us to write $v_{OUT} = -(R2/R1)([R_A + R_B]/R_B)v_{IN}$
- Fairly large values of closed-loop gain can be realized with this network without using extremely large IC resistors

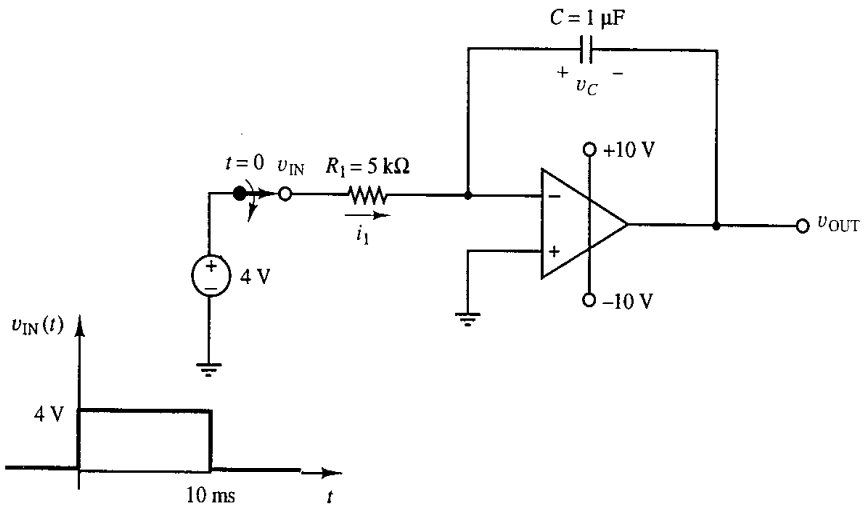


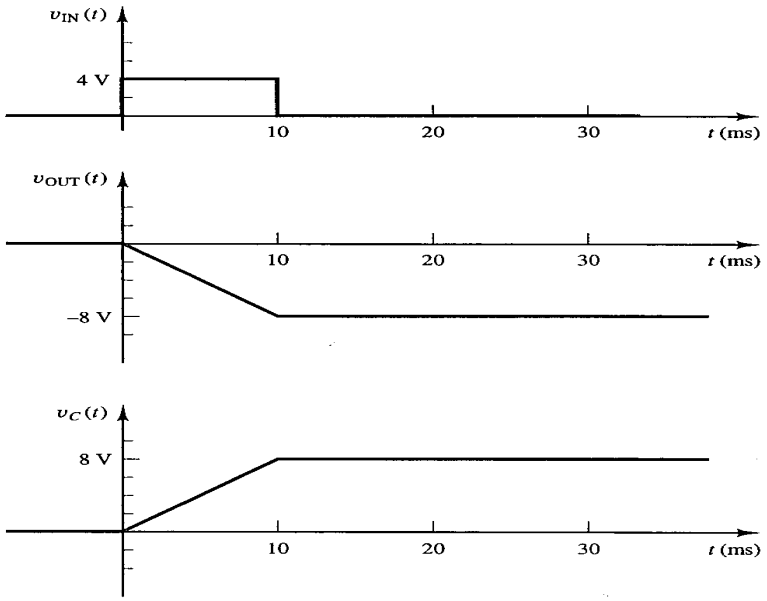
Op-amp Integrator Network

- Shown below is an op-amp integrator network
  - The output will be equal to the integral of the input, as long as the op-amp remains in its linear region
  - Due to the virtual short property of the op-amp input, we can write $i_1 = v_{IN}/R_1$
  - This current i_1 starts charging the capacitor C according to the relation $i_1 = C(dv_C/dt)$
- Since v- remains at GND, the output drops below GND as C charges and the time derivative of v_{OUT} becomes the negative of the time derivative of v_C
  - since $v_C = 0 - v_{OUT}$
- Combining the above equations, we obtain
  - $dv_{OUT}/dt = -i_1/C = -v_{IN}/R_1C$
- Solving for $v_{OUT}(t)$ and assuming C is initially uncharged, we obtain
  - $v_{OUT}(t) = (-1/R_1C) \int v_{IN}\, dt$ where the integral is from 0 to t



Op-amp Integrator Example



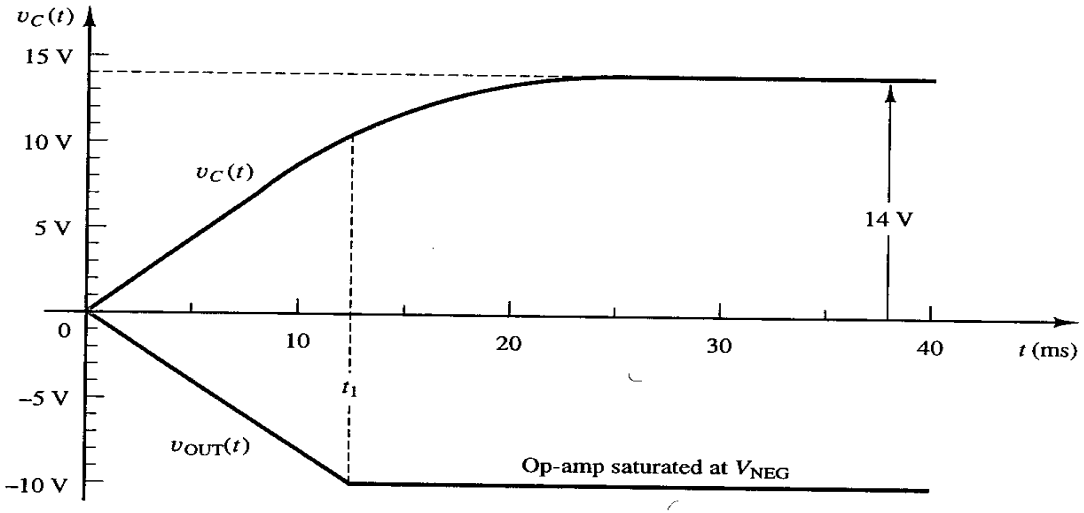


- Given an input signal of 4V square wave for 10 ms duration, what is the integrator output versus time for the integrator circuit at the left?
  - The current into the capacitor during the square wave is constant at 4V/5Kohm = 0.8 mA
  - Using the integral expression from the previous chart, the capacitor voltage will increase linearly in time ($1/R_1C$) 4t = 0.8t V/ms during the square wave duration
  - The output will therefore reduce linearly in time by – 0.8t V/ms during the pulse duration, falling from 0 to –8 volts, as shown in the figure at left
  - Since at 10 ms the output will be –8 V > V_{NEG}, the op-amp will not saturate during the 10 ms input pulse

Op-amp Integrator Example with Long Pulse

- Consider a case with an infinitely long 4V pulse
  - The capacitor will continue to charge linearly in time, but will eventually reach 10V which will force v_{OUT} to –10V (= V_{NEG}) and saturate the op-amp (at 12.5 ms)
  - After this time, the op-amp will no longer be able to maintain v- at 0 volts
  - Since v_{OUT} is clamped at –10V, the capacitor will continue to charge exponentially with time constant R_1C until v- = +4V
    - During this time the capacitor voltage will be given by

      $$\mathbf{v_C(t) = 10 + 4[1 - exp(t_1 - t)/R_1C]}$$ where t_1 = 12.5 ms
    - At t = t_1 , v_C = 10 V and at t = infinity, v_C = 14 V
  - The resulting capacitor and output waveforms are shown below.



Op-amp as a Differentiator

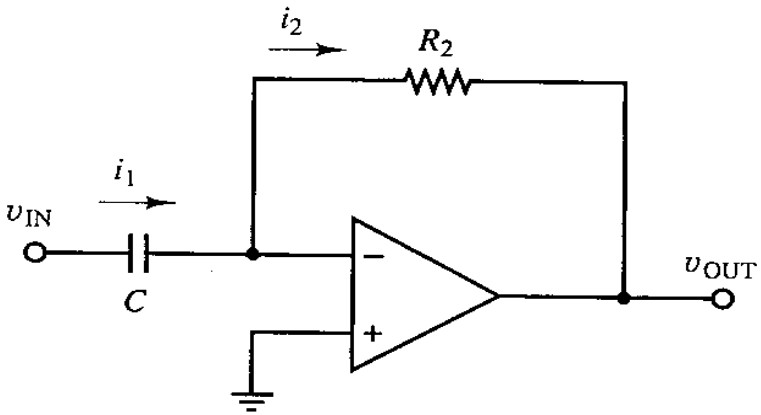
- The two op-amp configurations shown below perform the function of differentiation
  - The circuit on the left is the complement of the integrator circuit shown on slide 2-14, simply switching the capacitor and resistor
  - The circuit on the right differentiates by replacing the capacitor with an inductor
- For the circuit on the left we can write
  - $i_1 = C(dv_{IN}/dt) = i_2 = (0 - v_{OUT})/R2$ or

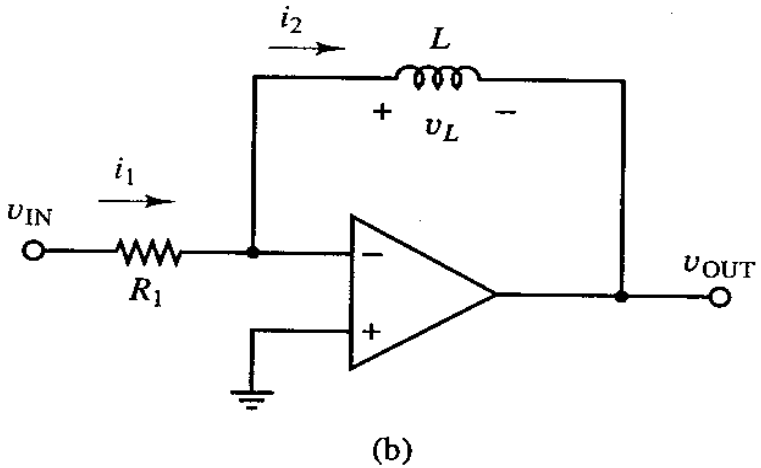
$$\mathbf{v_{OUT} = - R_2C\ (dv_{IN}/dt)}$$

- Similarly, for the circuit on the right we can obtain

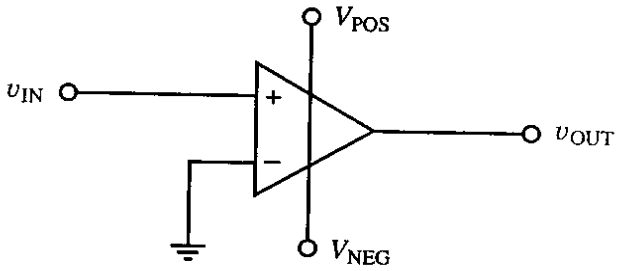
$$\mathbf{v_{OUT} = - (L/R_1)\ (dv_{IN}/dt)}$$

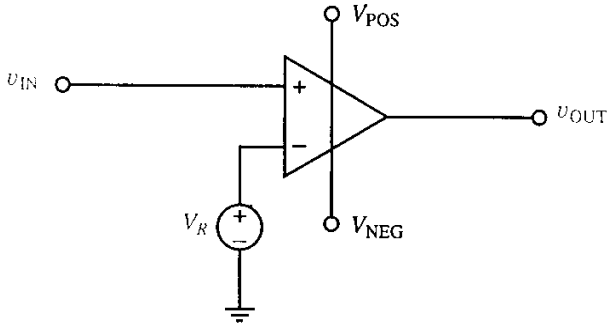
- By nature a differentiator is more susceptible to noise in the input than an integrator, since the slope of the input signal will vary wildly with the introduction of noise spikes.
- Do exercises 2.23 and 2.25.





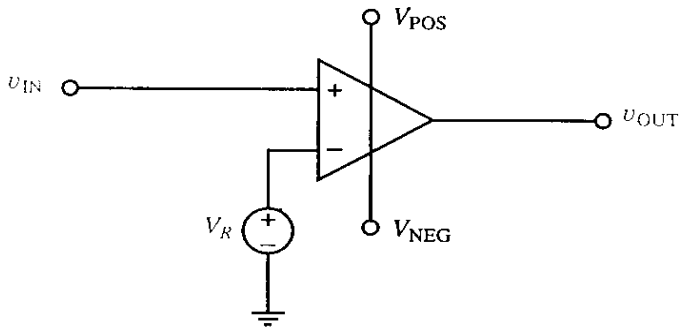
Non-Linear Op-amp Circuits

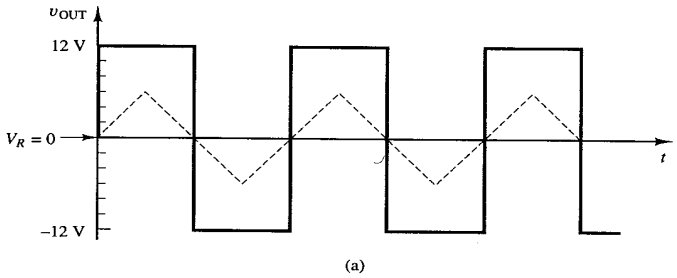




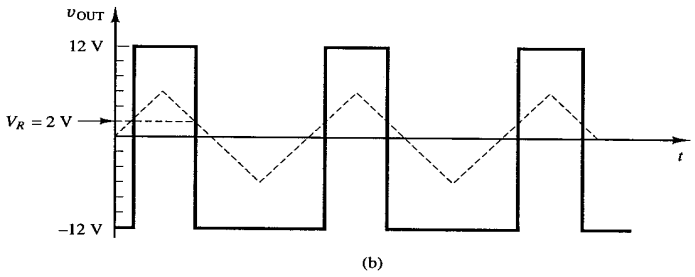
- Op-amps are sometimes used in non-linear open-loop configurations where the slightest change in v_{IN} will force the op-amp into saturation (V_{POS} or V_{NEG})
  - Such non-linear op-amp uses are often found in signal processing applications
- Two examples of such non-linear operation are shown at the left
  - Left-top is an **open-loop polarity indicator**
    - If v_{IN} is above or below GND by a few mV, v_{OUT} is forced to either positive or negative rail voltage
  - Left-bottom is an **open-loop comparator**
    - If v_{IN} is above or below V_R by a few mV, v_{OUT} is forced to the positive or negative rail voltage

Open-Loop Comparator (Example 2.8 in text)

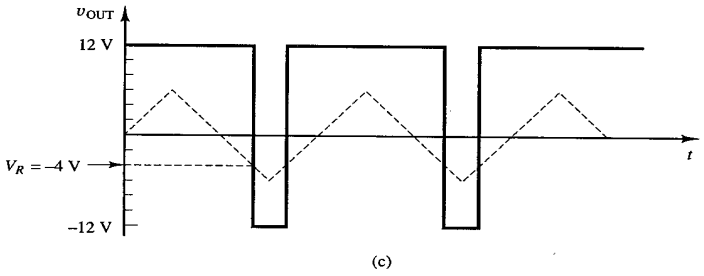




(a)



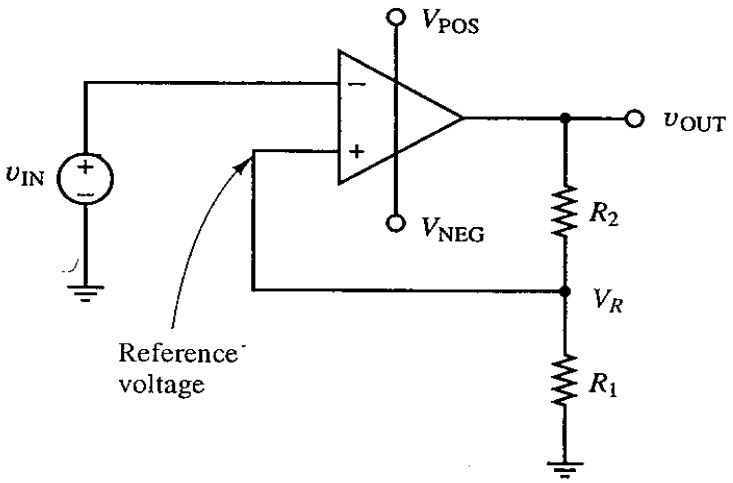
(b)

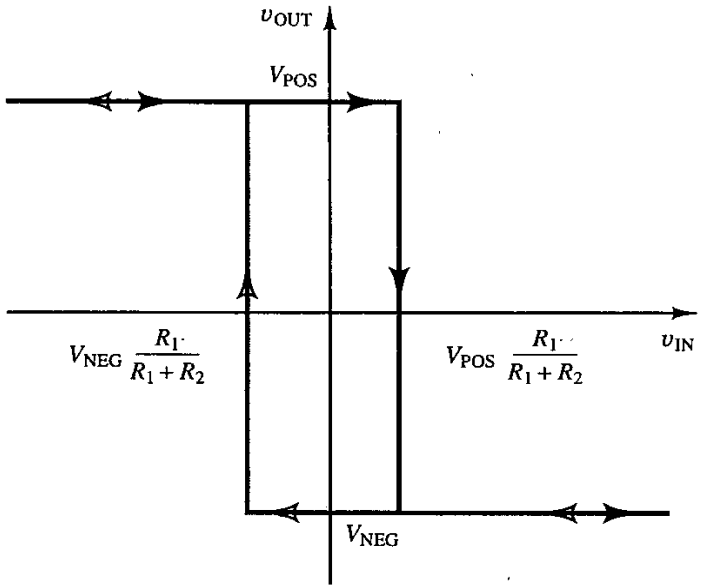


(c)

- Given the open-loop comparator shown at the left with V_{POS}= +12V and V_{NEG}= -12V, plot the output waveforms for V_R = 0, +2V, and –4V, assuming v_{IN} is a 6V peak triangle wave
- The solution is shown at the left
  - In (a) the output switches symmetrically from VPOS rail to V_{NEG} rail as the input moves above or below GND
  - In (b) the output switches between the rail voltages as the input goes above or below +2 V
  - In (c) the output switches between the rail voltages as the input varies above or below –4 V
  - The output becomes a pulse generator with adjustable pulse width
- Do Exercise 2.28.

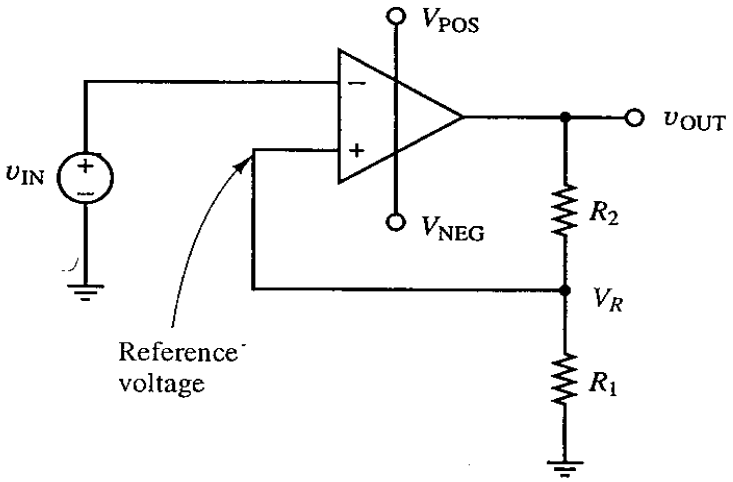
Schmitt Trigger Op-amp Circuit

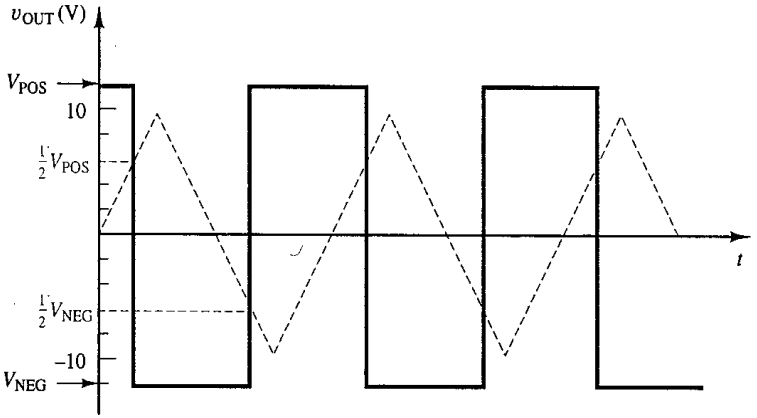




- The open-loop comparator from the previous two slides is very susceptible to noise on the input
  - Noise may cause it to jump erratically from + rail to – rail voltages
- The Schmitt Trigger circuit (at the left) solves this problem by using positive feedback
  - It is a comparator circuit in which the reference voltage is derived from a divided fraction of the output voltage, and fed back as positive feedback.
  - The output is forced to either V_{POS} or V_{NEG} when the input exceeds the magnitude of the reference voltage
  - The circuit will remember its state even if the input comes back to zero (has memory)
- The transfer characteristic of the Schmitt Trigger is shown at the left
  - Note that the circuit functions as an inverter with hysteresis
  - Switches from + to – rail when $v_{IN} > V_{POS}(R1/(R1 + R2))$
  - Switches from – to + rail when $v_{IN} < V_{NEG}(R1/(R1 + R2))$

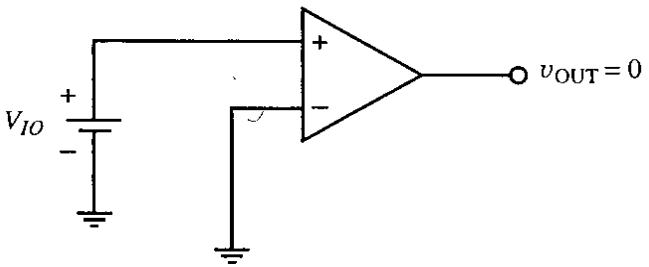
Schmitt Trigger Op-amp Example (2.9 in text)





- Assume that for the Schmitt trigger circuit shown at the left, $V_{POS}/_{NEG}$ = +/- 12 volts, R1 = R2, and v_{IN} is a 10V peak triangular signal. What is the resulting output waveform?
- Answer:
  - The output will switch between +12 and –12 volts
  - The switch to V_{NEG} occurs when v_{IN} exceeds V_{POS}(R1/(R1 + R2)) = +6 volts
  - The switch to V_{POS} occurs when v_{IN} drops below V_{NEG}(R1/R1 + R2)) = -6 volts
  - See waveforms at left
- Consider the case where we start out the Schmitt Trigger circuit with v_{IN} = 0 and v_{OUT} = 0 (a quasi-stable solution point for the circuit)
  - However, any small noise spike on the input will push the output either in the + or – direction, causing v+ to also go in the same direction, which will cause the output to move further in the same direction, etc. until the output has become either V_{POS} or V_{NEG}.

Non-Ideal Properties of Op-amps:
Output Saturation and Input-Offset Voltage



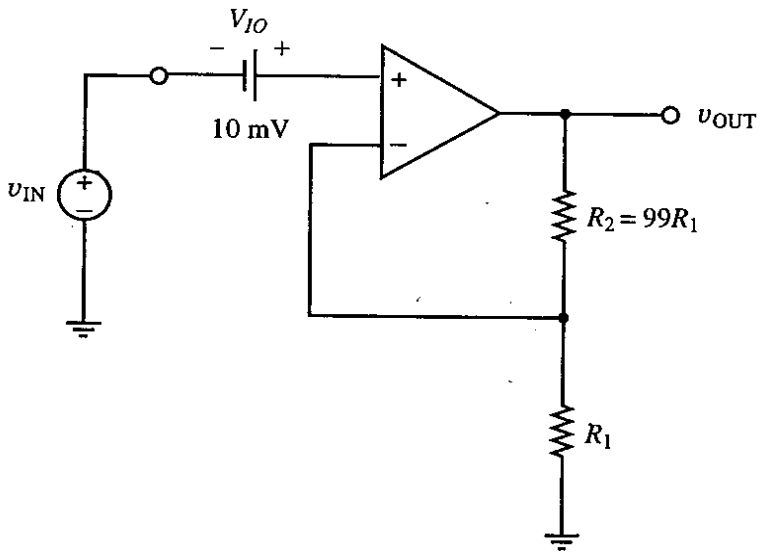
Output Saturation Voltage

- Although we have been assuming the op-amp will saturate at the supply voltages V_{POS} and V_{NEG}, in actual practice an op-amp circuit will saturate at somewhat lower than V_{POS} and higher than V_{NEG}, due to internal voltage drops in the design
  - Emitter-follower output stage (BJT design) will drop a V_{BE}
  - CMOS design will have a similar drop

Input-Offset Voltage

- We have been assuming v+ = v- when $v_{OUT} = 0$. In actual practice, however, there is usually a small input (or output) dc offset voltage in order to force v_{OUT} to 0, under open-loop operation.
  - The input-offset voltage (labeled $\boldsymbol{V_{IO}}$ in the figure at the left) can be positive or negative and is usually small (anywhere from 1 uV to 10 mV)

Input-Offset Voltage Effect on Output Voltage



- To examine the effect input-offset voltage has on the output voltage, consider the non-inverting op-amp
  - The gain of the op-amp is (R1 + R2)/R1 = 100
  - Assume the input voltage is modeled adequately by a source V_{IO} = +/- 10 mV
  - Then, we can write that the output voltage is given by

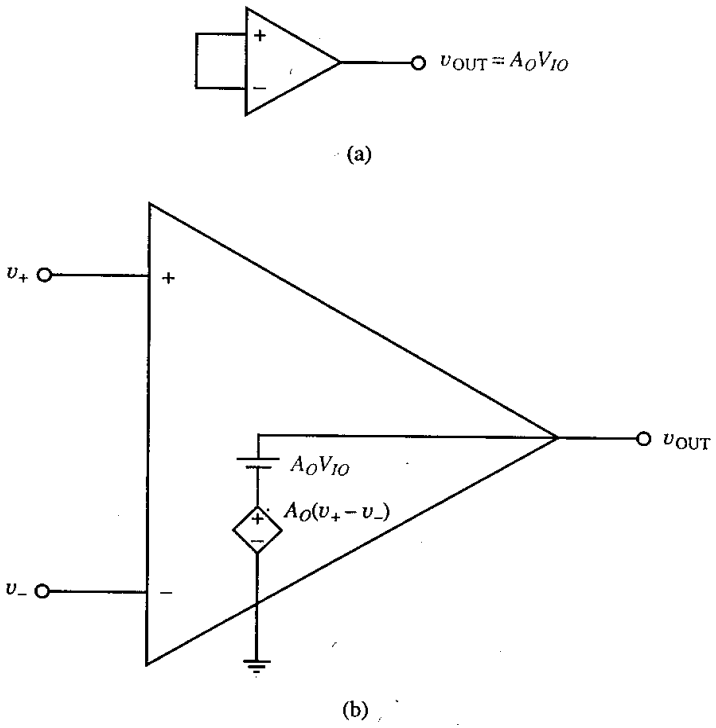
    $\mathbf{v_{OUT} = (v_{IN} + V_{IO})(R1 + R2)/R1}$

    $\mathbf{= 100\ v_{IN} +/- 1\ volt}$
  - Thus, a 10 mV input-offset causes a 1V offset in v_{OUT}
- *Exercise 2.32*: Show that the above equation applies even if V_{IO} is placed in series with the v- input, instead of the v+ input.
  - Using the virtual short condition, we can write

    $v_{OUT}[R1/(R1 + R2)] + V_{IO} = v_{IN}$ or

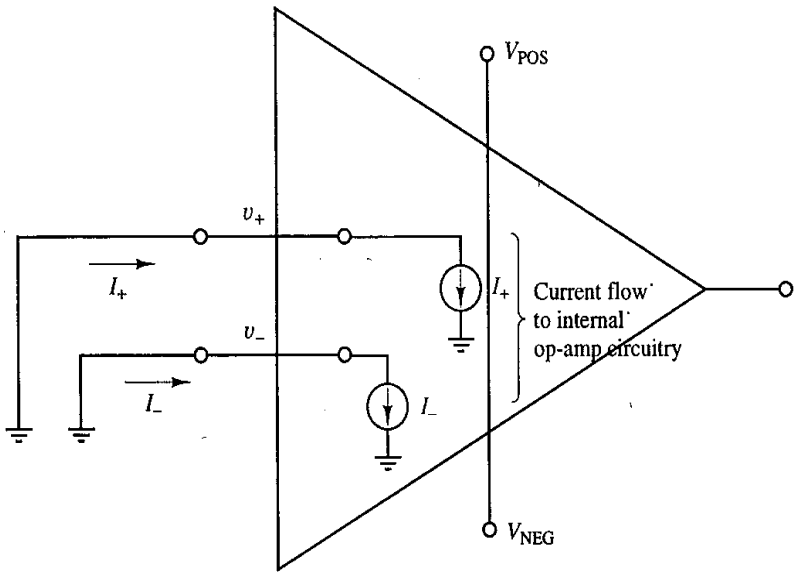
    $v_{OUT} = (R1 + R2)/R1)(v_{IN} + V_{IO})$ → same as above!
- *Exercise 2.33*: What is the output of an inverting op-amp if the effect of input offset is considered?
  - Based on the inverting op-amp circuit of slide 2-6, we can write $i_1 = (v_{IN} – V_{IO})/R1 = i_2 = (V_{IO} – v_{OUT})/R2$
  - or, $\mathbf{v_{OUT} = - (R2/R1)\ v_{IN} + V_{IO}\ (R1 + R2)/R1}$

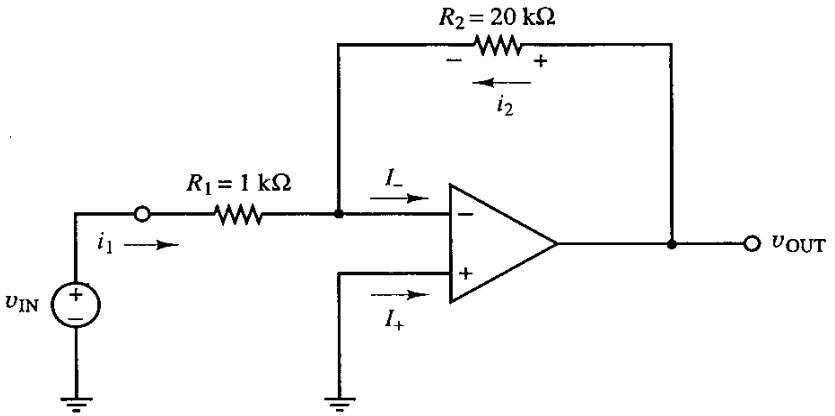
Output-Offset Voltage and Nulling Out Offset



- A parameter called the **output-offset voltage** may be used to represent the internal imbalance of an op-amp, rather than the input-offset voltage
  - The output-offset voltage is defined as the measured output voltage when the input terminals are shorted together, as shown at the left-top fig.
  - The output-offset voltage may be modeled by placing a voltage source A_0V_{IO} in series with the output voltage source $A_0(v_+ - v_-)$
    - Consequently, the output-offset voltage is essentially the input-offset voltage multiplied by the open loop gain.
  - Do exercise 2.34
- How can we correct for offset voltage?
  - Some op-amps provide two terminals (offset-null terminals) for adjusting out the offset voltage
    - A potentiometer is connected across the offset null terminals with the V_{NEG} supply voltage connected to the adjustable center tap
  - If the op-amp does not have an internal null adjustment provision, an external adjustment similar to that shown in Example 2.11 can be provided.
- Look at Exercise 2.36 (error in text)

Effect of Non-zero Input Bias Currents





- In practice op-amps do not actually have zero input currents, but rather have very small input currents labeled I_+ and I_- in the figure at the left
  - Modeled as internal current sources inside op-amp
  - I_+ and I_- are both the same polarity
    - e.g. if the input transistors are NPN bipolar devices, positive I_+ and I_- are required to provide base current
  - In order to allow for slightly different values of I_+ and I_-, we define the term I_{BIAS} as the average of I_+ and I_-

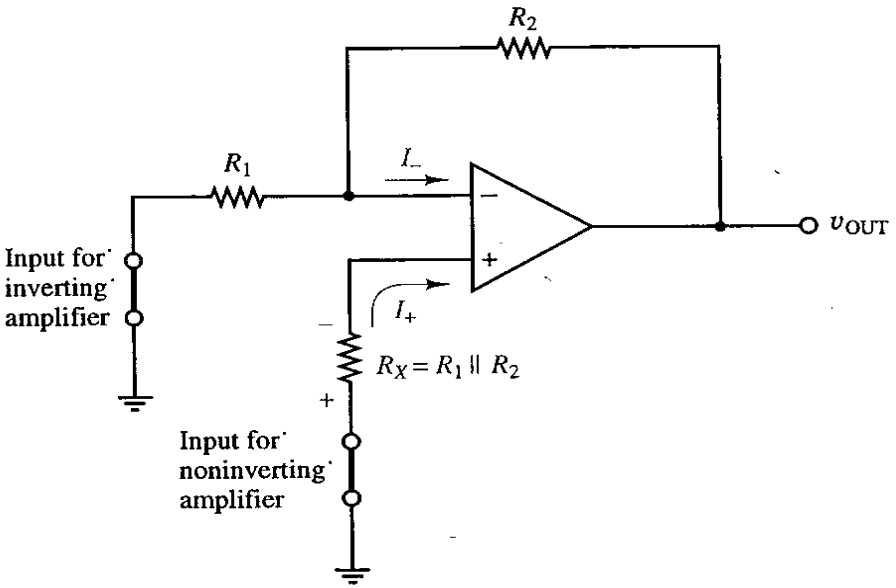
$$\mathbf{I_{BIAS} = \tfrac{1}{2}\,(I_+ + I_-)}$$

- Example: Given the op-amp shown in the bottom left figure, derive an expression for v_{out} that includes the effect of input bias currents
  - Assume $I_+ = I_- = 100$ nA
  - Using the virtual short condition and KCL, we can write $v_{IN}/R1 = I_- + (0\text{-}v_{OUT})/R2$ or

$$\mathbf{v_{OUT} = -\,(R_2/R_1)v_{IN} + I_-R_2}$$

  - Plugging in values gives $v_{OUT} = -\,20\,v_{IN} + 2$ mV
  - Do exercise 2.38, p. 77

Correcting for Non-zero Input Bias Current



- The effect of non-zero input bias current can be zero'ed out by inserting a resistor R_x in series with the V+ input terminal (as shown)
  - This same correction works for both inverting and non-inverting op-amps
  - We choose Rx such that the dc component on the output caused by I+ exactly cancels the dc component on v_{OUT} caused by I-
  - One can use either KCL (Kirchhoff's Current Law) or superposition to show that choosing Rx = R1 || R2 completely cancels out the dc effect of non-zero input bias current
- KCL Method (inverting op-amp at left)
  - v_{IN} is applied to R1 and Rx is grounded
  - $v_- = v_+ = 0 - I_+R_x$ due to virtual short
  - Apply KCL to v+ input:

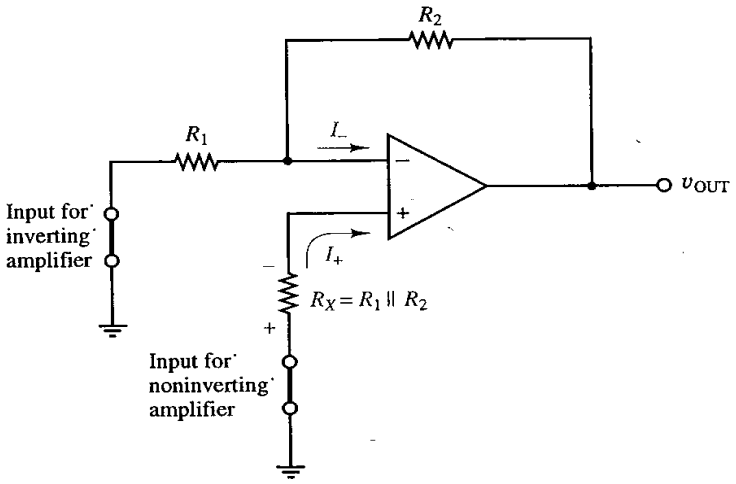
    $(v_{IN} - v_-)/R1 = I_- + (v_- - v_{OUT})/R2$
  - Solve for v_{OUT} and substitute $-I_+R_x$ for v_-

$v_{OUT} = - (R2/R1)\, v_{IN} + I_-R2 - I_+R_x(R1 + R2)/R1$

  - Setting the dc bias terms equal yields

Rx = R1 || R2 = R1 R2/(R1 + R2)

Input Offset Current Definition



- Non-zero input bias currents I+ and I- may not always be equal (some opamps)
  - Variation in bipolar transistor beta may cause base currents to non-track, or perhaps there are circuit design issues causing non equal offset I
- We define a parameter "input offset current"

  $I_{IO} = I_+ - I_-$
  - Typical values of I_{IO} are 5-10% (of I-) although it can be as high as 50%
- Example 2.13 based on figure at left
  - R1 = 1K, R2 = 20K ohms
  - Assuming Ibias = 1 uA and I_{IO} = 100 nA, find I+, I-, and the effect of I_{IO} on vout
  - Since $(I_+ + I_-)/2$ = 1 uA and $I_+ - I_-$ = 0.1uA, we can solve for I+ = 1.05 uA and I- = 0.95 uA
  - Using the expression for Vout from slide 2-26 with Vin = 0 and Rx = R1 || R2 gives us
  - $v_{OUT} = R2 (I_- - I_+) = -I_{IO} R2 = -2$ mV
- Do Exercise 2.40

Slew Rate Limitation in an Op-amp

- A real op-amp is limited in its ability to respond instantaneously to an input signal with a high rate of change of its input voltage. This limitation is called the **slew rate**, referring to the maximum rate at which the output can be "slewed".
  - Typical slew rates may be between 1–10 V/μs = 1E6 – 1E7 V/s
  - Max slew rate is a function of the device performance of the op-amp components & design
  - If the input is driven above the slew rate limit, the output will exhibit non-linear distortion
- Slew rate limitation behavior: (Example 2.14):
  - Assume an inverting op-amp with a gain of –10 has a max slew rate of 1 V/μs and is driven by a sinusoidal input with a peak of 1V. At what input frequency will the output start to show slew rate limitation?
    - Output has a peak of 10 volts since gain is –10 and input peak is 1 volt
    - If the input is given by v_{IN} = Vo sin ωt, the max slope will occur at t=0 and will be given by

      d (Vo sin ωt)/dt |(t=0) = ωVo = 2πf Vo
  - The max frequency is therefore given by

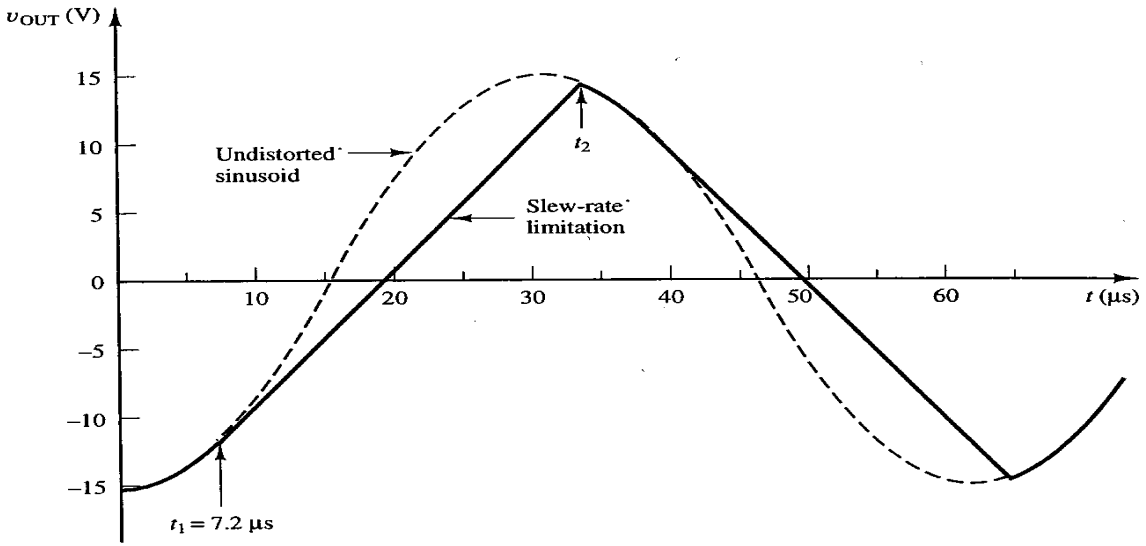
    $\mathbf{f_{max} = slew\ rate/2\pi V_o}$ = 1E6 V/s / 2π 10V = ~ 16 kHz
  - Note: This surprisingly low max frequency is directly proportional to the slew rate limit spec and inversely proportional to the peak output voltage!

Slew Rate Limitation in an Op-amp

Exceeding the slew rate limitation (Example 2.14b):

- If the inverting op-amp from 2.14a (with gain = –10 and slew rate = 1 V/μs) is driven by a 16 kHz sinusoidal input with a peak of 1.5V, what is the effect on the output waveform?
  - Since we are now exceeding the slew rate limit, the output will be distorted
  - Let v_{OUT} = - Vo cos ωt (for visual simplicity) where Vo = 10 x 1.5V = 15V
  - Then $dv_{OUT}/dt = \omega Vo \sin \omega t$
  - Above some t = t_1 the slew rate will limit the output response

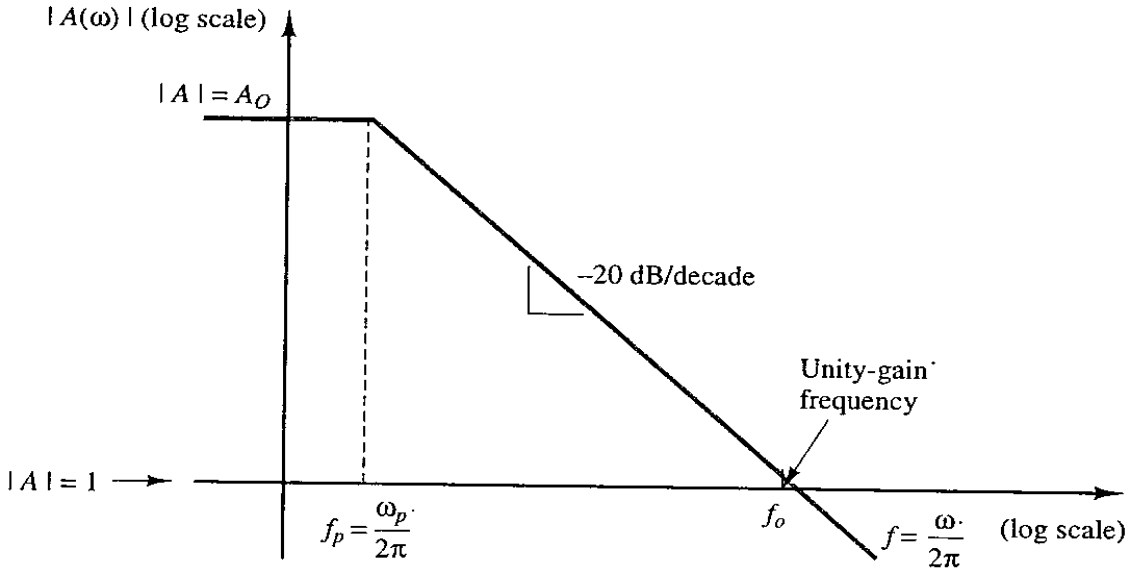
    $t_1 = (1/\omega) \sin^{-1}$ (slew rate/ωVo) = (1/2π 16 kHz) $\sin^{-1}$ (1E6 /2π 16 kHz x 15V) = 7.2 μs
  - The resulting waveform is shown below. At t_1 the slew-limited output can't keep up with the input until it catches up at t_2, when the cycle starts all over again.



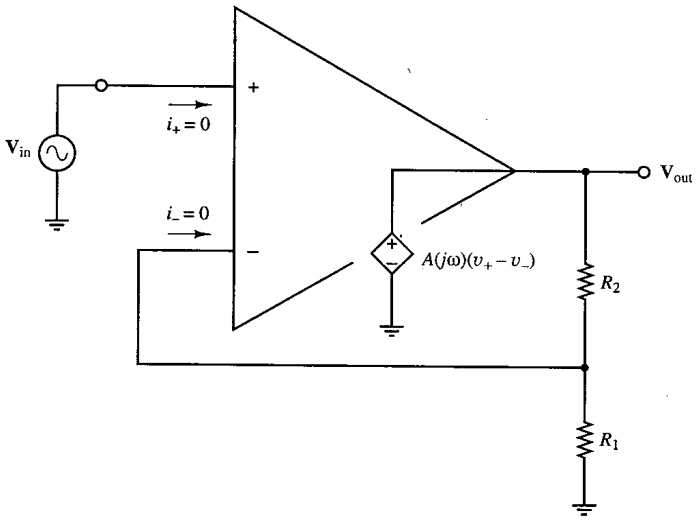
Frequency Response of an Op-amp

- An open-loop op-amp has a constant gain Ao only at low frequencies, and a continuously reducing gain at higher frequencies due to internal device and circuit inherent limits.
  - For a single dominant pole at freq f_p, the frequency-dependent gain $A(j\omega)$ can be written as

    $A(j\omega) = Ao/[1 + j\omega/\omega_p] = Ao/[1 + jf/ f_p]$ where $\omega_p = 2\pi f_p$
  - the gain rolls off at 20dB/decade for frequencies above f_p, as shown below
- An op-amp may have additional higher frequency poles, as well, but is often described over a large frequency range by the dominant pole (as assumed in the figure below)
- The unity gain frequency f_o is defined as the frequency where the gain = 1
  - For the single dominant pole situation assumed in the figure below, f_o can be found by extrapolating the 20 dB/decade roll-off to the point where the gain is unity.



Frequency-Dependent Closed-Loop Gain



- The effect of the frequency-dependent open-loop gain on the closed-loop gain can easily be found by deriving $v_{OUT}(j\omega)$ as a function of the open-loop gain $A(j\omega)$ in the op-amp configuration shown at the left

  $v_{OUT} = A(j\omega)\ (v+ - v-)$

  $= A(j\omega)\ [v_{IN} - v_{OUT}(R1/(R1 + R2))]$, or

  $v_{OUT} = A(j\omega)/[1 + A(j\omega)\beta]$ where

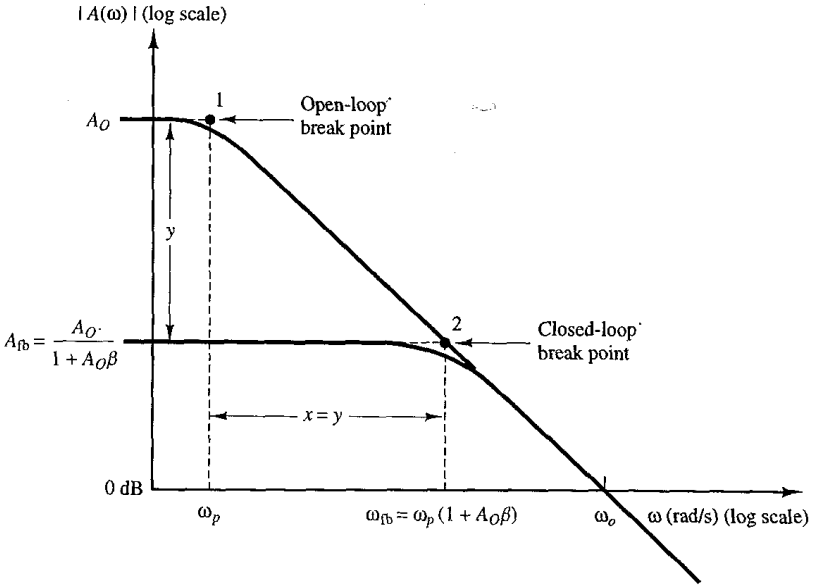
  $\beta = R1 / (R1 + R2)$ is the closed-loop feedback function

  - Substituting A(jw) into the above equation gives us the complete frequency dependent result for the closed loop gain

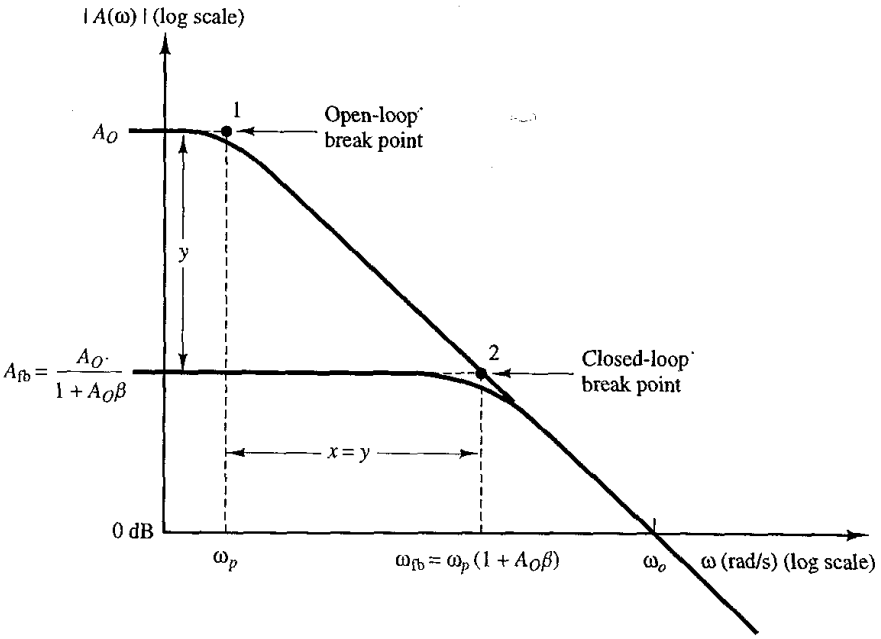
    $v_{OUT}/v_{IN} = Ao/[1 + Ao\beta + j\omega/\omega_p]$

    $= [Ao/(1 + Ao\beta)]/[1 + j\omega/\omega_p(1 + Ao\beta)]$

- The dc gain is given by
  - $Ao/(1 + Ao\beta) = \sim 1/\beta = (R1 + R2)/R1$
- The closed-loop response is seen to contain a single pole at $\omega_{fb} = \omega_p(1 + Ao\beta) >> \omega_p$
  - **Closed-loop BW = ~ $A_o\beta$ x open-loop BW**



Gain-Bandwidth Product



- Multiplication of the closed-loop BW by the closed-loop gain gives us

  $[Ao/(1+Ao\beta)]\omega_{fb} = [Ao/(1+Ao\beta)]\omega_p(1+Ao\beta)$

  $= Ao\omega_p$

  - which is the open-loop gain-BW product
- For the assumption of a single dominant pole and very high Ao, the gain-bandwidth product is a constant
- Unity-gain frequency ω_o ($= 2\pi f_o$) is the freq where the op-amp response extrapolates to a gain of 1
  - we can show that $\omega_o = A_o\omega_p$ (for a system with a single dominant pole)

Op-amp Output Current Limit:

- **A typical op-amp contains circuitry to limit the output current to a specified maximum in order to protect the output stage from damage**
  - **If a low value load impedance is utilized, the output current limit may be reached before the output saturates at the rail voltage, forcing the op-amp to lower gain**
  - **See Example 2.15**

UNIT - IV

STABILITY AND FREQUENCY COMPENSATION

Introduction

- **IN THIS CHAPTER YOU WILL LEARN**
  - The design and analysis of the two basic CMOS op-amp architectures: the two-stage circuit and the single-stage, folded cascode circuit.
  - The complete circuit of an analog IC classic: the 741 op-amp. Though 40 years old, the 741 circuit includes so many interesting and useful design techniques that its study is still a must.
  - Applications of negative feedback within op-amp circuits to achieve bias stability and increased CMRR.

Introduction

- **IN THIS CHAPTER YOU WILL LEARN**
  - How to break a large analog circuit into its recognizable blocks, to be able to make the analysis amendable to a pencil-and-paper approach – which is the best way to learn design.
  - Some of the modern techniques employed in the design of low-voltage single-supply BJT op amps.
  - Most importantly, how the different topics we learned about in the preceding chapters come together in the design of the most important analog IC – the op amp.

12.1. The Two Stage CMOS Op Amp

- Two-stage op amp is shown in Figure 12.1.
- It was studied in Section 8.6.1 as example of multi-stage CMOS amplifier.

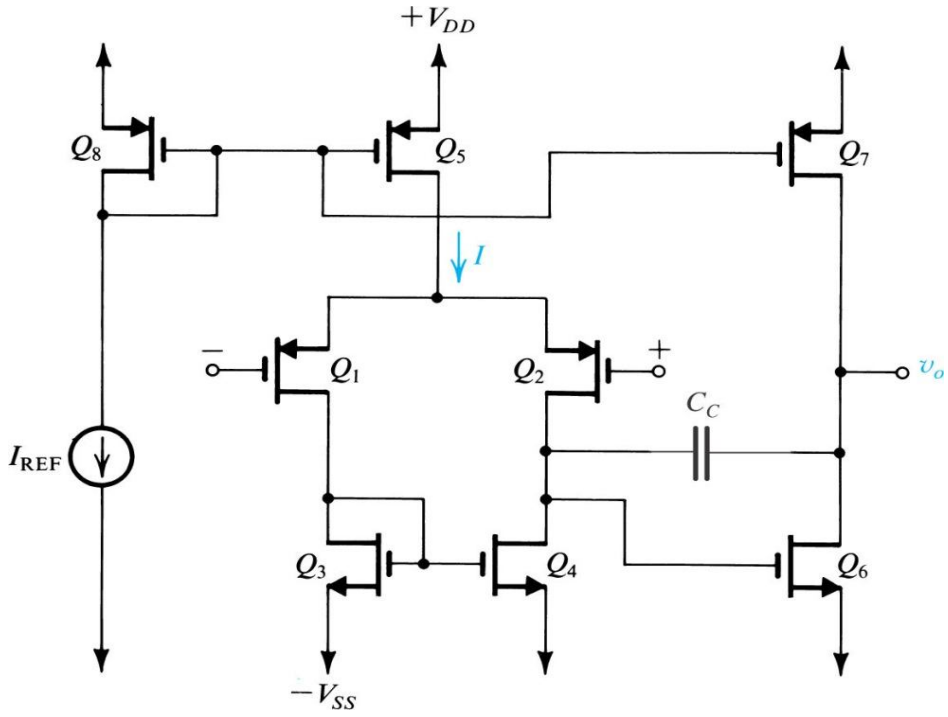


Figure 12.1 The basic two-stage CMOS op-amp configuration.

12.1.1. The Circuit

- Two Stages:
  - Differential Pair Q_1/Q_2.
    - Biased by current source Q_5
    - Fed by a reference current I_{REF}
  - Current Mirror Load Q_3/Q_4.
    - Frequency Compensation
- Voltage Gain 20V/V to 60V/V
- Reasonable Common-Mode Rejection Ratio (CMRR)

12.1.1. Input Common-Mode Range and Output Swing

(eq12.1) dc offset elimination: $$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$

(eq12.2) common-mode input: $$V_{ICM} \geq -V_{SS} + V_{tn} + V_{OV3} - |V_{tp}|$$

(eq12.3) common-mode input: $$V_{ICM} \leq -V_{DD} + |V_{OV5}| - |V_{tp}| - |V_{OV1}|$$

(eq12.4) $$-V_{SS} + V_{OV3} + V_{tn} - |V_{tp}| \leq V_{ICM} - |V_{tp}| - |V_{OV1}| - |V_{OV5}|$$

(eq12.5) $$-V_{SS} + V_{OV6} \leq v_O \leq V_{DD} - |V_{OV7}|$$

12.1.3. Voltage Gain

- Consider simplified equivalent circuit model for small-signal operation of CMOS amplifier.
  - Figure 12.2.
- Input resistance is practically infinite (R_{in}).
- First-stage transconductance (G_{m1}) is equal to values for Q_1 and Q_2.
- Since Q_1 and Q_2 are operated at equal bias currents (I/2) and equal overdrive voltages, equation (12.7) applies.

12.1.1. Input Common-Mode Range and Output Swing

(eq12.7) stage-one transconductance: $G_{m1} = \frac{2(I/2)}{V_{OV1}} = \frac{I}{V_{OV1}}$

(eq12.8) $R_1 = r_{o2} \,||\, r_{o4}$

(eq12.9) $r_{o2} = |V_{A2}| / (I/2)$

(eq12.10) $r_{o4} = |V_{A4}| / (I/2)$

(eq12.11) gain of first stage: $A_1 = -G_{m1} R_1$

(eq12.12) gain of first stage: $A_1 = -gm1(r_{o2} \,||\, r_{o4})$

(eq12.13) gain of first stage: $A_1 = -\frac{2}{V_{OV1}} I \left(\frac{1}{|V_{A2}|} + \frac{1}{|V_{A4}|} \right)$

(eq12.14) stage-two transconductance: $G_{m2} = g_{m6} = \dfrac{2I_{D6}}{V_{OV6}}$

(eq12.15) $R_2 = r_{o6} \,||\, r_{o7}$

(eq12.16) $r_{o6} = |V_{A6}| \,/\, I_{D6}$

(eq12.17) $r_{o4} = |V_{A7}| \,/\, I_{D7} = |V_{A7}| \,/\, I_{D6}$

(eq12.18) voltage gain of second stage: $A_2 = -G_{m2}R_2$

(eq12.19) voltage gain of second stage: $A_2 = -g_{m6}\left(r_{o6} \,||\, r_{o7}\right)$

(eq12.20) voltage gain of second stage: $A_2 = -\dfrac{2}{V_{OV6}} \,/\, \left(\dfrac{1}{V_{A6}} + \dfrac{1}{|V_{A7}|}\right)$

(eq12.21) overall dc gain: $A_v = G_{m1}R_1G_{m2}R_2$

(eq12.22) overall dc gain: $A_v = g_{m1}\left(r_{o2} \,||\, r_{o4}\right)g_{m6}\left(r_{o6} \,||\, r_{o7}\right)$

(eq12.21) output resistance: $R_o = r_{o6} \,||\, r_{o7}$

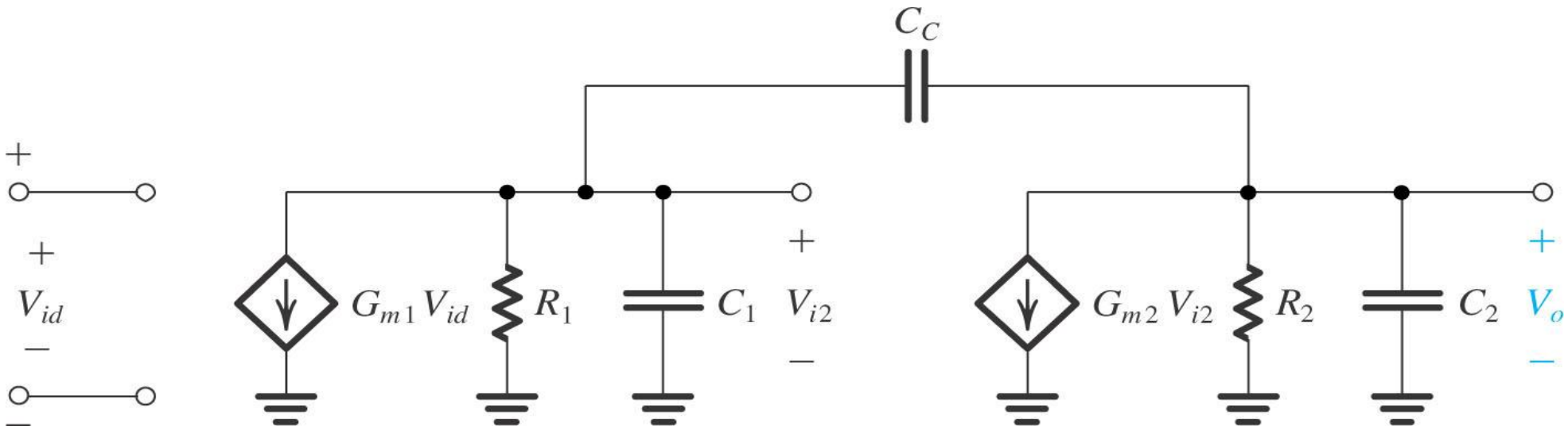


Figure 12.2: Small-signal equivalent circuit for the op amp in Fig. 12.1.

12.1.4. Common-Mode Rejection Ratio

- CMRR of two-stage amplifier is determined by first stage
  - CMRR = $[g_{m1}(r_{o2} \| r_{o4})[2g_{m3}R_{SS}]$
- RSS is output resistance of the bias source Q_5
- CMRR is of the order of $(g_m r_o)^2$
  - This is high.
- $G_m r_o$ is proportional to V_A/V_{OV}
- CMRR is increased if long channels are used.

12.1.5. Frequency Response

(eq12.25) $C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$

(eq12.26) $C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$

(eq12.27) $f_{P1} = \frac{1}{2\pi R_1 G_{m2} R_2 C_C}$

(eq12.28) $f_{P2} = \frac{G_{m2}}{2\pi C_2}$

(eq12.29) $f_{P2} = \frac{G_{m2}}{2\pi C_C}$

(eq12.30) $f_t = |A_v| f_{P1}$

(eq12.31) $f_t = \frac{G_{m1}}{2\pi C_C}$

(eq12.32) $\frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_2}$

(eq12.33) $G_{m1} < G_{m2}$

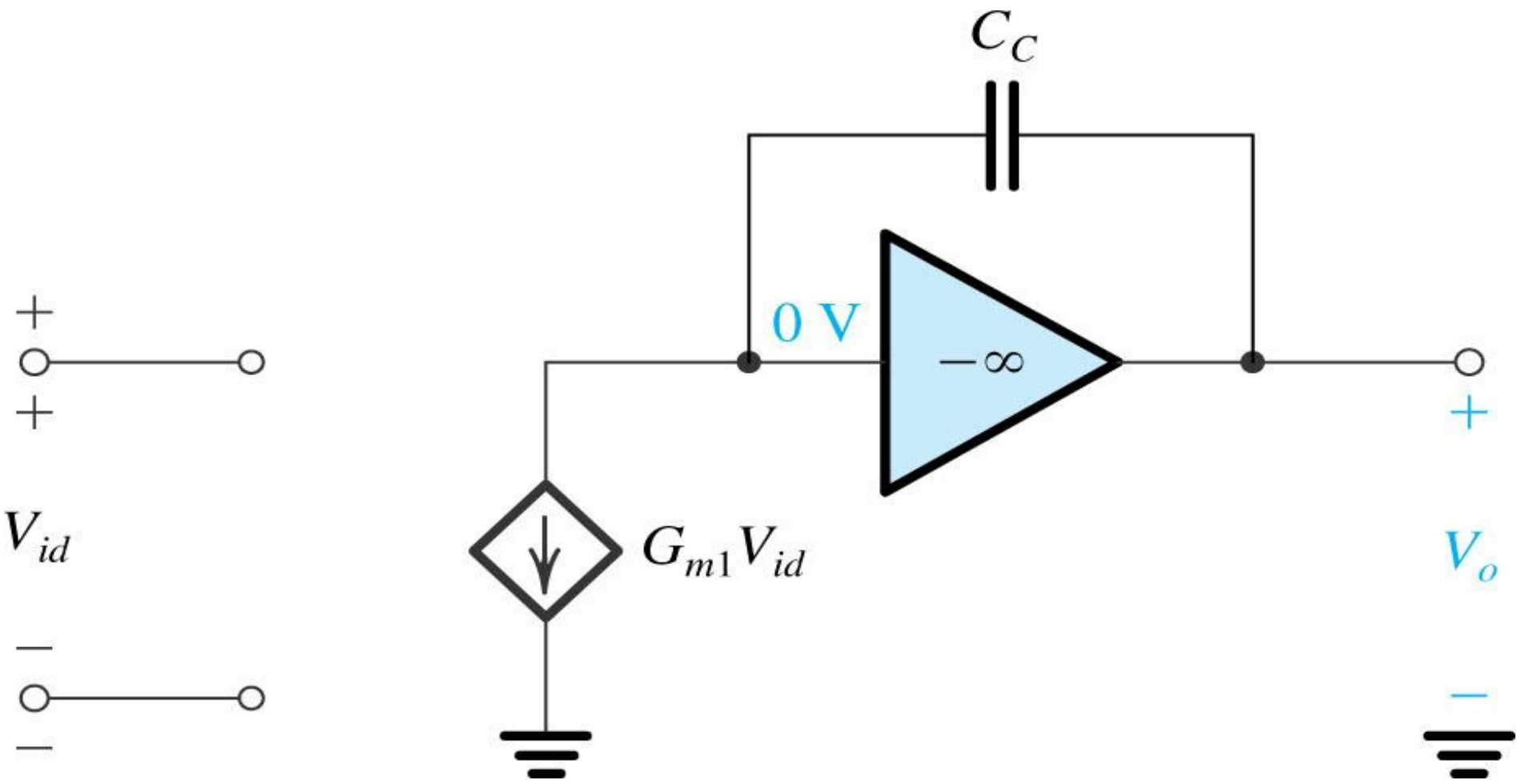
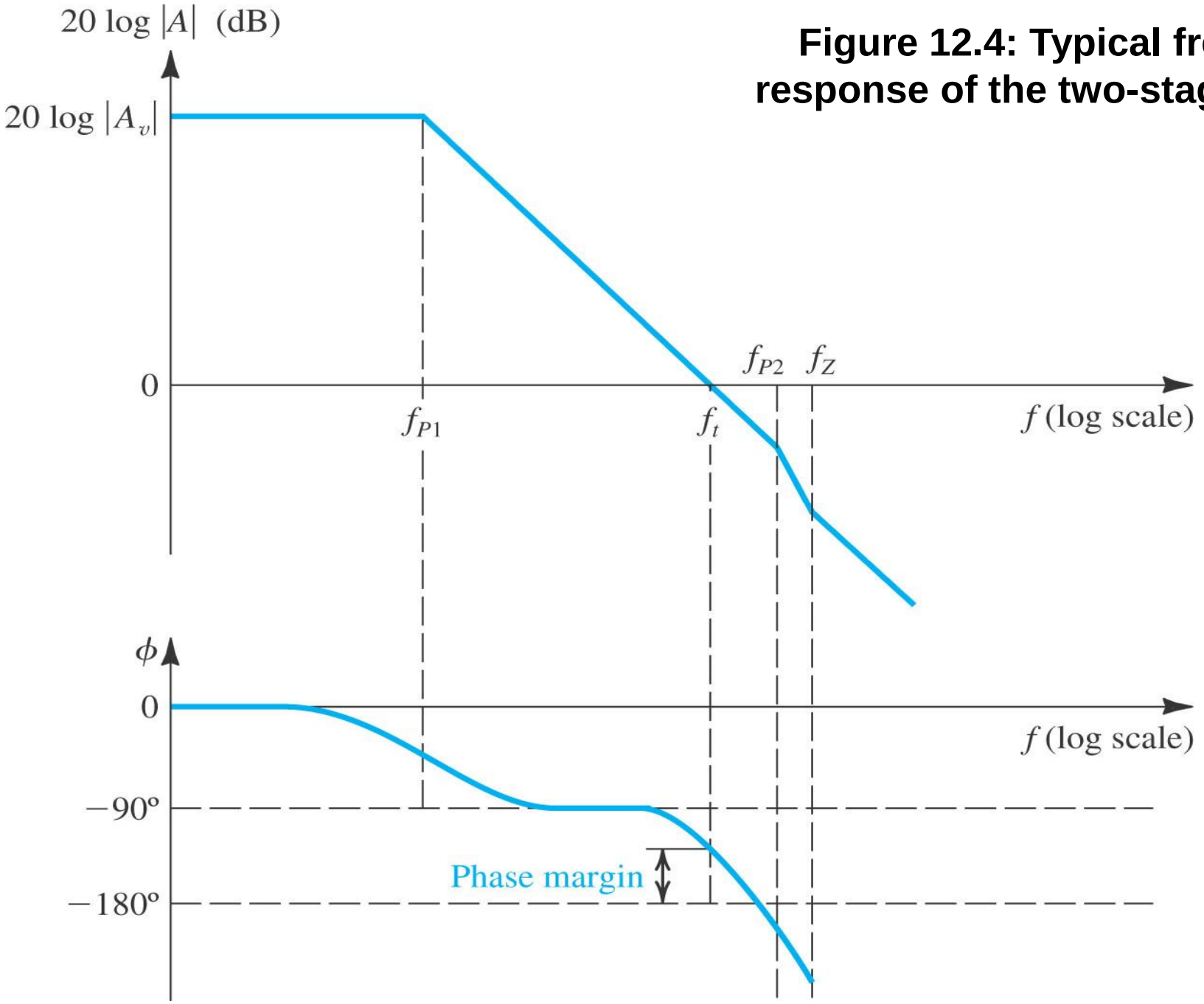


Figure 12.3 An approximate high-frequency equivalent circuit of the two-stage op amp. This circuit applies for frequencies $f \gg f_{P1}$.

Figure 12.4: Typical frequency response of the two-stage op amp.



12.1.5. Frequency Response

(eq12.34) $$\phi_{P2} = -\tan^{-1}\left(\frac{f_t}{f_{P2}}\right)$$

(eq12.36) $$\phi_{Z} = -\tan^{-1}\left(\frac{f_t}{f_{Z}}\right)$$

(eq12.37) $$\phi_{total} = 90^{O} + \tan^{-1}\left(\frac{f_t}{f_{Z}}\right) + \tan^{-1}\left(\frac{f_t}{f_{Z}}\right)$$

(eq12.38) $$\text{phase margin} = 180^{O} - \phi_{total}$$

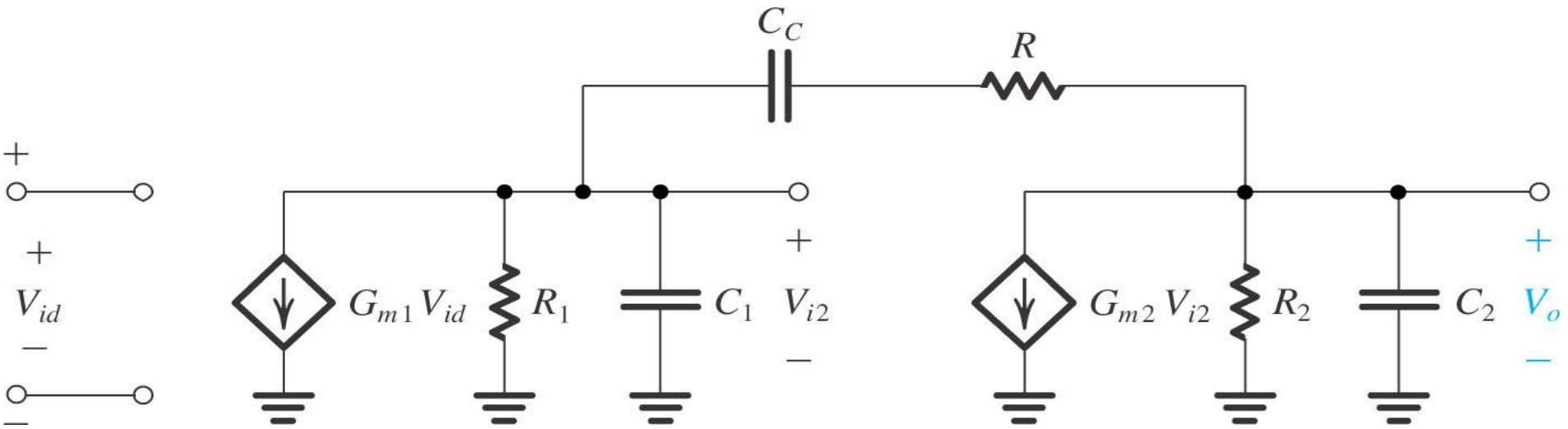


Figure 12.5: Small-signal equivalent circuit of the op amp in Fig. 12.1 with a resistance *R* included in series with *CC*.

12.1.6. Slew Rate

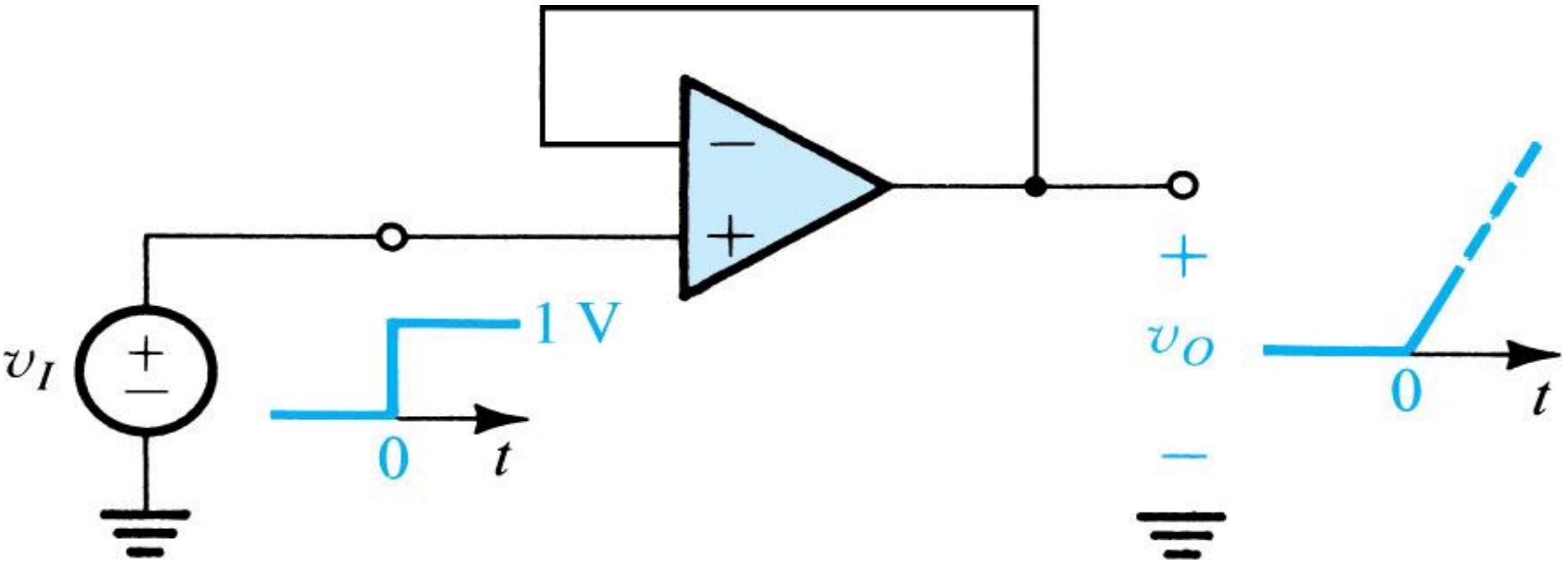


Figure 12.6: A unity-gain follower with a large step input. Since the output voltage cannot change immediately, a large differential voltage appears between the op-amp input terminals.

12.1.6. Slew Rate

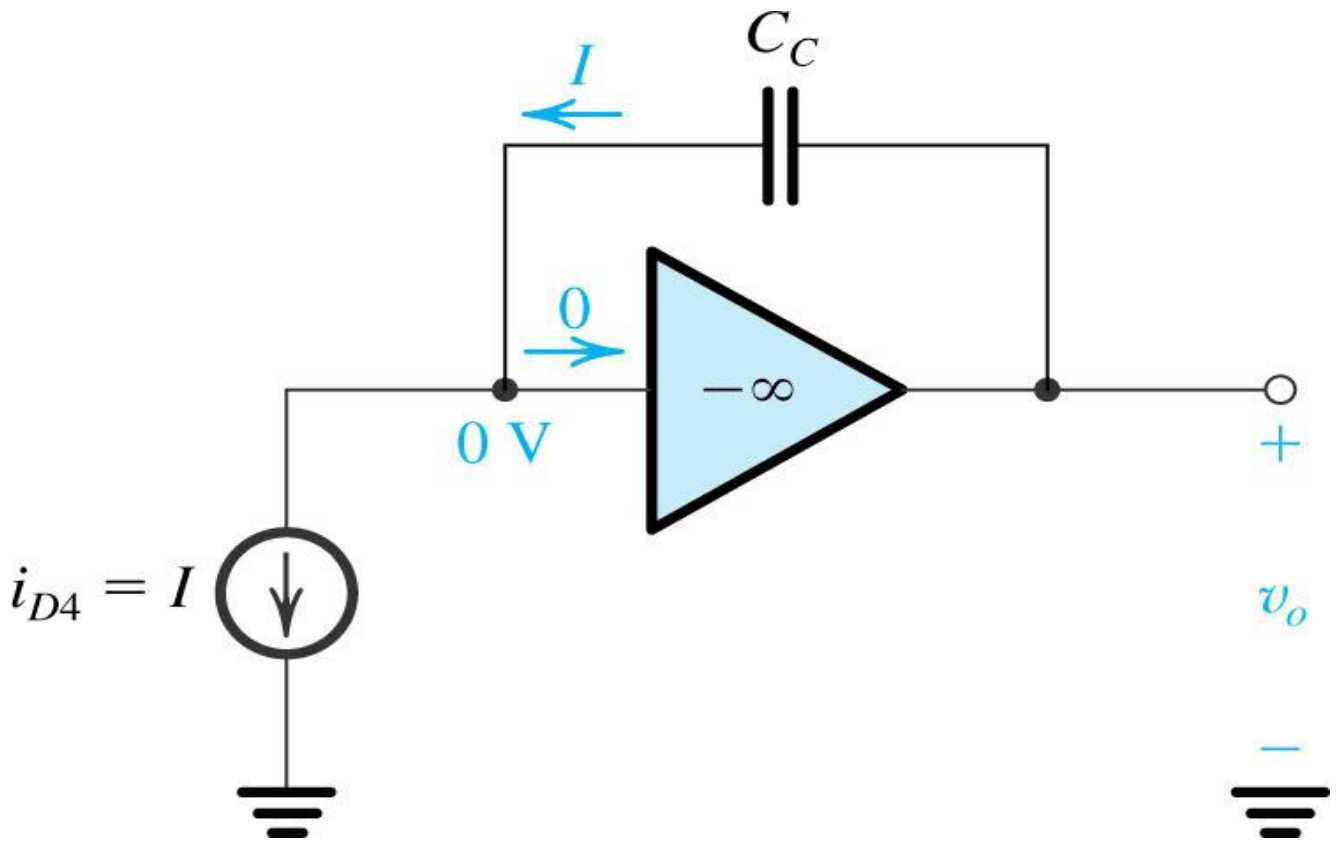


Figure 12.7: Model of the two-stage CMOS op-amp of Fig. 12.1 when a large differential voltage is applied.

Relationship Between SR and f_t

- Simple relationship exists between unity-gain bandwidth (f_t) and slew rate.
  - Equations (12.31) through (12.40).
- $SR = 2\pi f_t V_{OV}$
- Slew rate is determined by the overdrive voltage at which first-stage transistors are operated.
- For a given bias current I, a larger V_{OV} is obtained if Q_1 and Q_2 are p-channel devices.

12.1.7. Power Supply Rejection Ratio

- **mixed-signal circuit** – IC chip which combines analog and digital devices.
  - Switching activity in digital portion results in ripple within power supplies.
  - This ripple may affect op amp output.
- **power-supply rejection ratio** – the ability of a circuit to eliminate any ripple in the circuit power supplies.
  - PSRR is generally improved through utilization of capacitors.

(eq12.42) $PSRR^{+} \equiv A_d \,/\, A^{+}$

(eq12.43) $PSRR^{-} \equiv A_d \,/\, A^{-}$

(eq12.44) $A^{+} \equiv v_o \,/\, v_{dd}$

(eq12.45) $A^{-} \equiv v_o \,/\, v_{ss}$

(eq12.46) $$v_o = v_{ss} \frac{r_{o7}}{r_{o6} + r_{o7}}$$

(eq12.47) $$A^{-} \equiv v_o \,/\, v_{ss} = \frac{r_{o7}}{r_{o6} + r_{o7}}$$

(eq12.48) $$PSRR^{-} \equiv A_d \,/\, A^{-} = g_{m1}\left(r_{o2} \,||\, r_{o4}\right) g_{m6} r_{o6}$$

12.1.8. Design Trade-Offs

- The performance of the two-stage CMOS amplifier are primarily determined by two design parameters:
  - Length (L) of channel of each MOSFET
  - Overdrive voltage (V_{OV}) at which transistor is operated.
- **transition frequency** (f_T) – is defined below. It determined high-frequency operation.

$$\text{(eq12.49)}\quad f_T = g_m \,/\left[2\pi\left(C_{gs} + C_{gd}\right)\right]$$

12.2. The Folded-Cascode CMOS Op Amp

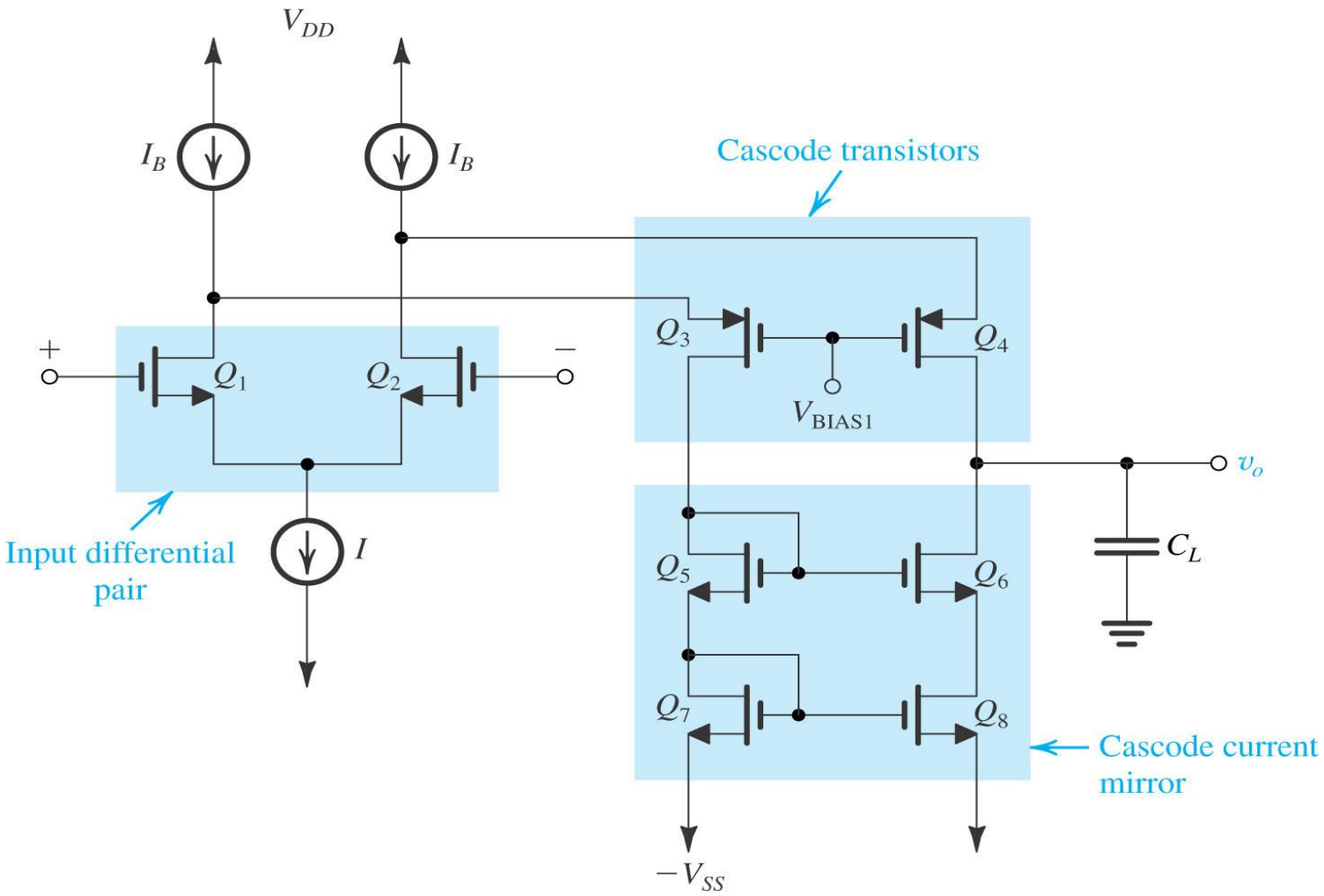


Figure 12.8: Structure of the folded-cascode CMOS op amp.

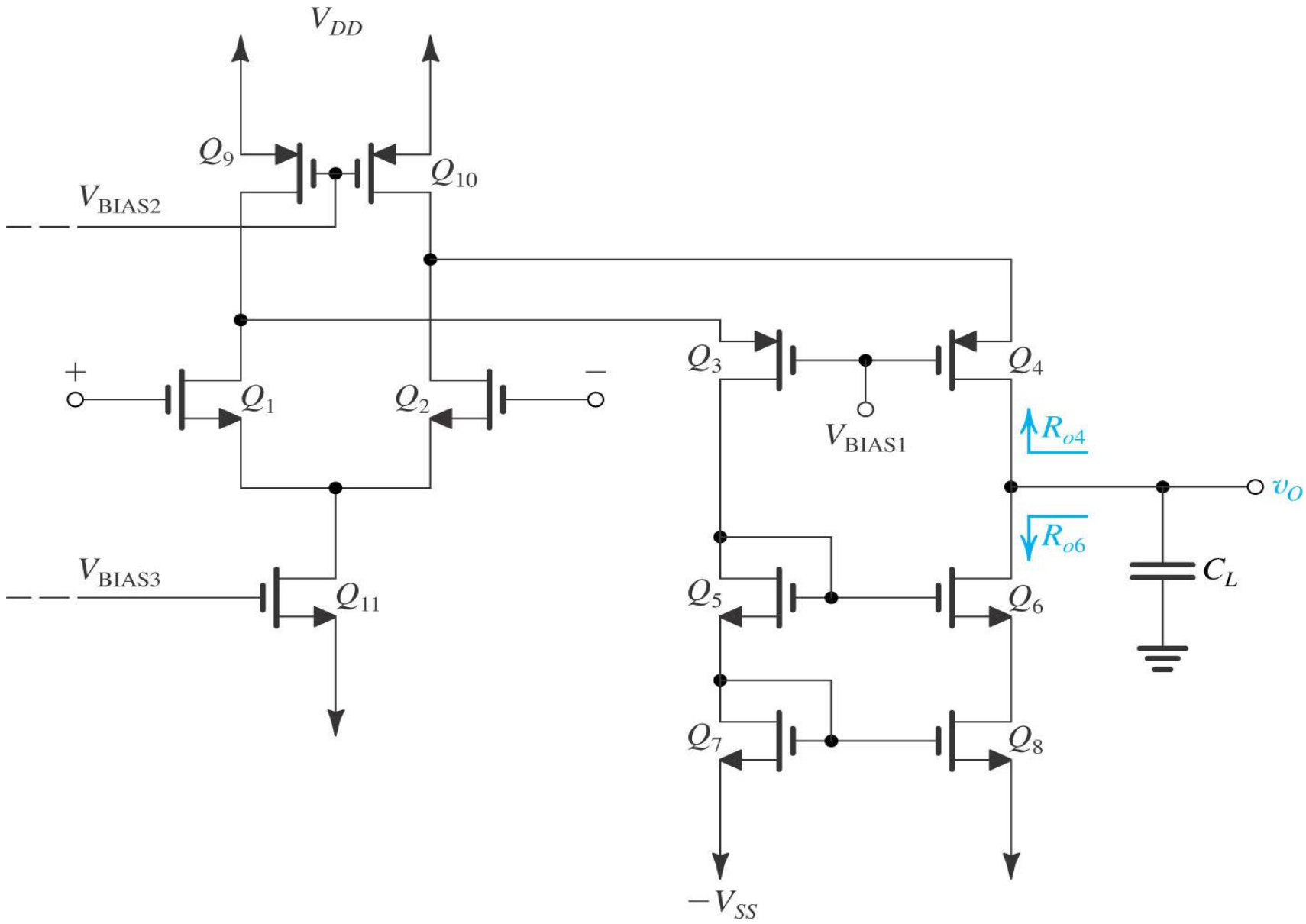


Figure 12.9: A more complete circuit for the folded-cascode CMOS amplifier of Fig. 12.8.

12.2.2. Input Common-Mode Range and Output Swing

(eq12.51) $$V_{ICM\max} = V_{DD} - \left|V_{OV9}\right| + V_{tn}$$

(eq12.52) $$V_{ICM\min} = -V_{SS} + V_{OV11} + V_{OV1} + V_{tn}$$

(eq12.53) $$-V_{SS} + V_{OV11} + V_{OV1} + V_{tn} \le V_{ICM} \le V_{DD} - \left|V_{OV9}\right| + V_{tn}$$

(eq12.54) $$V_{BIAS} = V_{DD} - \left|V_{OV10}\right| - V_{SG4}$$

(eq12.55) $$v_{O\max} = V_{DD} - \left|V_{OV10}\right| - \left|V_{OV4}\right|$$

(eq12.56) $$v_{O\min} = -V_{SS} + V_{OV7} + V_{OV5} + V_{tn}$$

12.2.3. Voltage Gain

(eq12.57) $G_m = g_{m1} = g_{m2}$

(eq12.58) $G_m = \dfrac{2(I/2)}{V_{OV1}} = \dfrac{I}{V_{OV1}}$

(eq12.59) $R_o = R_{o4} \,||\, R_{o6}$

(eq12.60) $R_{o4} = g_{m4} r_{o4} \left(r_{o2} \,||\, r_{o10}\right)$

(eq12.61) $R_{o6} = g_{m6} r_{o6} r_{o8}$

(eq12.62) $R_o = \left[g_{m4} r_{o4} \left(r_{o2} \,||\, r_{o10}\right)\right] \,||\, \left[g_{m6} r_{o6} r_{o8}\right]$

(eq12.63) $A_v = G_m R_o$

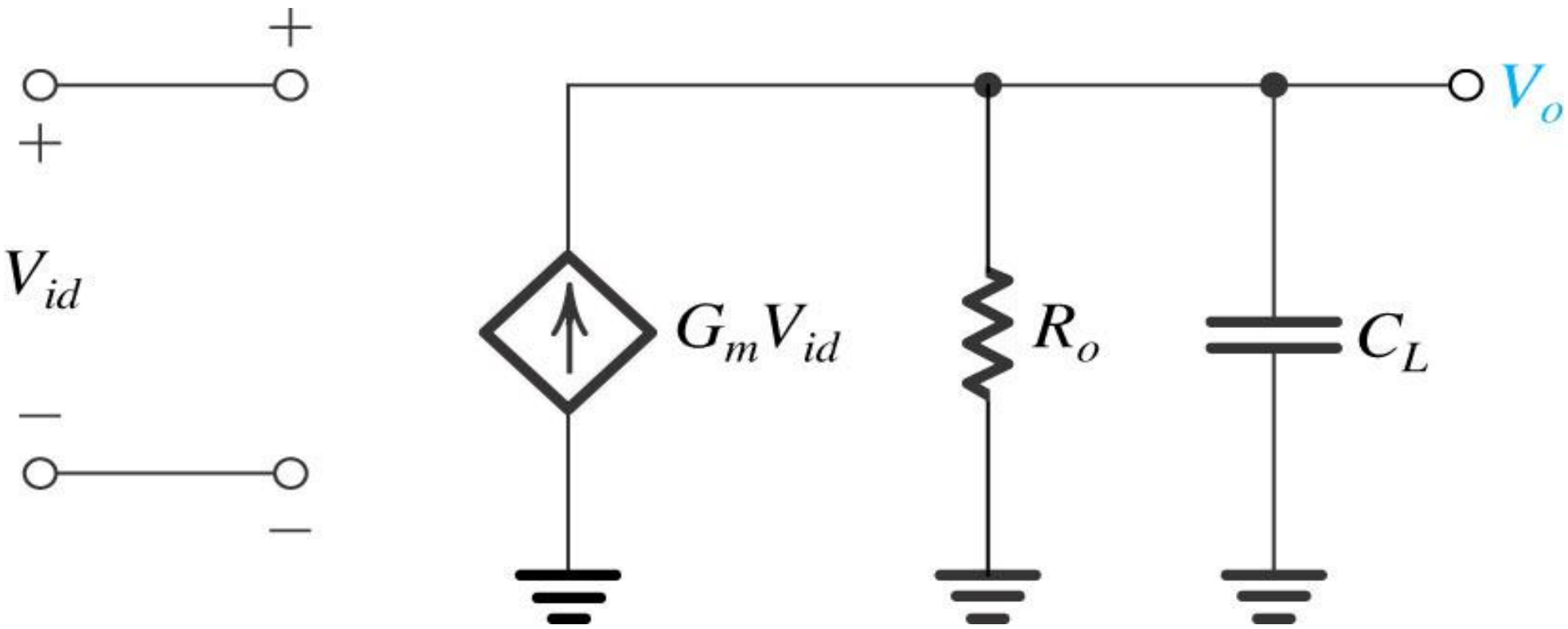


Figure 12.10: Small-signal equivalent circuit of the folded-cascode CMOS amplifier. Note that this circuit is in effect an operational transconductance amplifier (OTA)

12.3. The 741 Op-Amp Circuit

- Sections 12.3. through 12.6 focus on the 741 op-amp circuit.
  - Figure 12.13. provides a circuit schematic.
  - The design uses many transistors, few resistors.
- 741 requires two power supplies.
- $V_{CC} = V_{EE} = 15V$

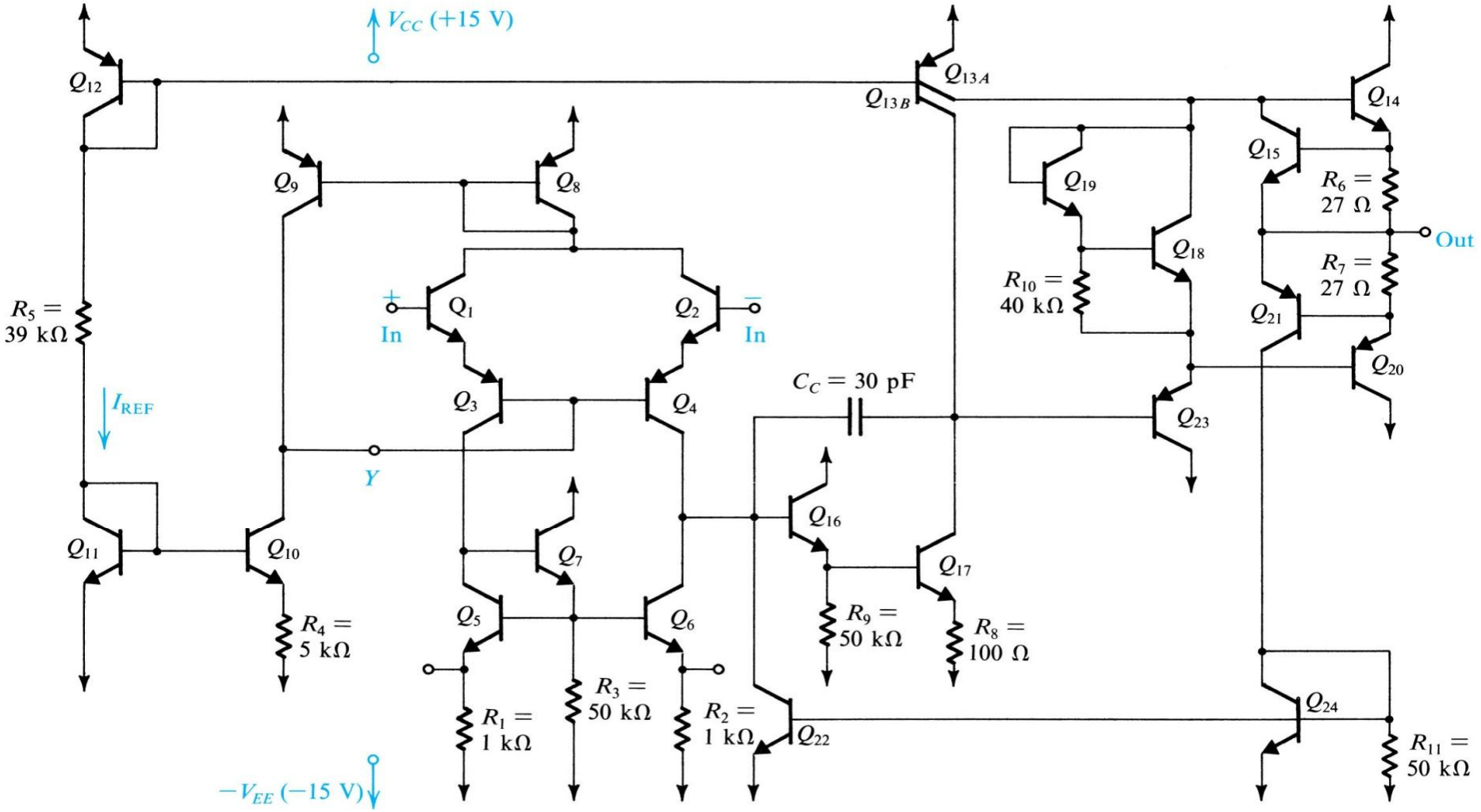


Figure 12.13: The 741 op-amp circuit: *Q*11, *Q*12, and *R*5 generate a reference bias current; *I*REF. *Q*10, *Q*9, and *Q*8 bias the input stage, which is composed of *Q*1 to *Q*7. The second gain stage is composed of *Q*16 and *Q*17 with *Q*13B acting as active load. The class AB output stage is formed by *Q*14 and *Q*20 with biasing devices *Q*13A, *Q*18, and *Q*19, and an input buffer *Q*23. Transistors *Q*15, *Q*21, *Q*24, and *Q*22 serve to protect the amplifier against output short circuits and are normally cut off.

12.3.3. The Input Stage

- 741 consists of three-stages:
  - Input Differential Stage (Q_1 through Q_7)
    - Emitter Followers: Q_1, Q_2
    - Differential Common-Base: Q_3, Q_4
    - Load Circuit: Q_5, Q_6, Q_7
    - Biasing: Q_8, Q_9, Q_{10}
  - Intermediate Single-Ended High-Gain Stage
  - Output-Buffering Stage (other transistors)

12.3.4. The Second Stage

- Consists of Q_{16}, Q_{17}, and Q_{13B}
  - Emitter Follower: Q_{16}
  - Common-Emitter: Q_{17}
  - Load: Q_{13B}
- Output of second stage is taken at collector of Q_{17}.
- Capacitor C_C is connected in feedback path of second stage.
  - Frequency compensation using Miller Technique.

12.3.5. The Output Stage

- Provides low output resistance.
- Able to supply relatively large load current.
  - With minimal power dissipation.
- Consists of Q_{14} and Q_{20}.
  - Complementary pair.
- Transistors Q_{18} and Q_{19} are fed by current source Q_{13A} and bias transistors Q_{14} and Q_{20}.

12.3.6. Device Parameters

- **npn:** $I_S = 10^{-14}A$, $\beta = 200$, $V_A = 125V$
- **pnp:** $I_S = 10^{-14}A$, $\beta = 50$, $V_A = 50V$
- **Q_{13A} and Q_{13B}:** $I_{SA} = 0.25(10^{-14})A$, $I_{SB} = 0.75(10^{-14})A$
  - These devices are non-standard.
- Q_{14} and Q_{20} will be assumed to have area three times of the standard device – for increased loading.

12.4. DC Analysis of the 741

for $V_{CC}=V_{EE}=15V$, $V_{EB11}=V_{BE12}=0.7V$, $I_{REF}=0.73mA$

$$I_{REF}=\frac{V_{CC}-V_{EB12}-V_{BE11}+V_{EE}}{R_5}$$

(eq12.75) $$V_T \ln\left(\frac{I_{REF}}{I_{C10}}\right)=I_{C10}R_4$$

(eq12.76) $$I_{C5}=I_{C6}$$

(eq12.77) $$I_{C5}\approx I_{C3}\approx I$$

(eq12.78) $$I_{C6}\approx I_{C4}\approx I$$

(eq12.79) $$I_{C7}\approx I_{E7}=\frac{2I}{\beta_N}+\frac{V_{BE6}+IR_2}{R_3}$$

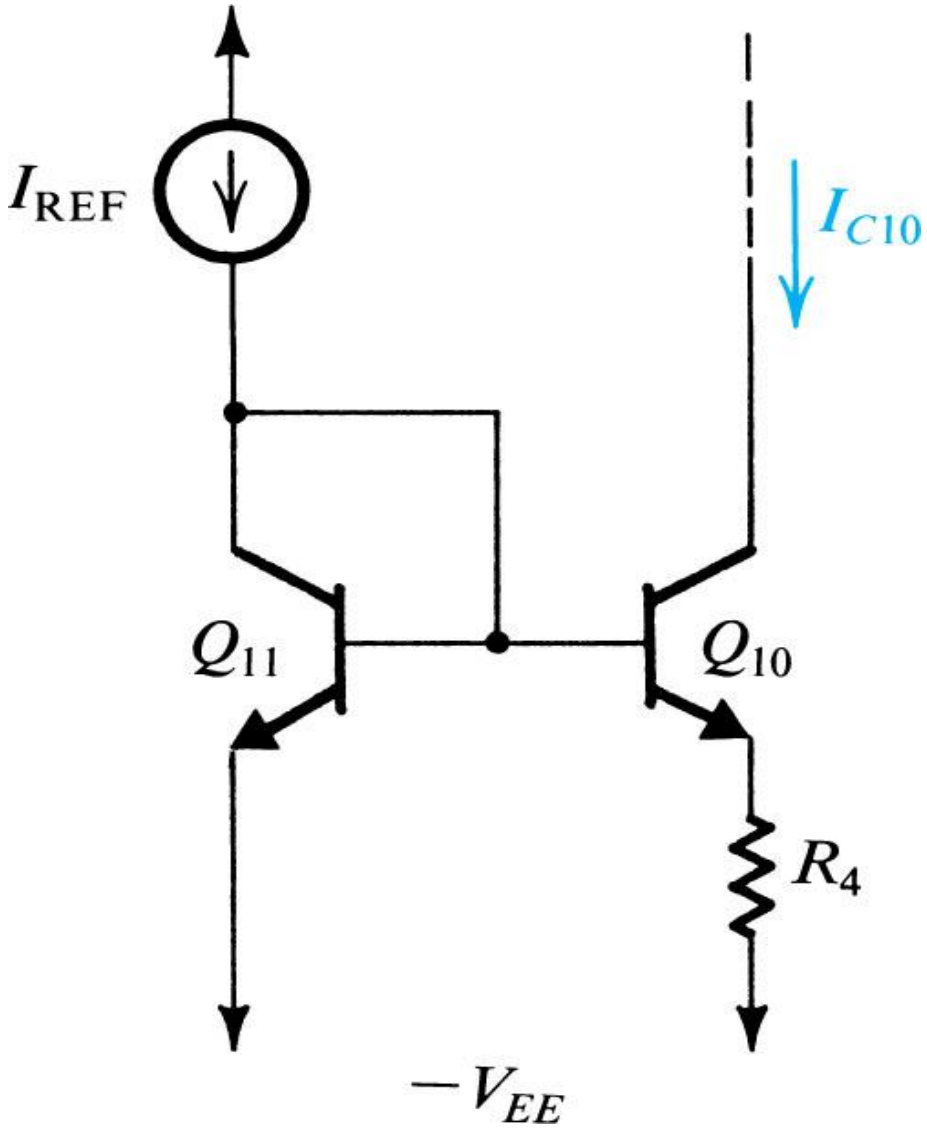


Figure 12.14: The Widlar current source that biases the input stage.

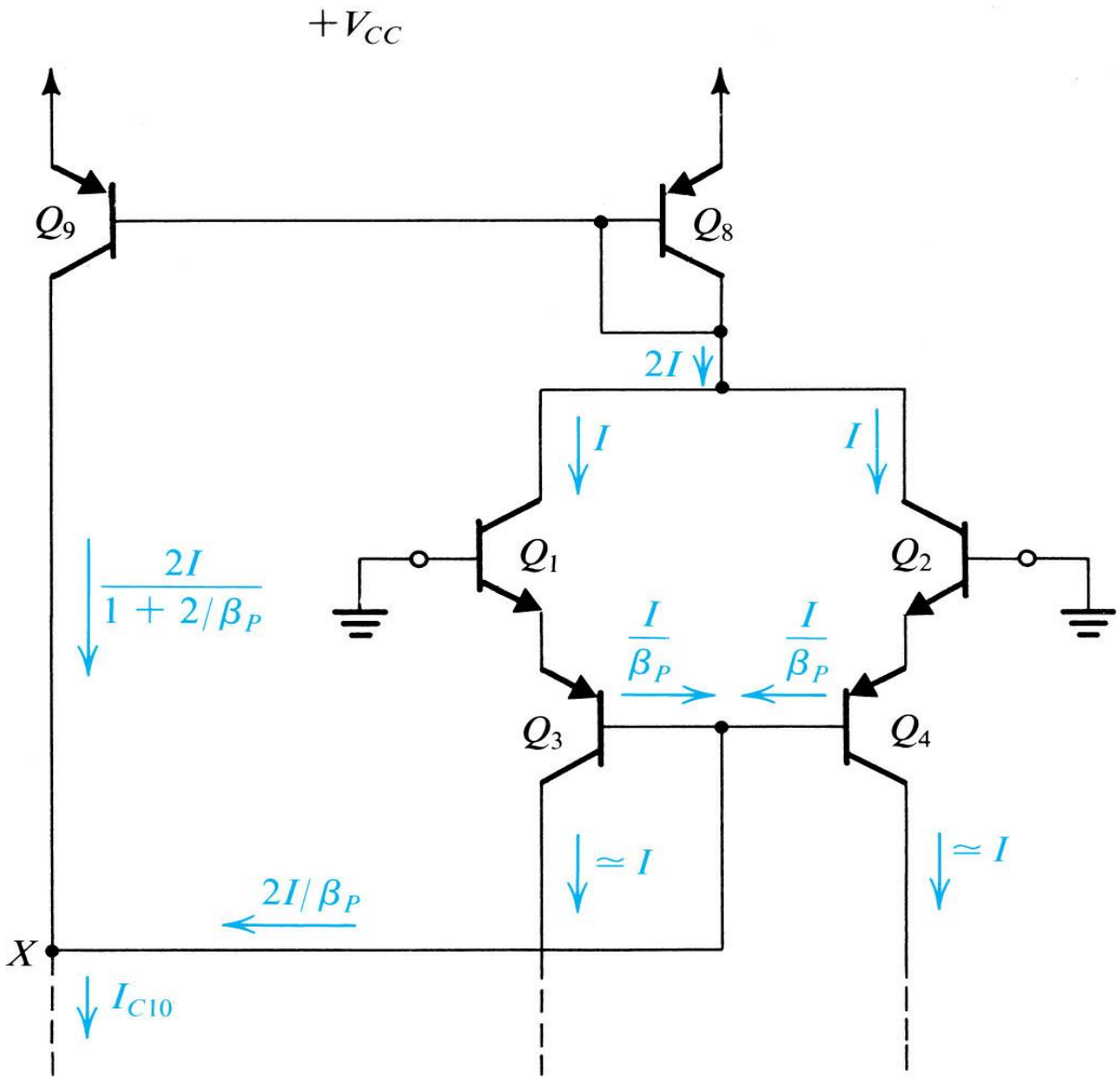


Figure 12.15: The dc analysis of the 741 input stage.

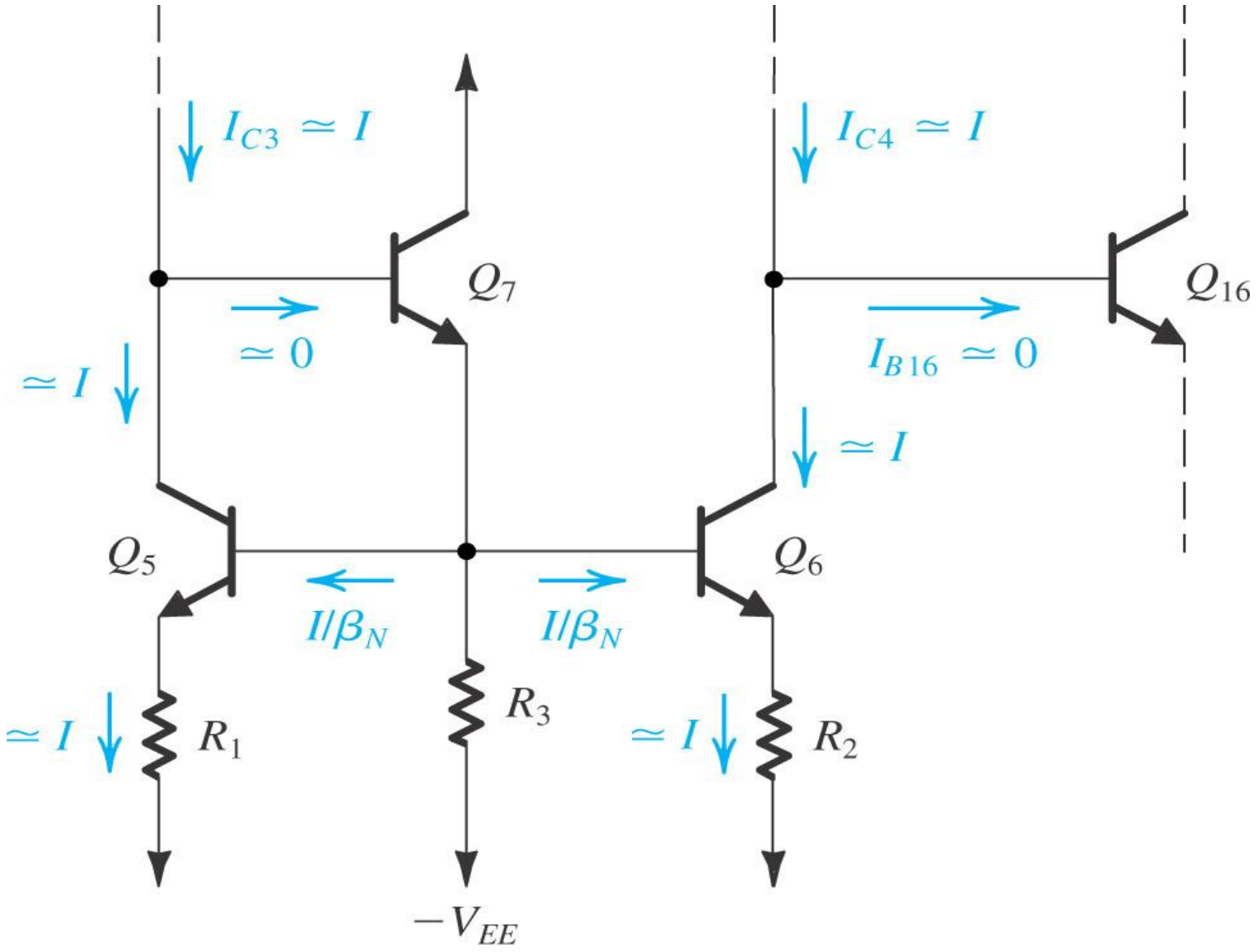


Figure 12.16: The dc analysis of the 741 input stage, continued.

12.4. DC Analysis of the 741

Table 12.1 DC Collector Currents of the 741 Circuit (μA)

Q_1	9.5	Q_8	19	Q_{13B}	550	Q_{19}	15.8
Q_2	9.5	Q_9	19	Q_{14}	154	Q_{20}	154
Q_3	9.5	Q_{10}	19	Q_{15}	0	Q_{21}	0
Q_4	9.5	Q_{11}	730	Q_{16}	16.2	Q_{22}	0
Q_5	9.5	Q_{12}	730	Q_{17}	550	Q_{23}	180
Q_6	9.5	Q_{13A}	180	Q_{18}	165	Q_{24}	0
Q_7	10.5						

12.5. Small Signal Analysis of 741

- One may use small-signal analysis (as in previous chapters) to analyze linear behavior of the 741.
  - Figures 12.18 – 12.21 describe this process for input stage.
  - Figures 12.25 – 12.27 describe this process for gain stage.
  - Figures 12.28 – 12.30 describe this process for output stage.

12.5. Small Signal Analysis of 741

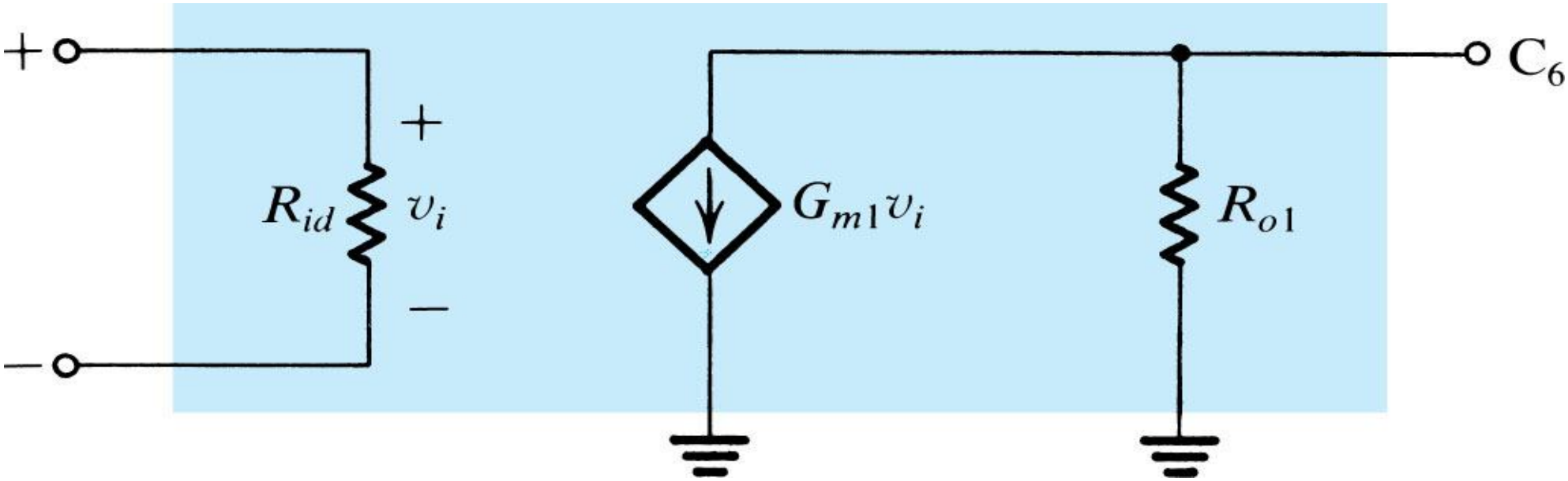


Figure 12.21: Small-signal equivalent circuit for the input stage of the 741 op amp.

12.5. Small Signal Analysis of 741

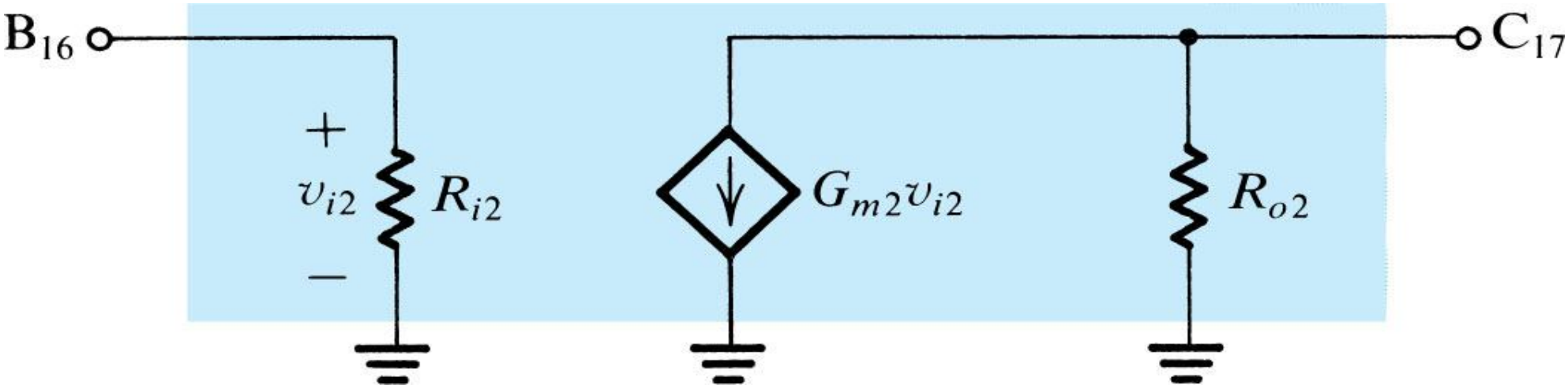


Figure 12.25: Small-signal equivalent-circuit model of the second stage.

Summary

- Most CMOS op-amps are designed to operate as part of a VLSI circuit and thus required to drive only small capacitive loads. Therefore, most do not have a low-output-resistance stage.
- There are basically two approaches to the design of CMOS op-amps: a two-stage configuration and a single-stage topology using the folded-cascode circuit.
- In the two-stage CMOS op-amp, approximately equal gains are realized in the two stages.

Summary

- The threshold mismatch together with the low transconductance of the input stage result in a larger input offset voltage for the CMOS op-amps than for bipolar units.
- Miller compensation is employed in the two-stage CMOS op-amp, but a series resistor is required to place the transmission zero at either s = infinity or on the negative real axis.
- CMOS op-amps have better slew rates (than alt's).

Summary

- Use of the cascode configuration increases the gain of a CMOS amplifier stage by about two orders of magnitude, thus making possible a single-stage op-amp.
- The dominant pole of the folded-cascode op-amp is determined by the total capacitance at the output CL. Increasing CL improves the phase margin at the expense of reducing bandwidth.
- By using two complementary input differential pairs in parallel, the common-mode range may be extended.

Summary

- The output voltage swing of the folded-cascode op-amp may be extended by utilizing a wide-swing current mirror in place of the cascode mirror.
- The internal circuit of the 741 op-amp embodies many of the design techniques employed in bipolar analog integrated circuits.
- The 741 circuit consists of an input differential stage, a high-gain single-ended second stage, and a class AB output stage. It is the basis for many other devices.

Summary

- To obtain low input offset voltage and current, and high CMRR, the 741 input stage is designed to be perfectly balanced. The CMRR is increased by common-mode feedback, which also stabilizes the dc operating point.
- To obtain high input resistance and low input bias current, the input stage of the 741 is operated as a very low current level.
- The use of Miller Frequency compensation in the 741 circuit enables locating the dominant pole at a very low frequency, while utilizing a relatively small compensating capacitance.

Summary

- Two-stage op-amps may be modeled as a transconductance amplifier feeding an ideal integrator with C_C as the integrating capacitor.
- The slew rate of a two-stage op-amp is determined by the first-stage bias current and frequency-compensation capacitor.
- While the 741 and similar op-amps nominally operate from 15V power supplies, modern BJT op-amps typically utilize a single ground-referenced supply of only 2 or 3V.

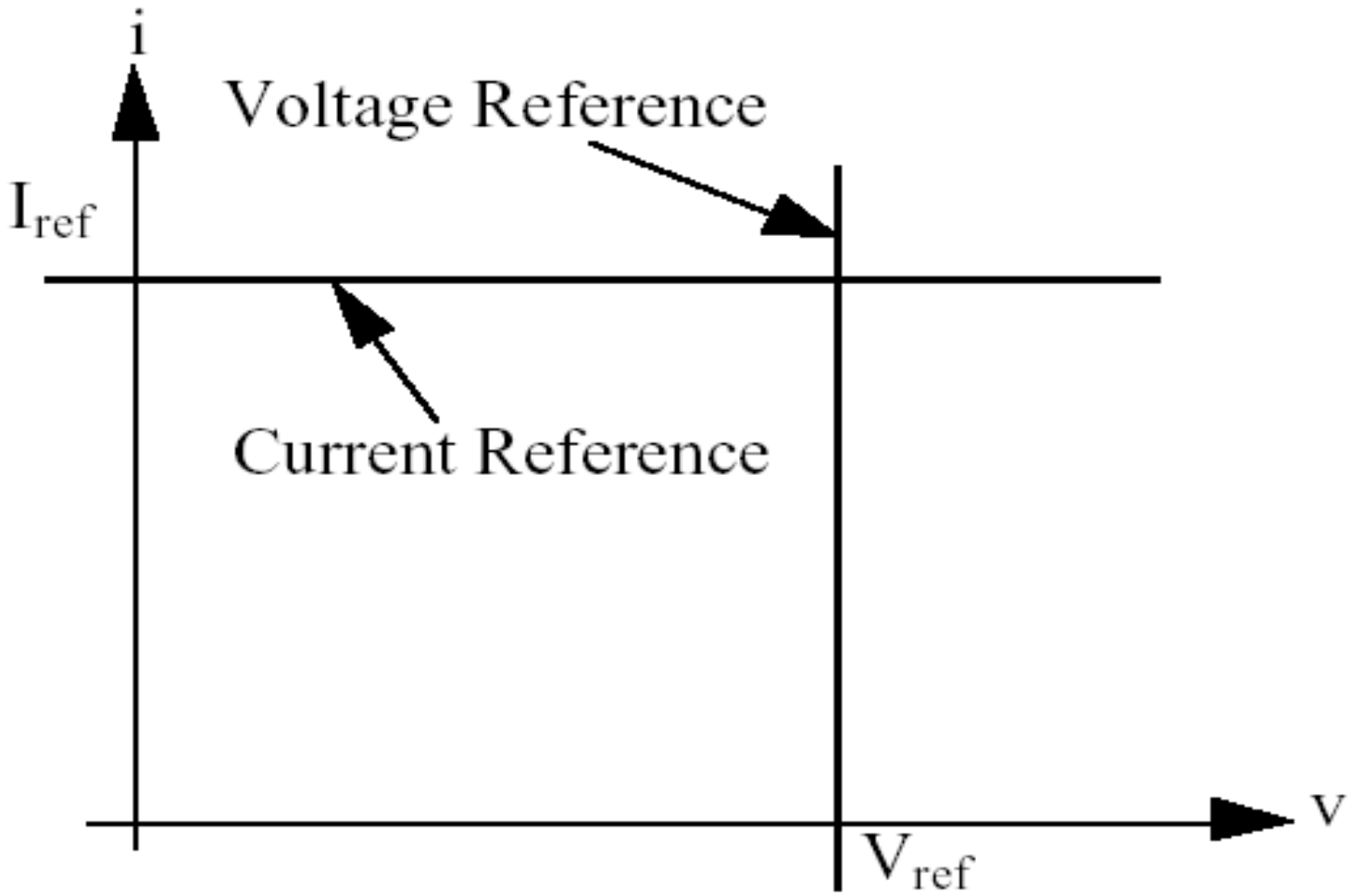
UNIT - V

BANDGAP REFERENCES

REFERENCE CIRCUITS

- A reference circuit is an independent voltage or current source which has a high degree of precision and stability.
  - Output voltage/current should be independent of power supply.
  - Output voltage/current should be independent of temperature.
  - Output voltage/current should be independent of processing variations

I-V curves of ideal references



Types of commonly used references

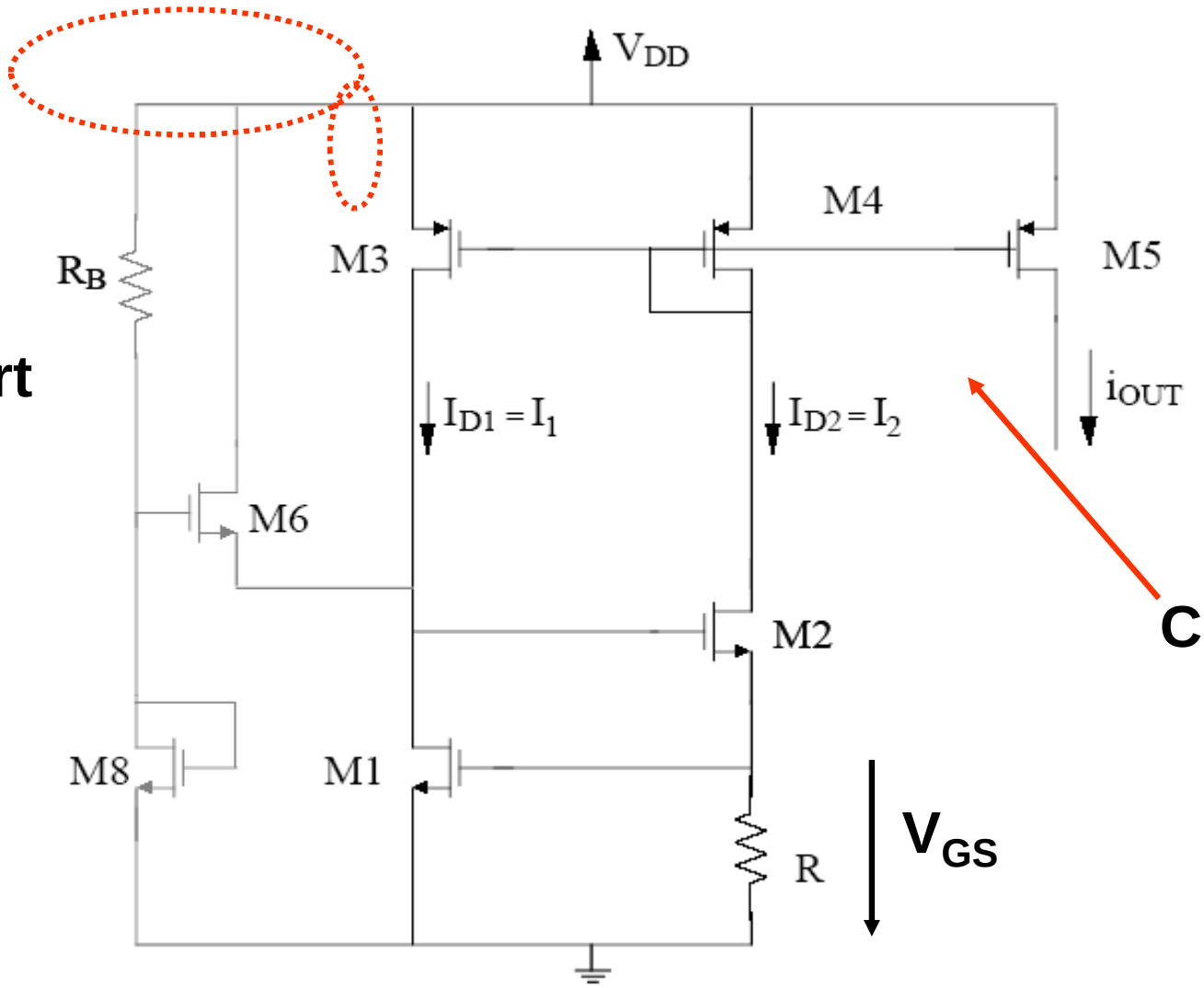
- Voltage dividers - passive and active.
- MOS diode reference.
- PN junction diode reference.
- Gate-source threshold reference circuit.
- Base-emitter reference circuit.
- Thermo voltage reference circuit
- Bandgap reference circuit

Typical variations affecting the references

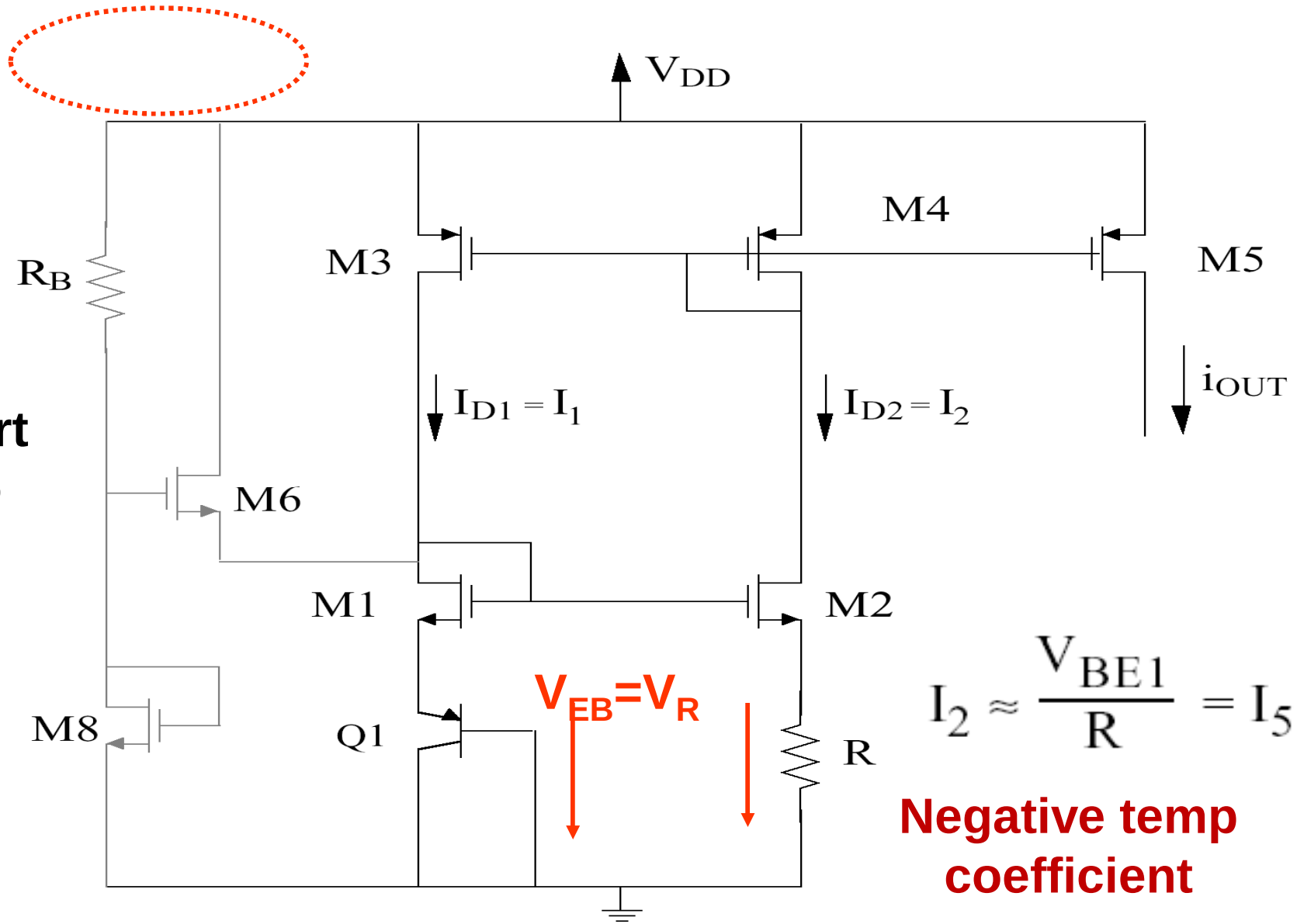
- Power supply variation (main concern here)
- Load variation (r_o=∞ for I-ref, r_o=0 for V-ref)
- Temperature variation (main concern also)
- Processes variation (good process and layout)
- Interferences and noise (not considered here)

V_{GS} based Current reference

MOS version: use V_{GS} to generate a current and then use negative feed back stabilize i in MOS



V_{EB} based current reference

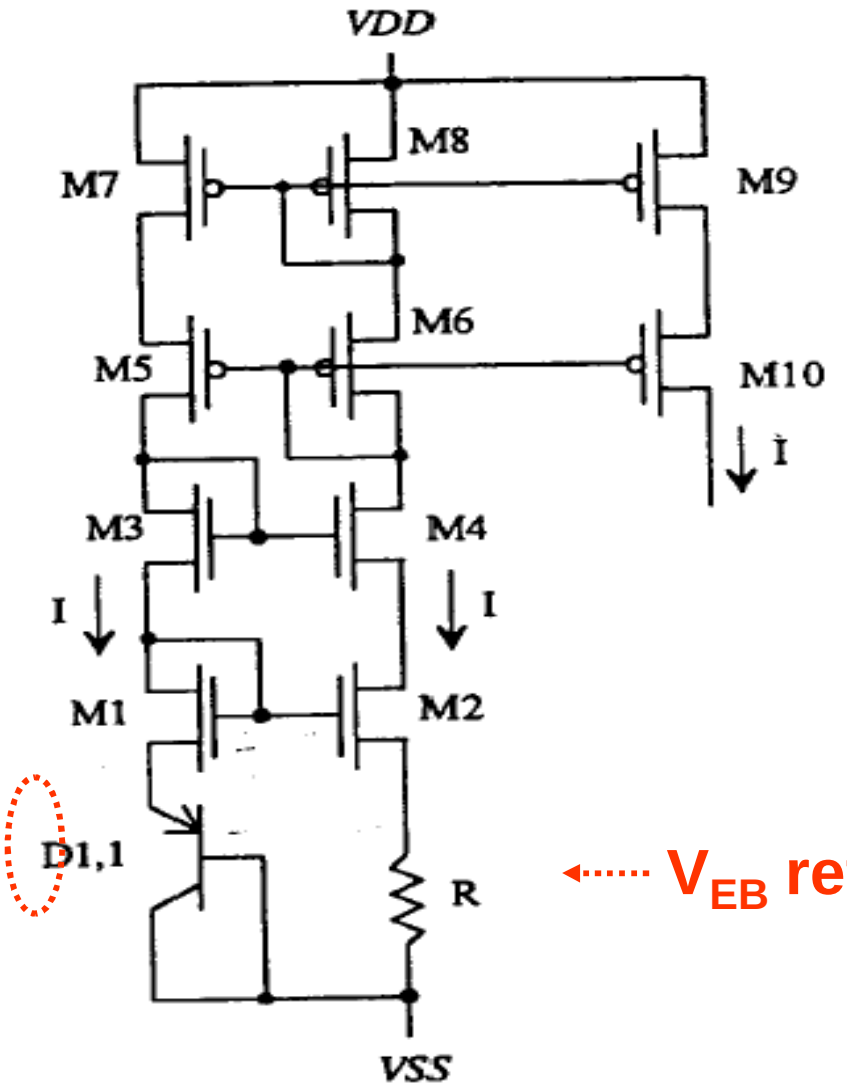


Start up

$$I_2 \approx \frac{V_{BE1}}{R} = I_5$$

Negative temp coefficient

A cascoded version to increase r_o and reduce sensitivity:

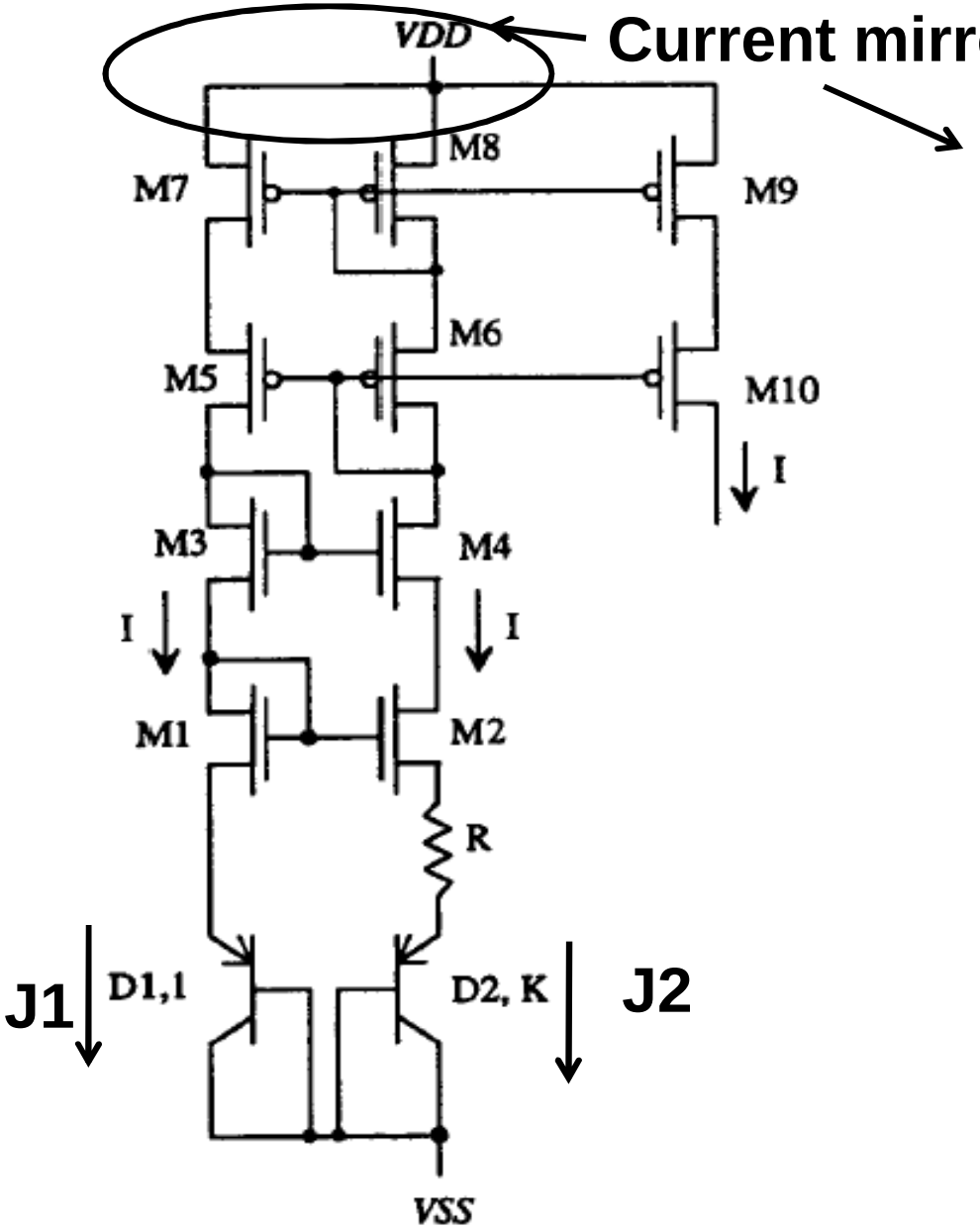


Requires start up

Not shown here

V_{EB} reference

A thermal voltage based current reference



$$I_1 = I_2, \Rightarrow J_1 = KJ_2,$$

$$\text{but } J = J_s \exp(V_{EB}/V_t)$$

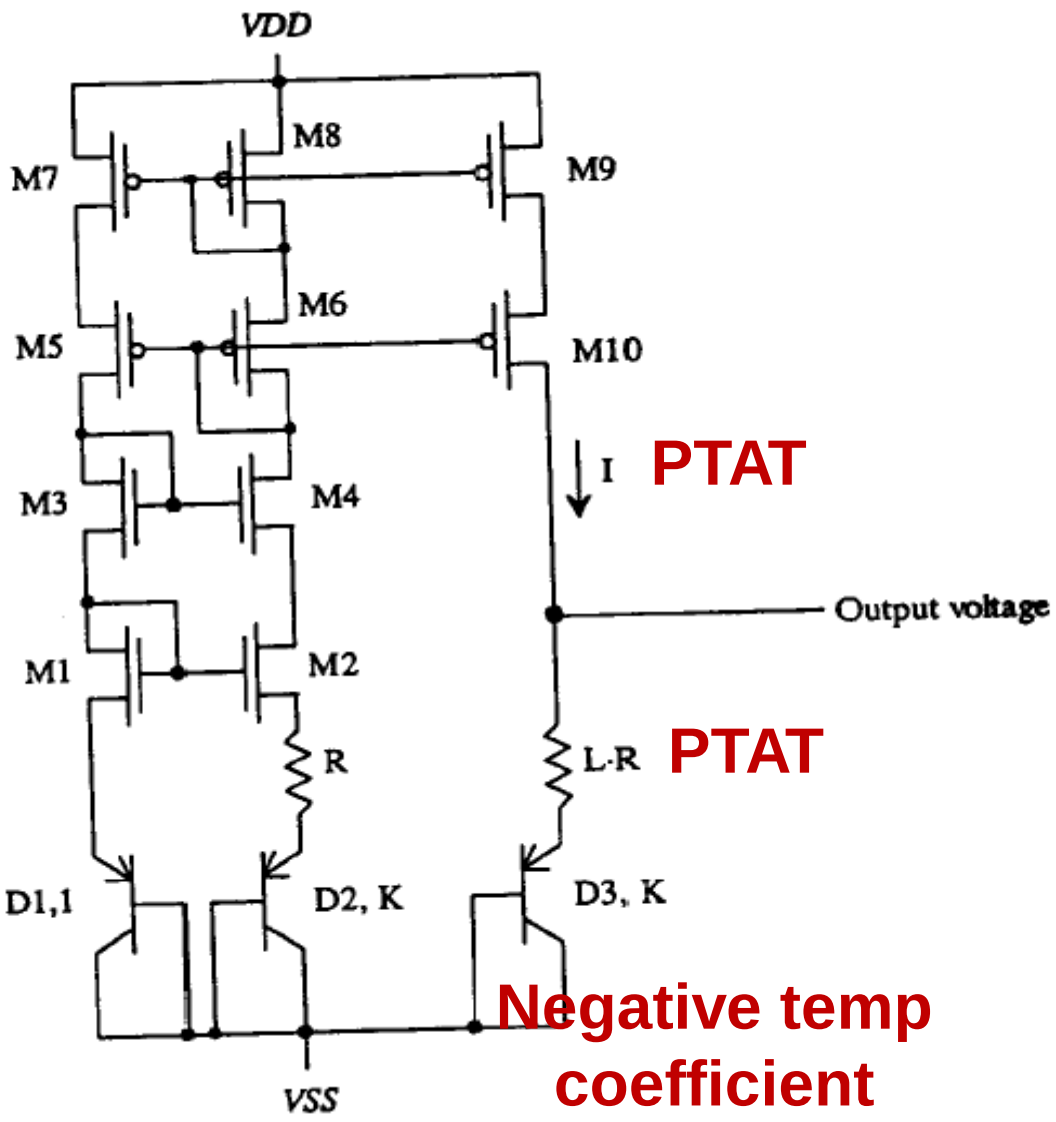
$$\Rightarrow J_1/J_2 = K = \exp((V_{EB1} - V_{EB2})/V_t)$$

$$\Rightarrow V_{EB1} - V_{EB2} = V_t \ln(K)$$

$$\Rightarrow I = (V_{EB1} - V_{EB2})/R$$
$$= V_t \ln(K)/R \propto V_t = kT/q$$

PTAT

A band gap voltage reference



$V_{out} = V_{EB3} + I*L*R = V_{EB3} + (kT/q)*Lln(K)$

$\partial V_{out}/\partial T = \partial V_{EB3}/\partial T + (k/q)*Lln(K)$

At room temperature,

$\partial V_{EB3}/\partial T = -2.2$ mV/°C,

$k/q = +0.085$ mV/°C.

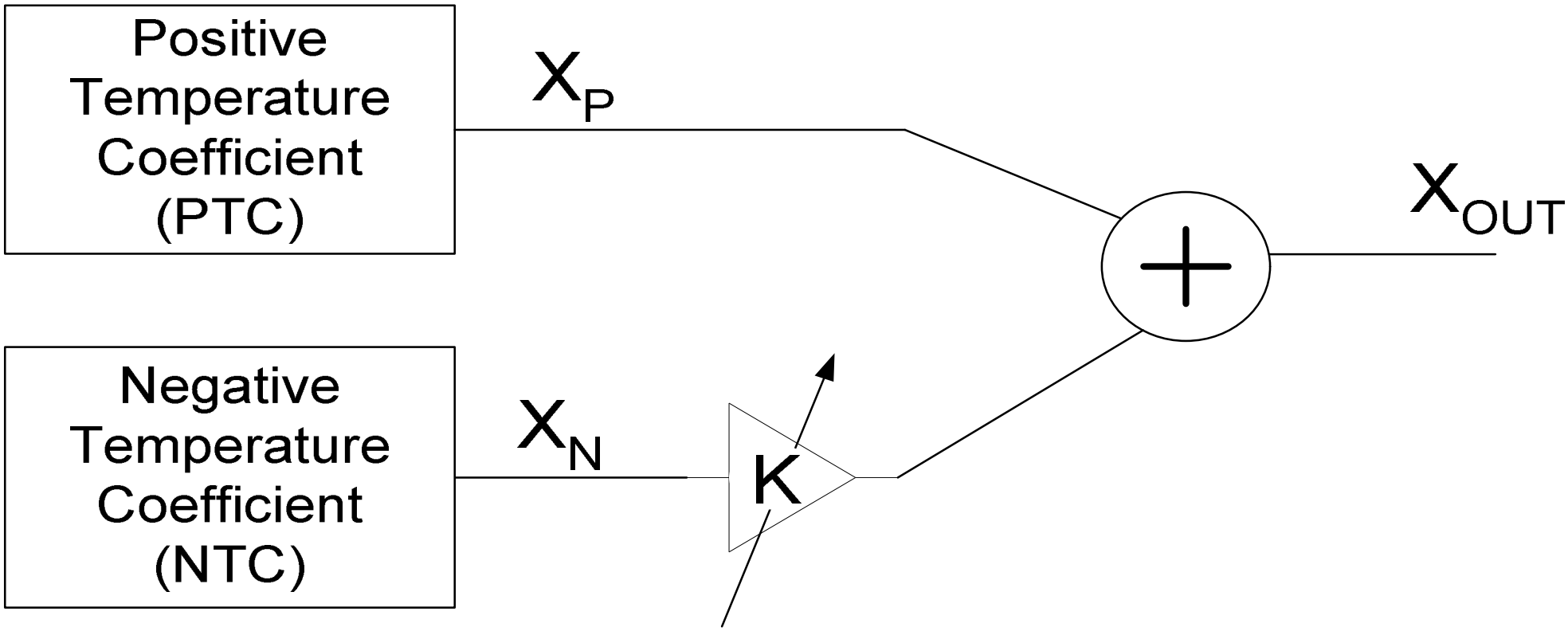
Hence, choosing appropriate L and K can make

$\partial V_{out}/\partial T = 0$

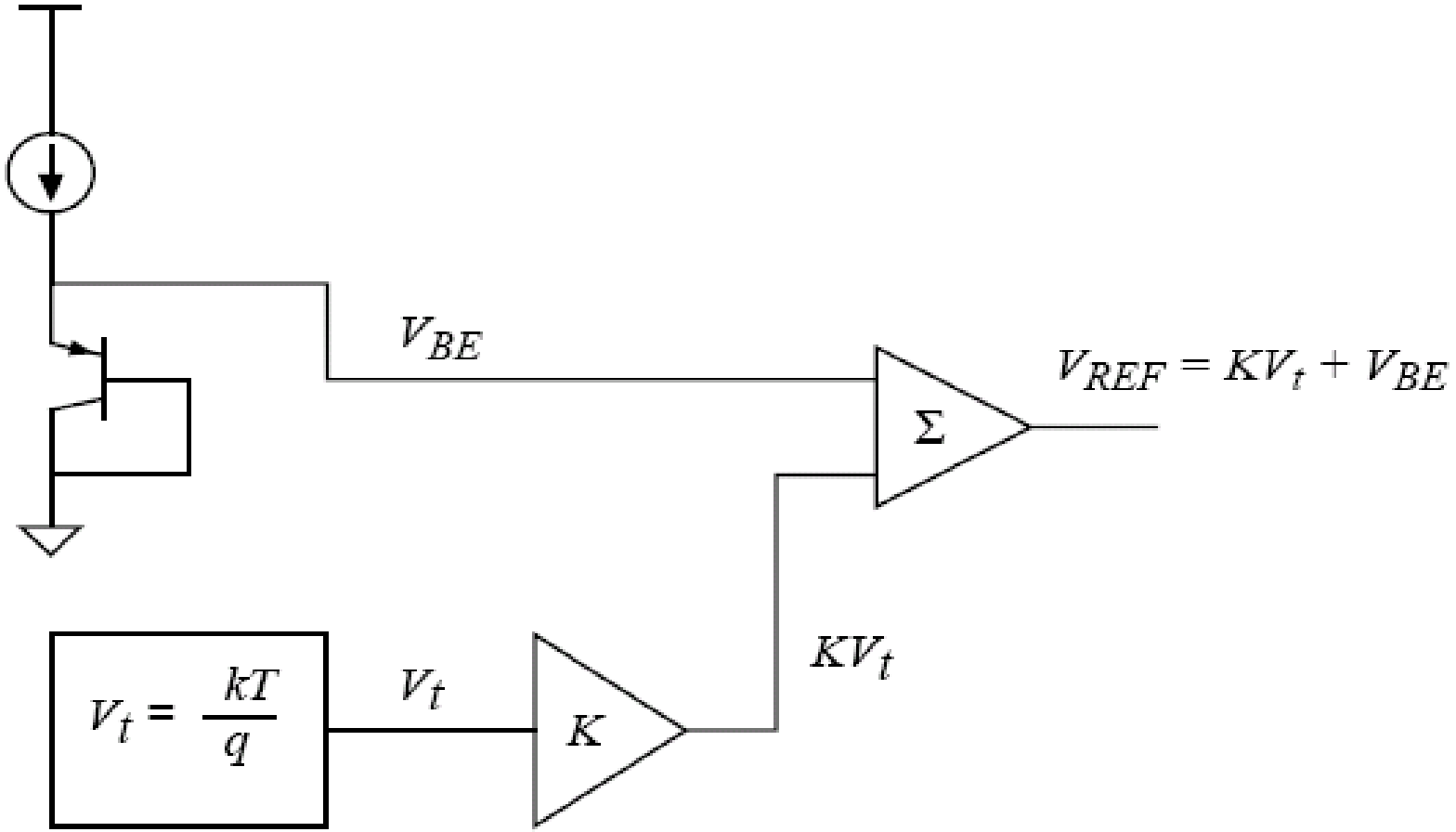
When this happens, V_{out} = 1.26 V

General principle of bandgap reference

Generate a negatively PTAT (Proportional To Absolute Temperature) and a positively PTAT voltages and sum them appropriately.



A Common way of bandgap reference



V_{BE} is negatively PTAT at roughly -2.2 mV/°C at room temperature, called CTAT

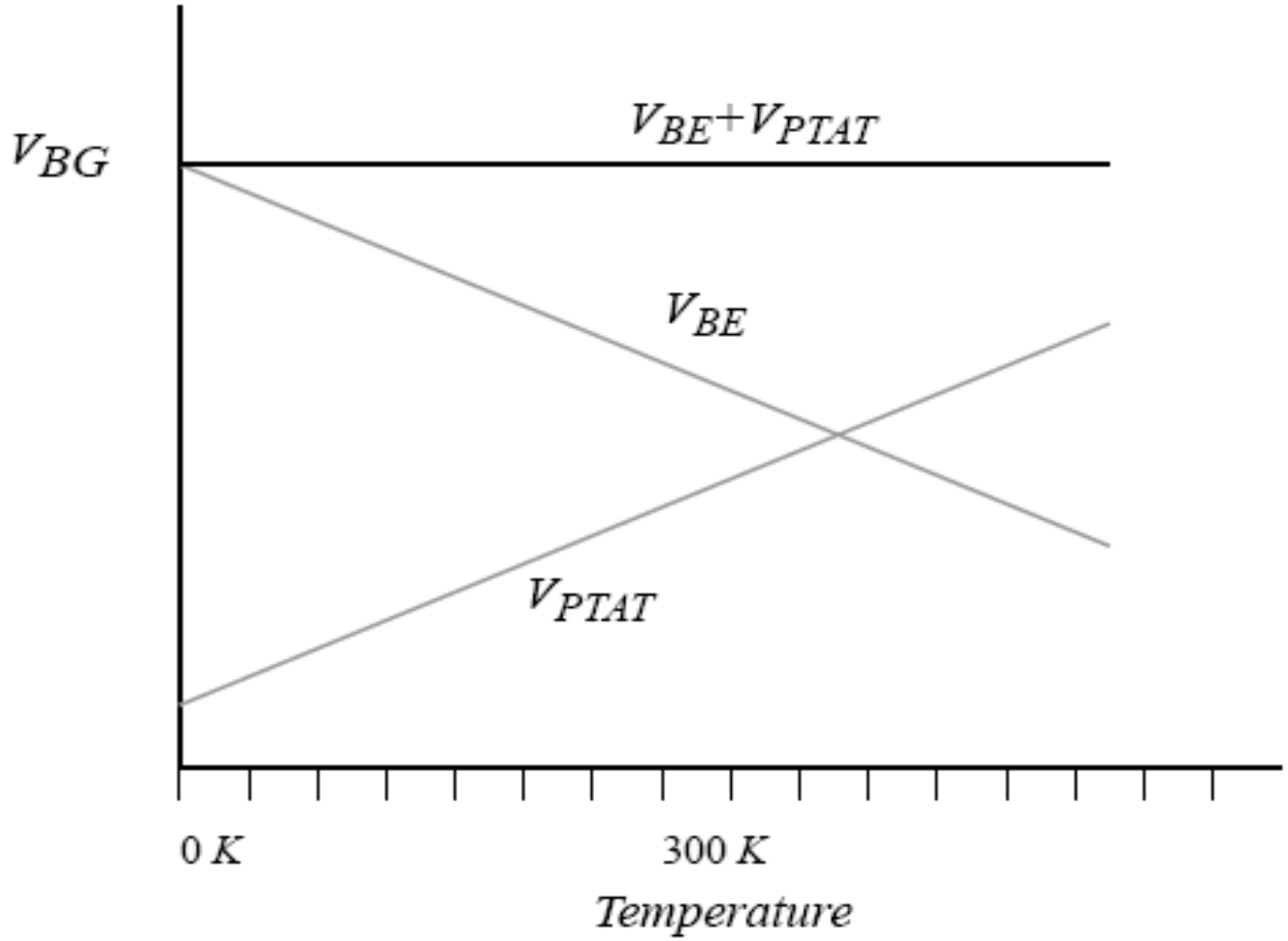
V_t ($V_t = kT/q$) is PTAT that has a temperature coefficient of +0.085 mV/°C at room temperature.

Multiply V_t by a constant K and sum it with the V_{BE} to get

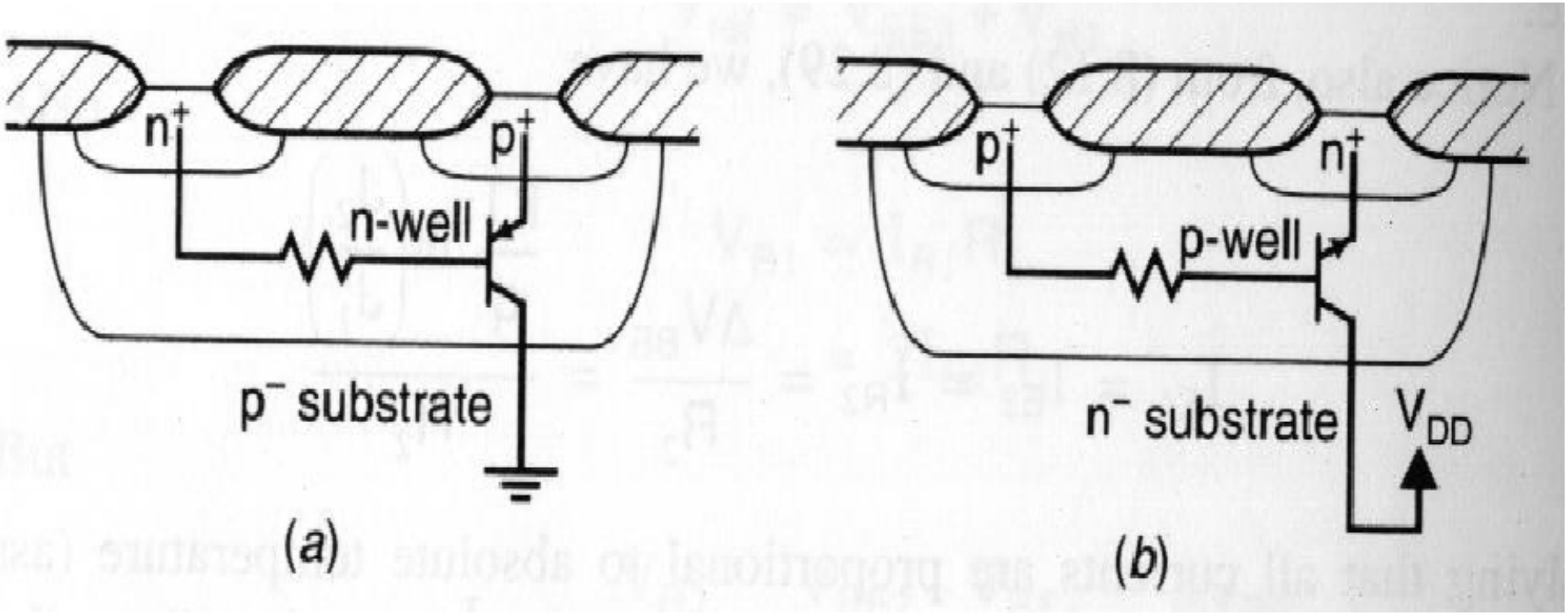
$$V_{REF} = V_{BE} + KV_t$$

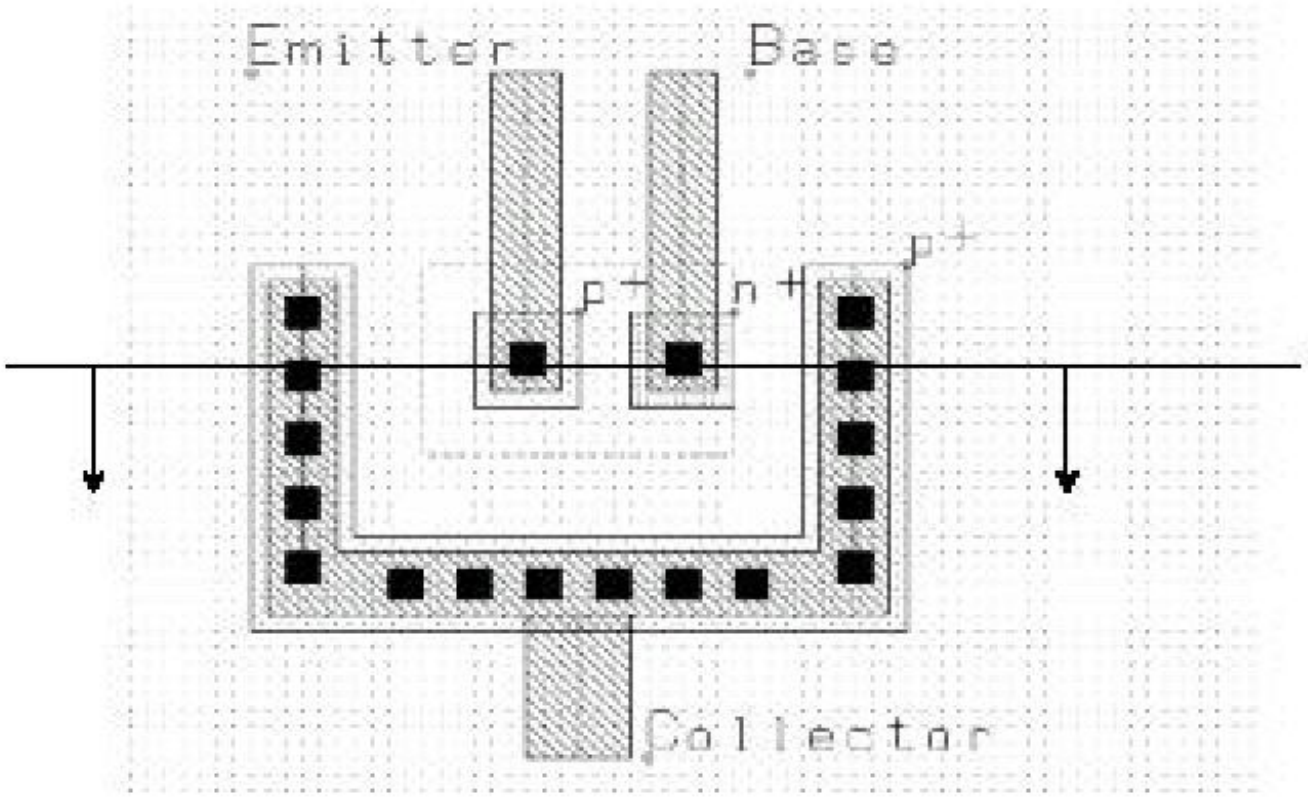
If K is right, temperature coefficient can be zero.

In general, use $V_{BE} + V_{PTAT}$

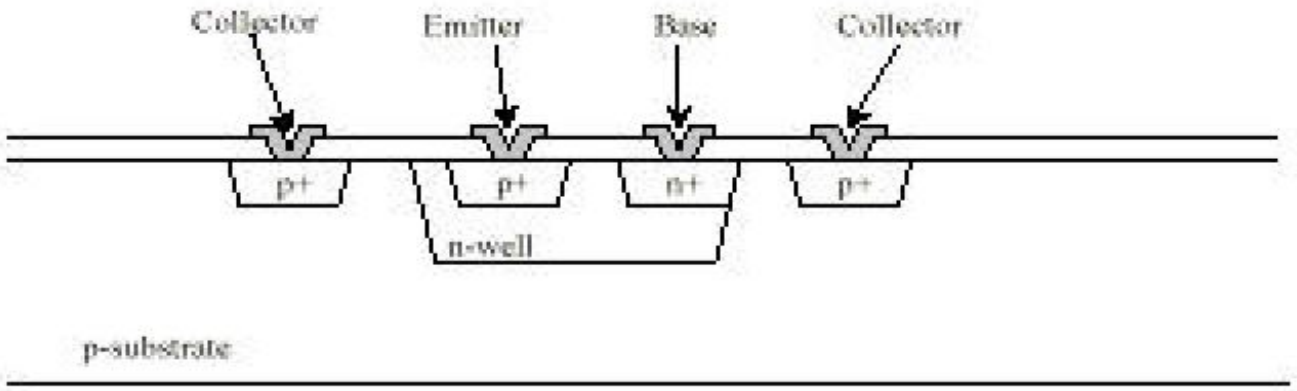


How to get Bipolar in CMOS?

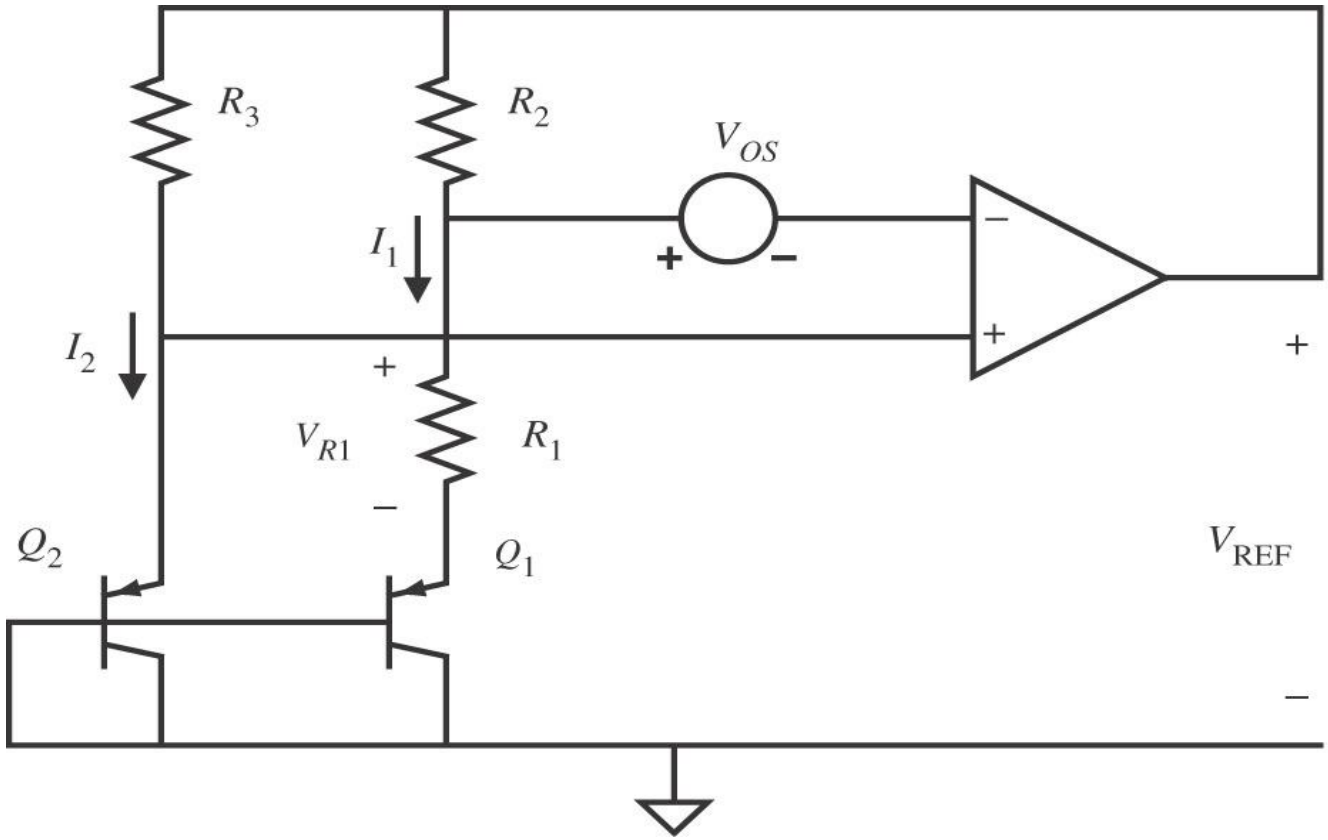



Emitter
Base
p+
p+
n+
Collector

(a)


Collector
Emitter
Base
Collector
p+
p+
n+
p+
n-well
p-substrate

A conventional CMOS bandgap reference for a n-well process



V_{OS} represents input offset voltage of the amplifier. Transistors Q_1 and Q_2 are assumed to have emitter-base areas of A_{E1} and A_{E2}, respectively.

If V_{OS} is zero, then the voltage across R_1 is given as

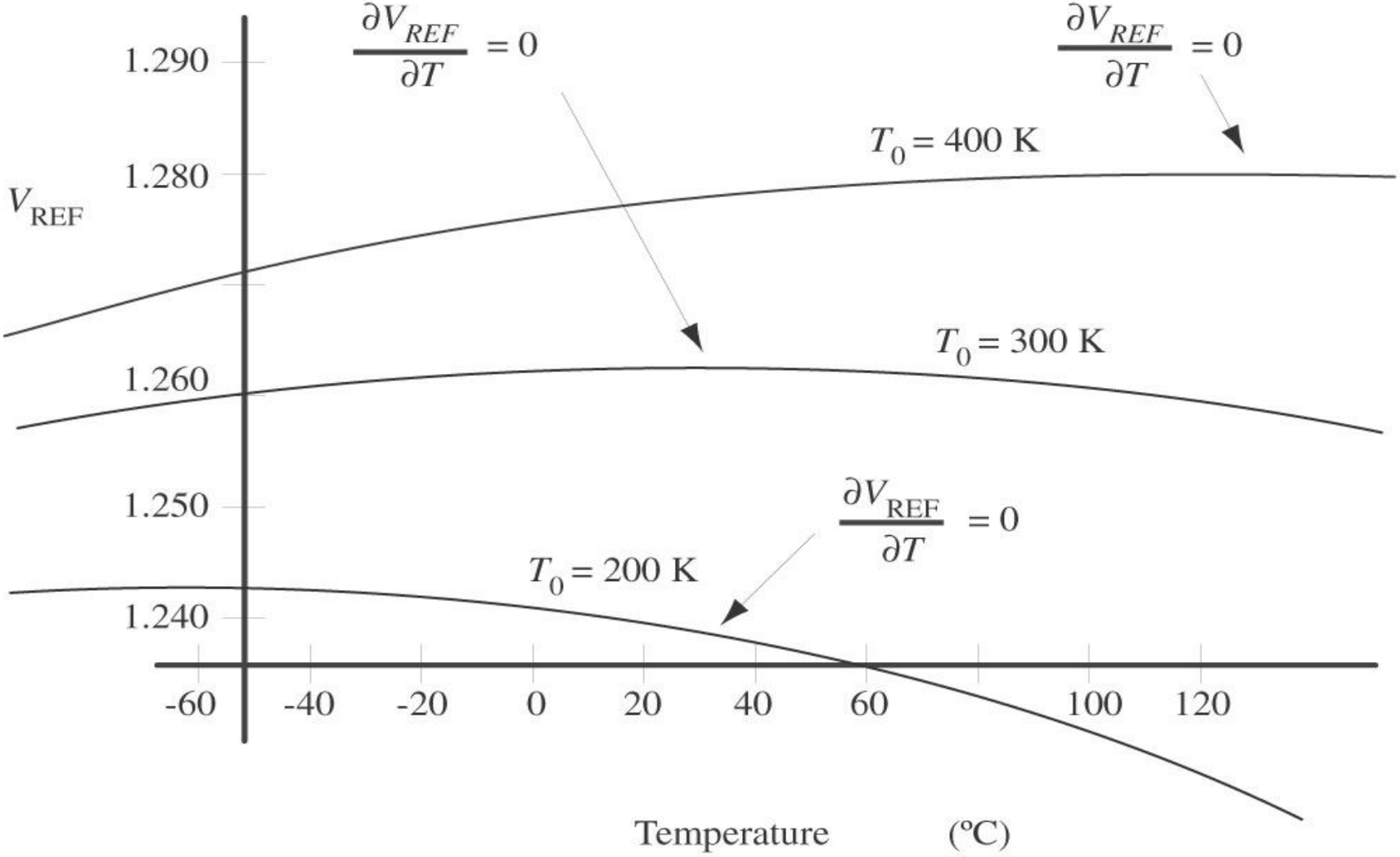
$$V_{R1} = V_{BE2} - V_{BE1} = V_t \ln\left(\frac{J_2}{J_{S2}}\right) - V_t \ln\left(\frac{J_1}{J_{S1}}\right) = V_t \ln\left(\frac{I_2 A_{E1}}{I_1 A_{E2}}\right)$$

$$I_1 R_2 = I_2 R_3 \qquad V_{\mathrm{REF}} = V_{BE2} + I_1 R_2 = V_{BE2} + V_{R1}\left(\frac{R_2}{R_1}\right)$$

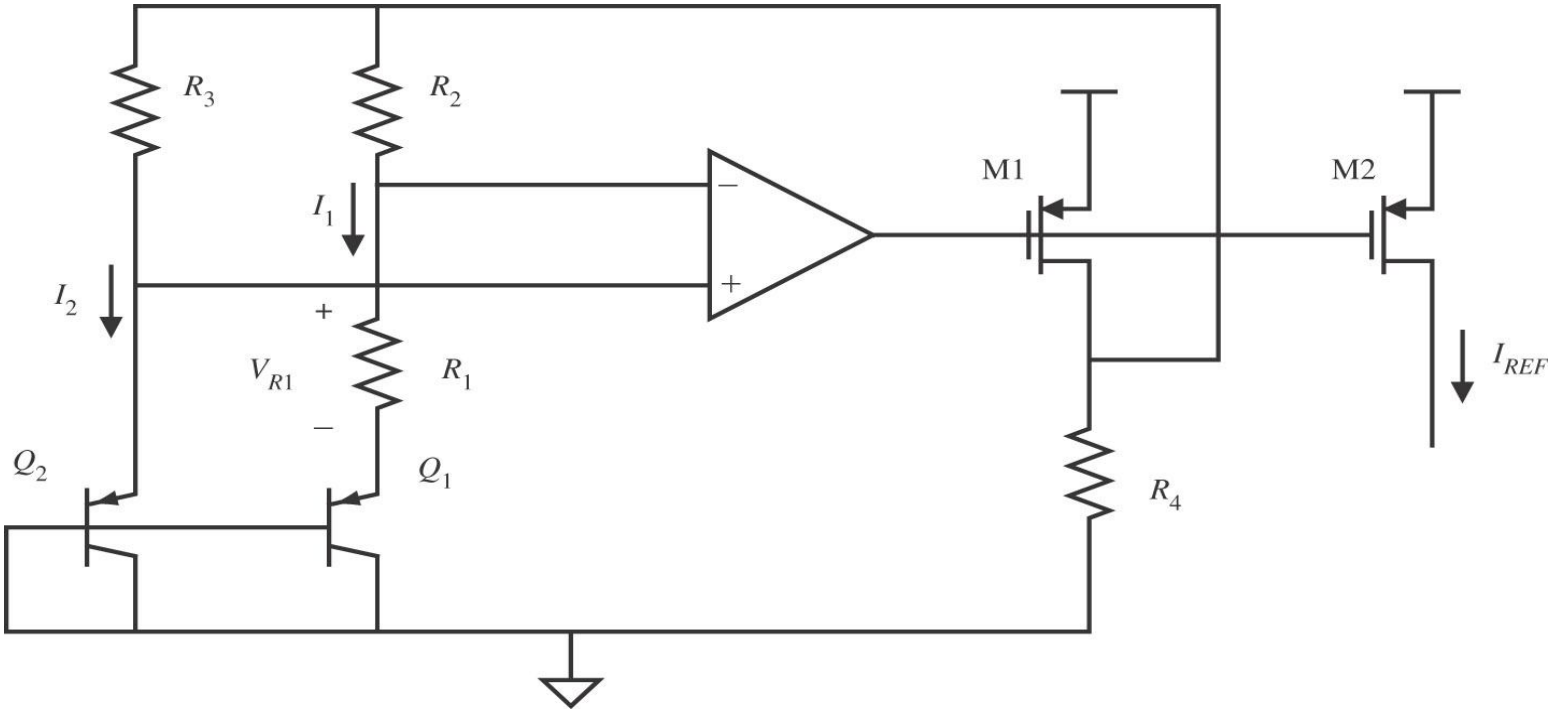
$$V_{\mathrm{REF}} = V_{BE2} + \left(\frac{R_2}{R_1}\right) V_t \ln\left(\frac{R_2 A_{E1}}{R_3 A_{E2}}\right)$$

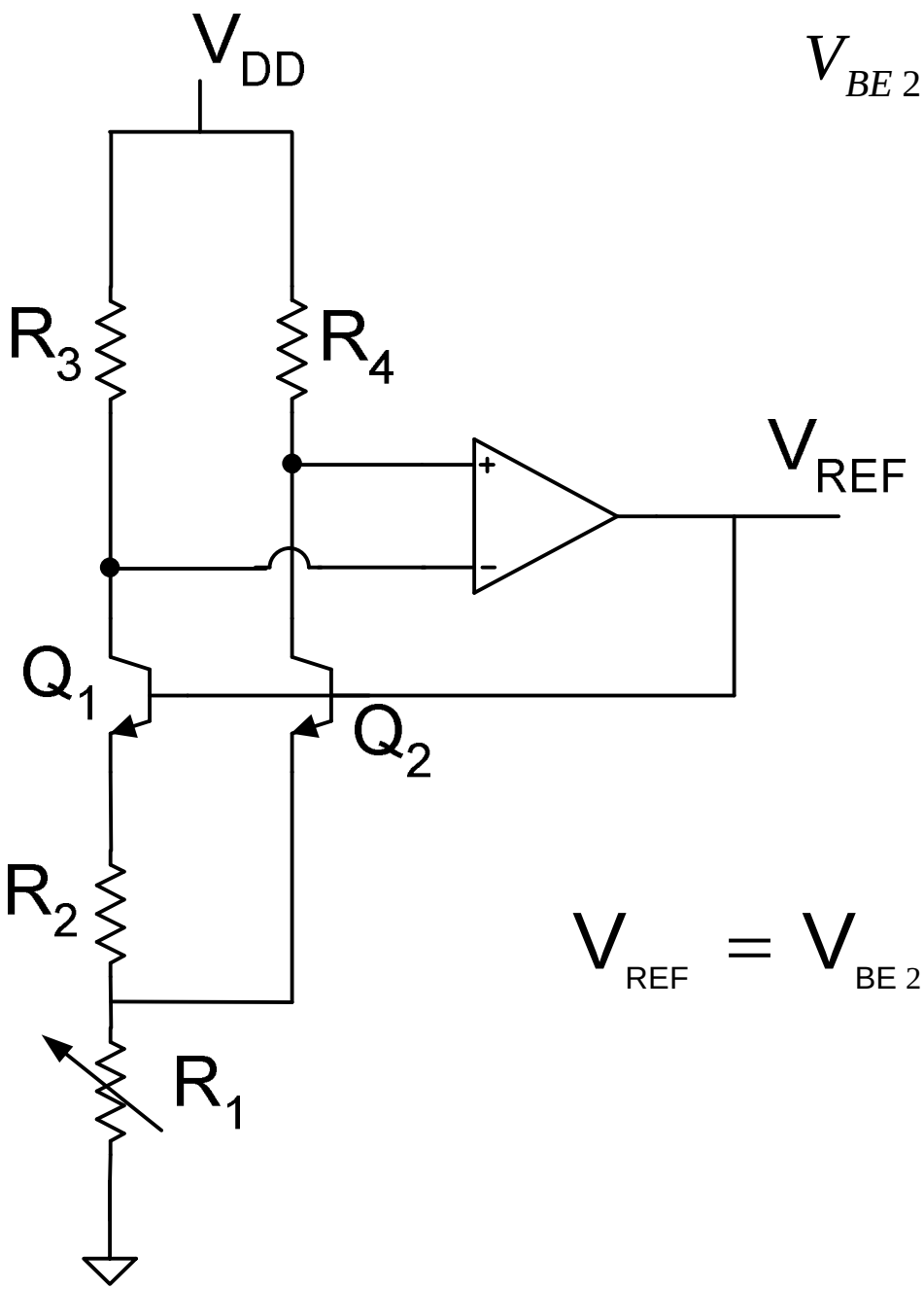
$$K = \left(\frac{R_2}{R_1}\right) \ln\left(\frac{R_2 A_{E1}}{R_3 A_{E2}}\right)$$

Bandgap reference still varies a little with temp



Converting a bandgap voltage reference to a current reference



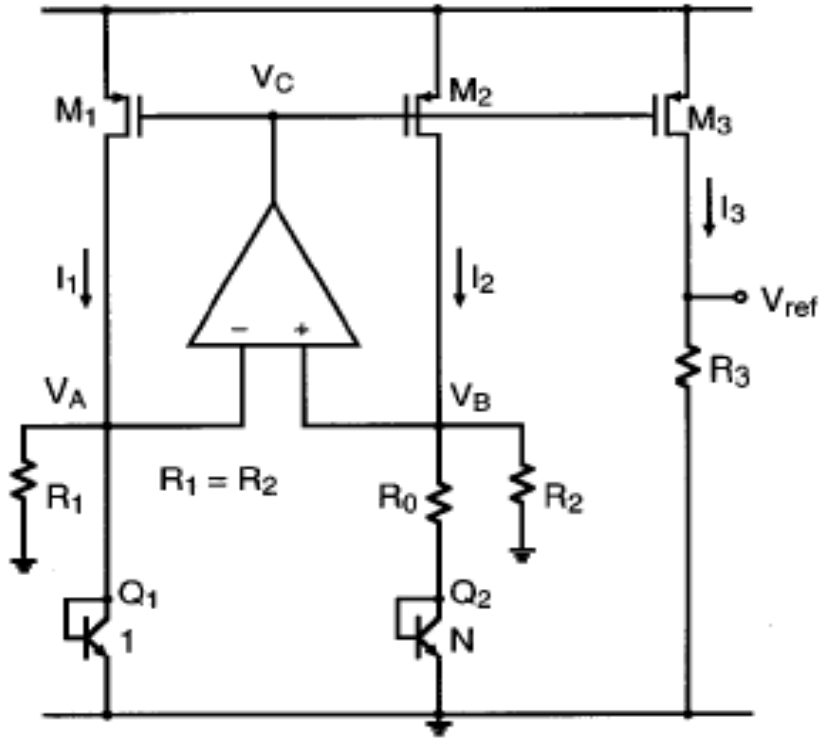


$$V_{BE2} - V_{BE1} = \Delta V_{BE} = \left[\frac{k}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\frac{R_3}{R_4}\right)\right]T$$

$$I_{C1} = \left(\frac{\beta_1}{1+\beta_1}\right)I_{E1} = \alpha_1 I_{E1}$$

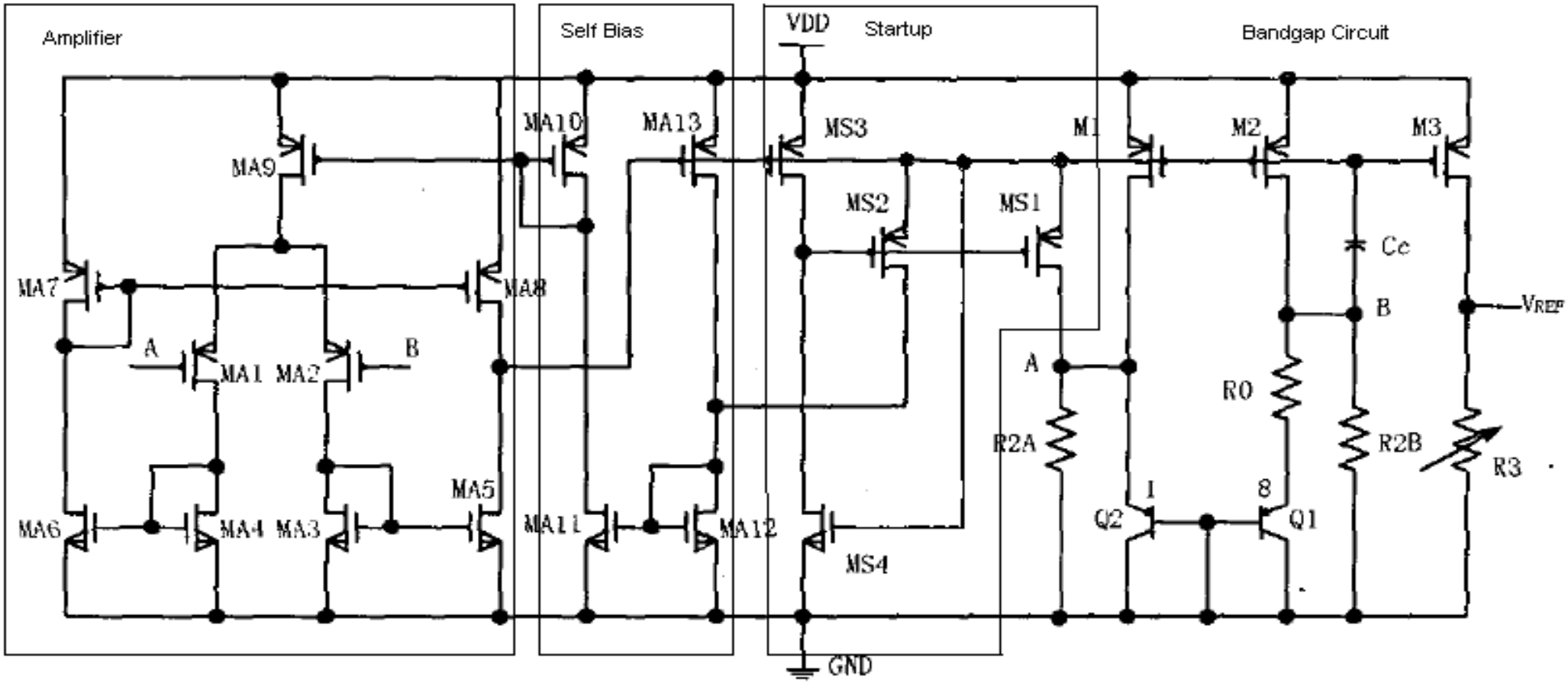
$$I_{C2} = \left(\frac{\beta_2}{1+\beta_2}\right)I_{E2} = \alpha_2 I_{E2}$$

$$V_{REF} = V_{BE2} + \frac{R_1}{R_2}\left(1 + \left(\frac{\alpha_1}{\alpha_2}\right)\frac{R_3}{R_4}\right) \bullet \left[\Delta V_{BE}\right]$$



Vref=I_3*R_3=

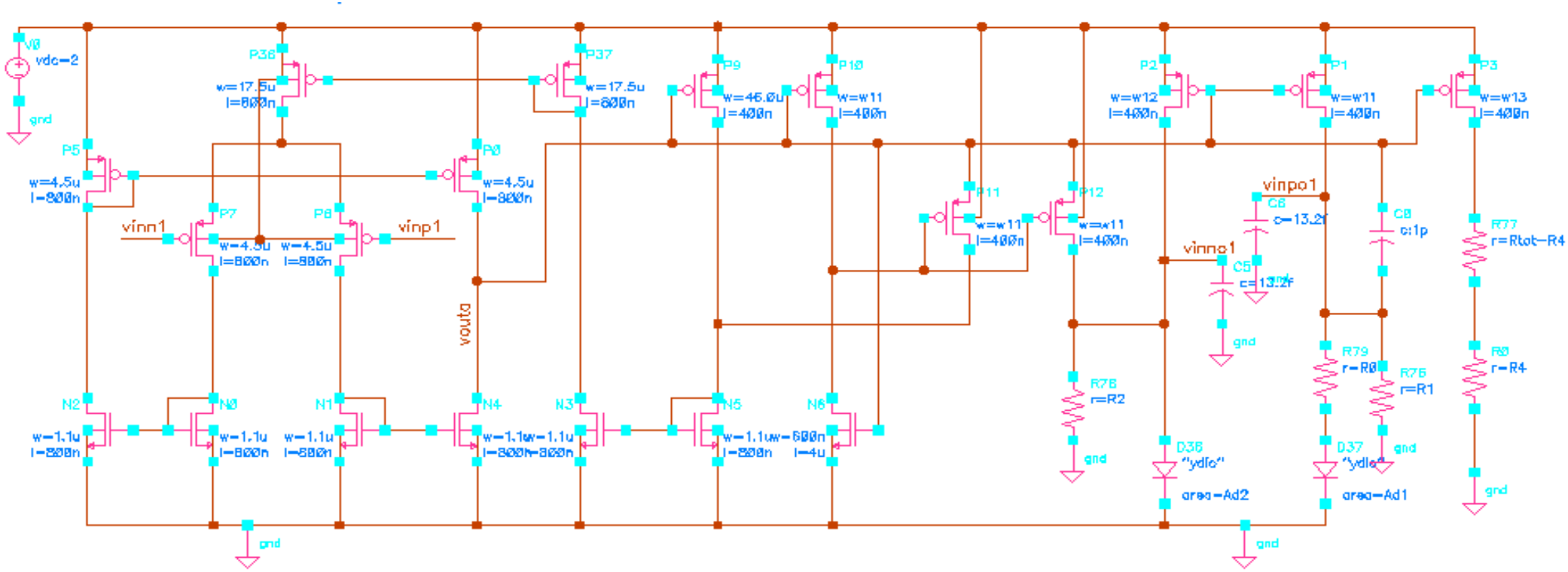
$$R_3[\frac{V_{Go}}{R_1}+(\frac{1}{R_0}\frac{k}{q}\ln(\frac{A_2}{A_1})+\frac{V_{BE}-V_{G0}}{T_o})\cdot T+\frac{m-1}{R_1 q}kT\cdot\ln(\frac{T_o}{T})]$$



Bandgap circuit formed by transistors M1, M2, M3, Q1, Q2, resistors R0, R2A, R2B, and R3.

Cc is inter-stage compensation capacitor. Think of M2 as the second stage of your two stage amplifier, then Cc is connected between output B and the input Vc.

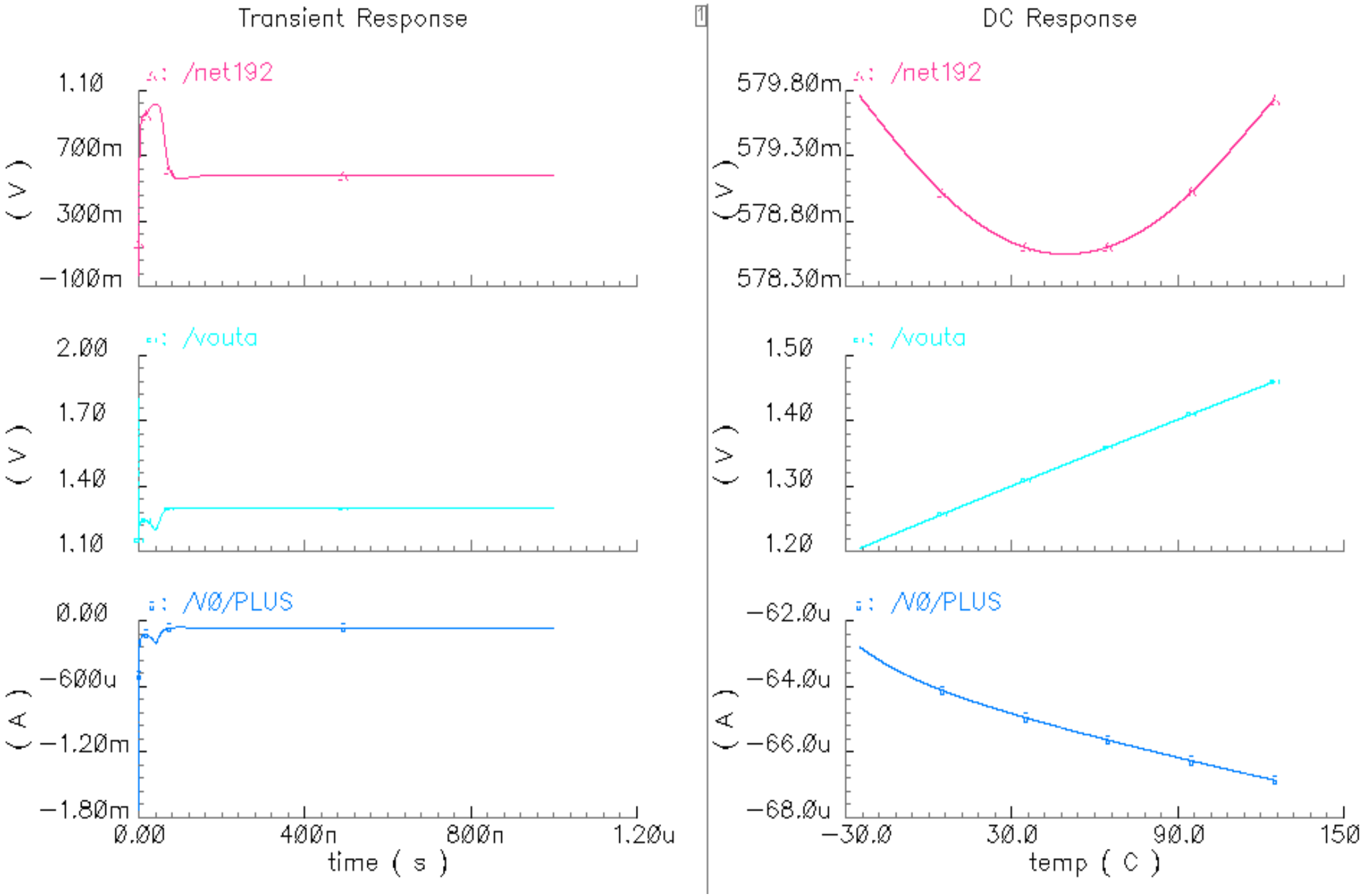
- **Amplifier:** MA1~MA9, MA9 is the tail current source, MA1 and MA2 consistent of the differential input pair of the op amp, MA3~MA6 form the current mirrors in the amplifier, MA7 converts the amplifier output to single ended, and MA5 and MA8 form the push pull output node.
  - The offset voltage of the amplifier is critical factor, ➔use large size differential input pair and careful layout; and use current mirror amplifier to reduce systematic offset.
  - 2V supple voltage is sufficient to make sure that all the transistors in the amplifier work in saturation.
  - PMOS input differential pair is used because the input common mode range (A,B nodes) is changing approximately from 0.8 to 0.6 V and in this case NMOS input pair won't work.
- **Self Bias:** MA10~MA13, a self-bias approach is used in this circuit to bias the amplifier. Bias voltage for the primary stage current source MA13 is provided by the output of the amplifier, i.e. there forms a self-feedback access from MA8 drain output to bias current source MA9 through current mirror MA10~MA13.
- **Startup Circuit:** MS1~MS4. When the output of the amplifier is close to Vdd, the circuit will not work without the start-up circuit. With the start-up circuit MS1 and MS2 will conduct current into the BG circuit and the amplifier respectively.



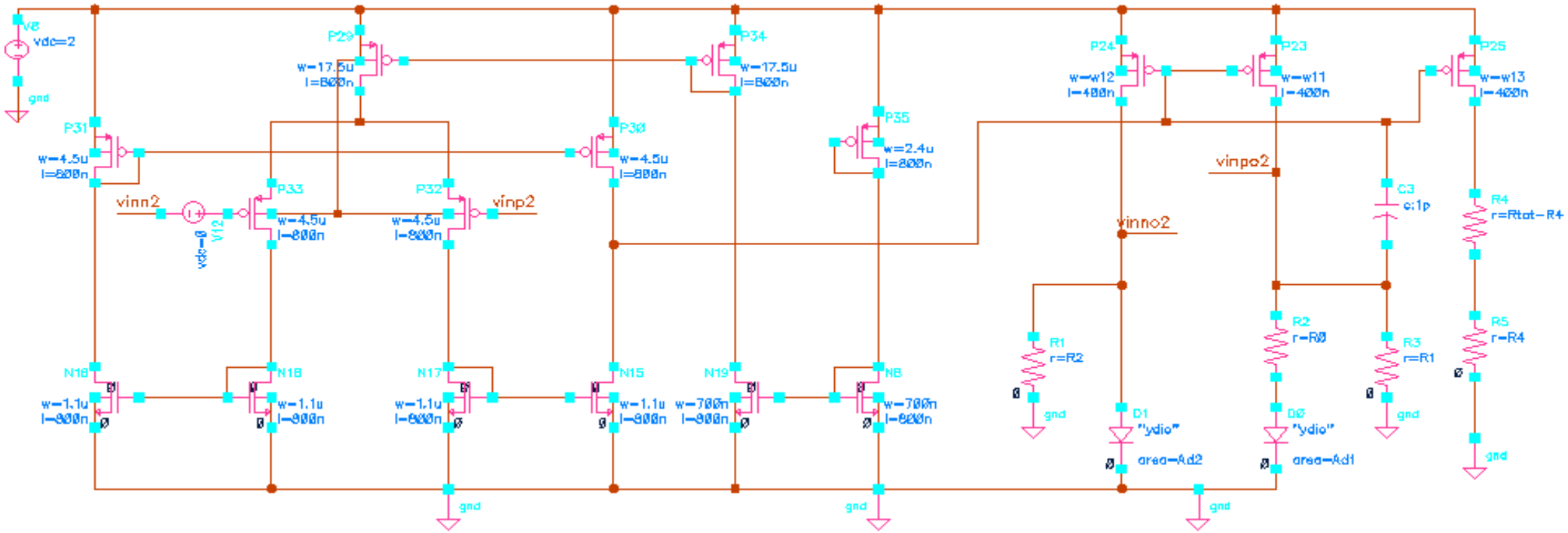
Cc is 1 pF

To have better mirror accuracy, M3 is driving a constant resistor Rtot.

Capacitors at nodes A and B are added.


Transient Response
/net192
1.1Ø
700m
300m
−100m
(V)
/vouta
2.ØØ
1.7Ø
1.4Ø
1.1Ø
(V)
/VØ/PLUS
Ø.ØØ
−6ØØu
−1.2Ø m
−1.8Ø m
(A)
Ø.ØØ
4ØØn
8ØØn
1.2Øu
time (s)
DC Response
/net192
579.8Øm
579.3Øm
578.8Øm
578.3Øm
(V)
/vouta
1.5Ø
1.4Ø
1.3Ø
1.2Ø
(V)
/VØ/PLUS
−62.Øu
−64.Øu
−66.Øu
−68.Øu
(A)
−3Ø.Ø
3Ø.Ø
9Ø.Ø
15Ø
temp (C)

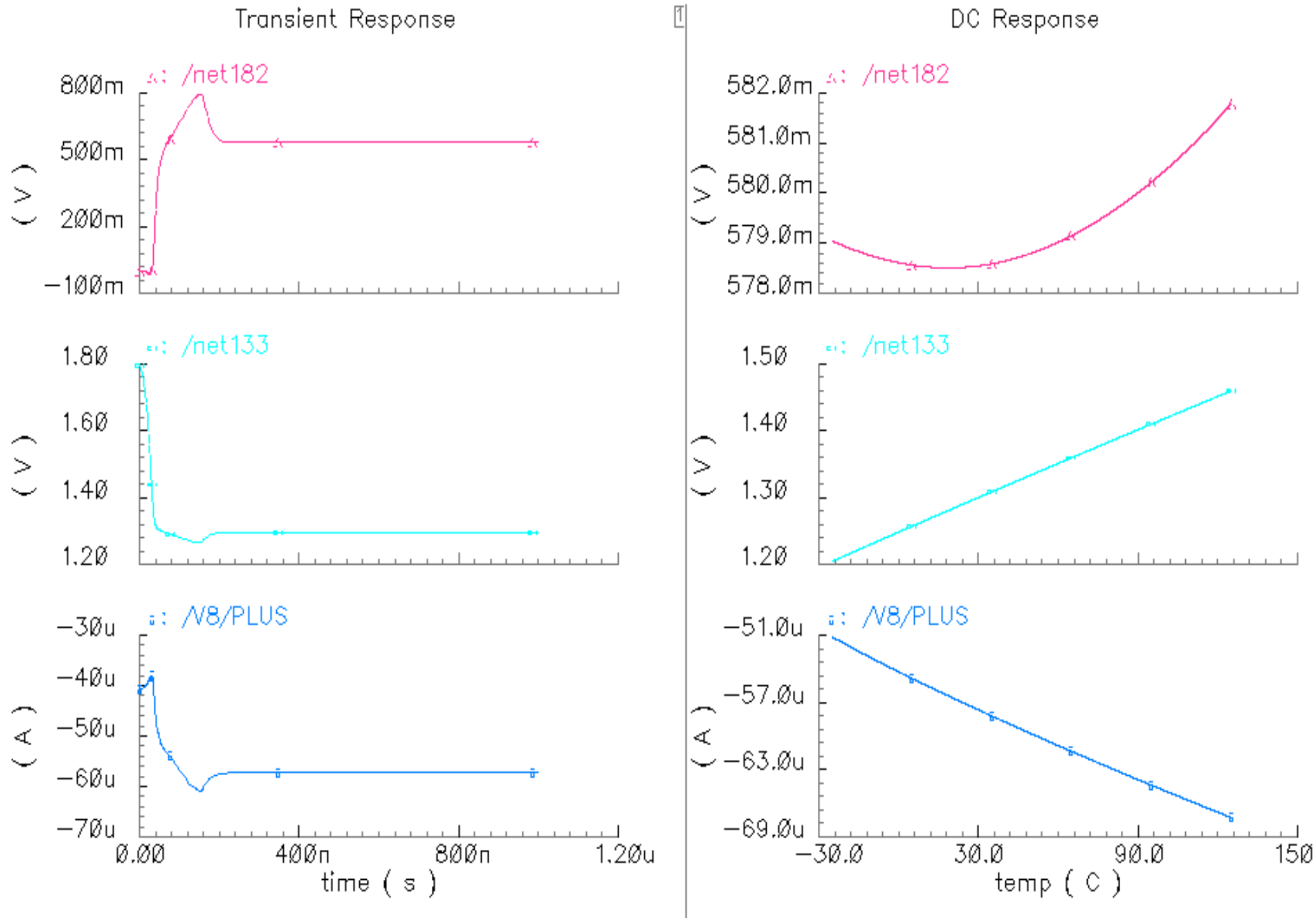
BG Circuit with simple bias circuit

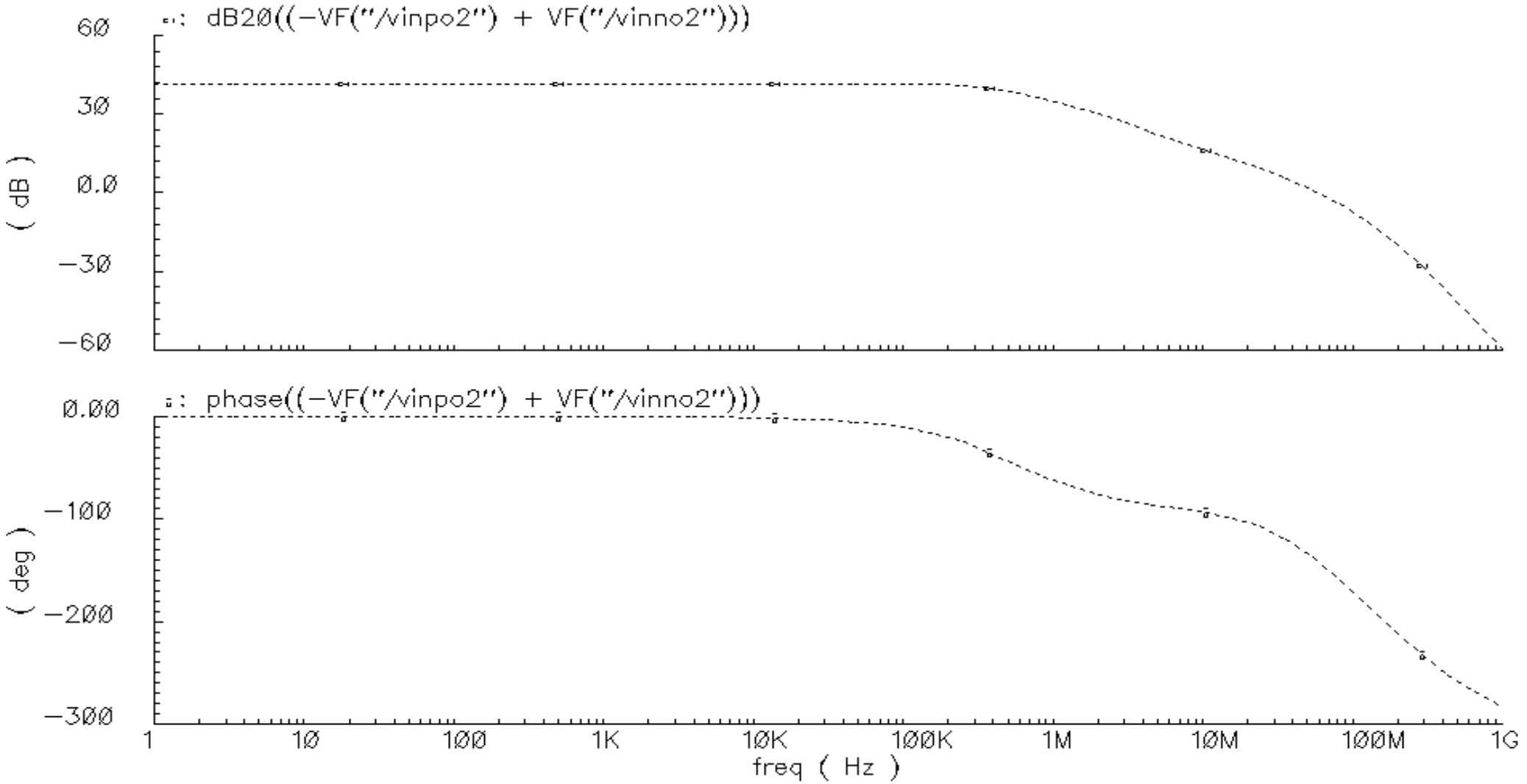


No self biasing

No startup problem, no startup circuit needed

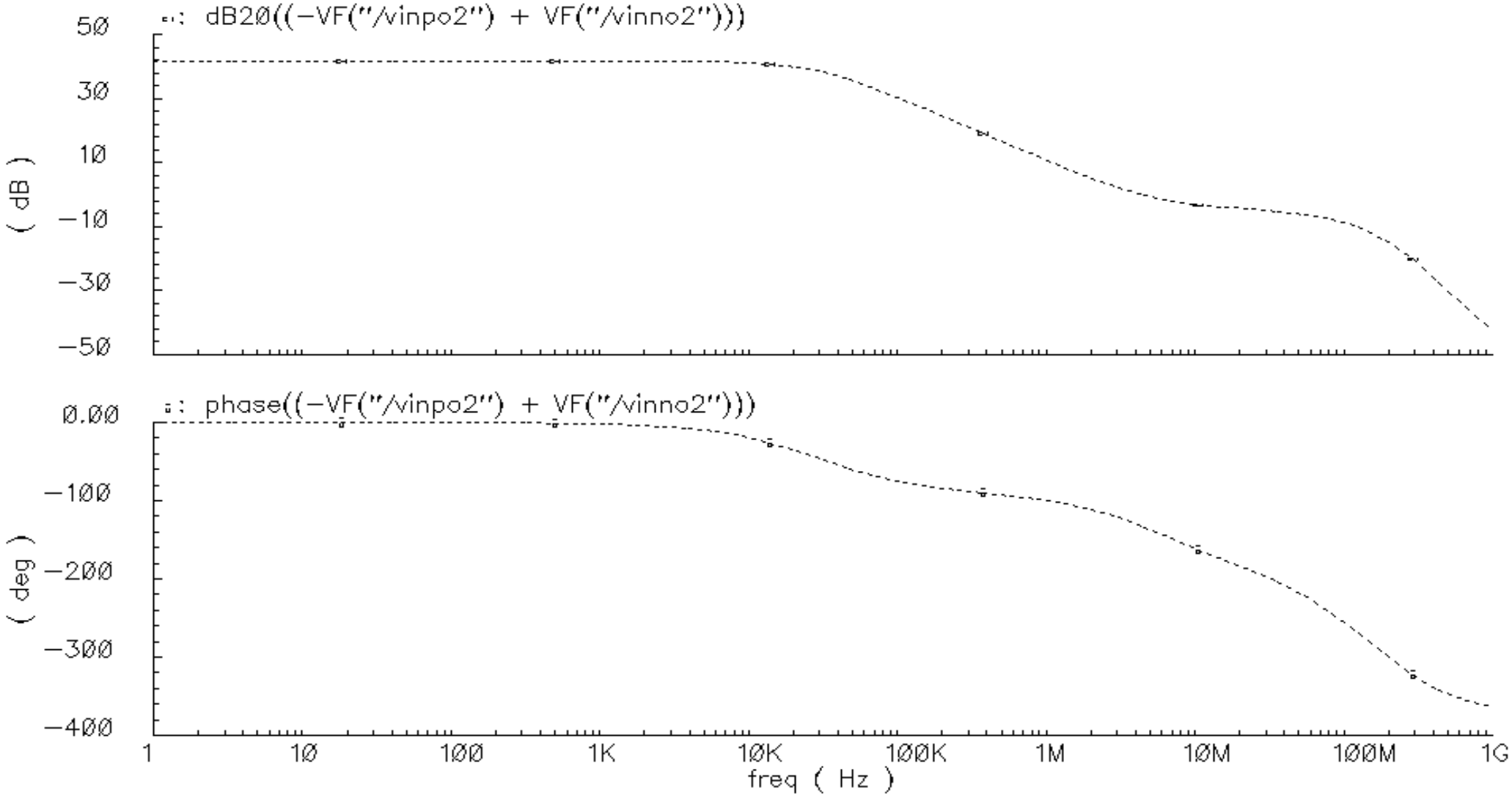
Amplifier current depends on power supply voltage


Transient Response
DC Response
/net182
/net133
/V8/PLUS
800m
500m
200m
-100m
582.0m
581.0m
580.0m
579.0m
578.0m
1.80
1.60
1.40
1.20
1.50
1.40
1.30
1.20
-30u
-40u
-50u
-60u
-70u
-51.0u
-57.0u
-63.0u
-69.0u
(V)
(A)
0.00
400n
800n
1.20u
time (s)
-30.0
30.0
90.0
150
temp (C)



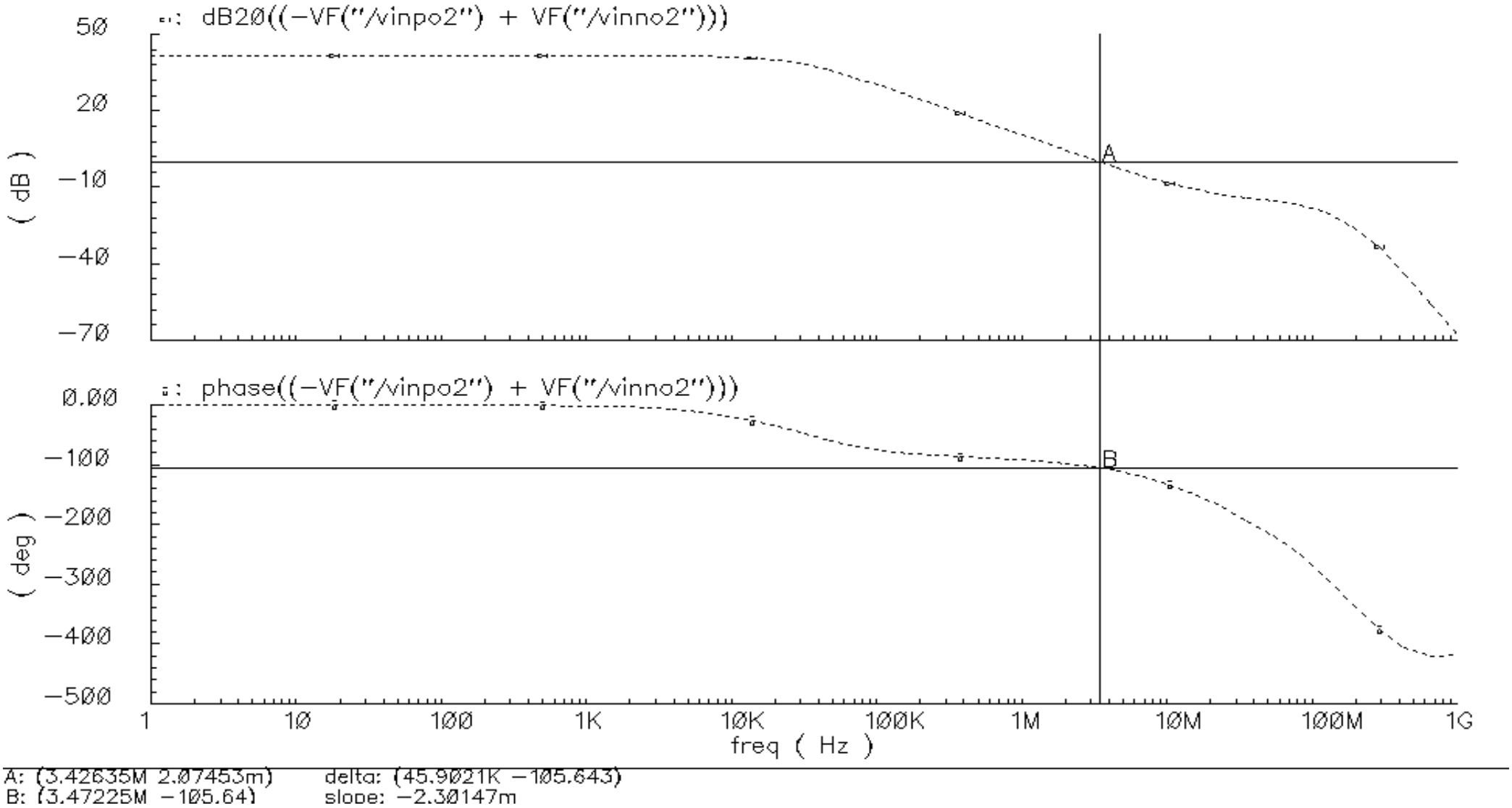
Loop gain simulation

Cc=0 F , Phase Margin = 37.86º



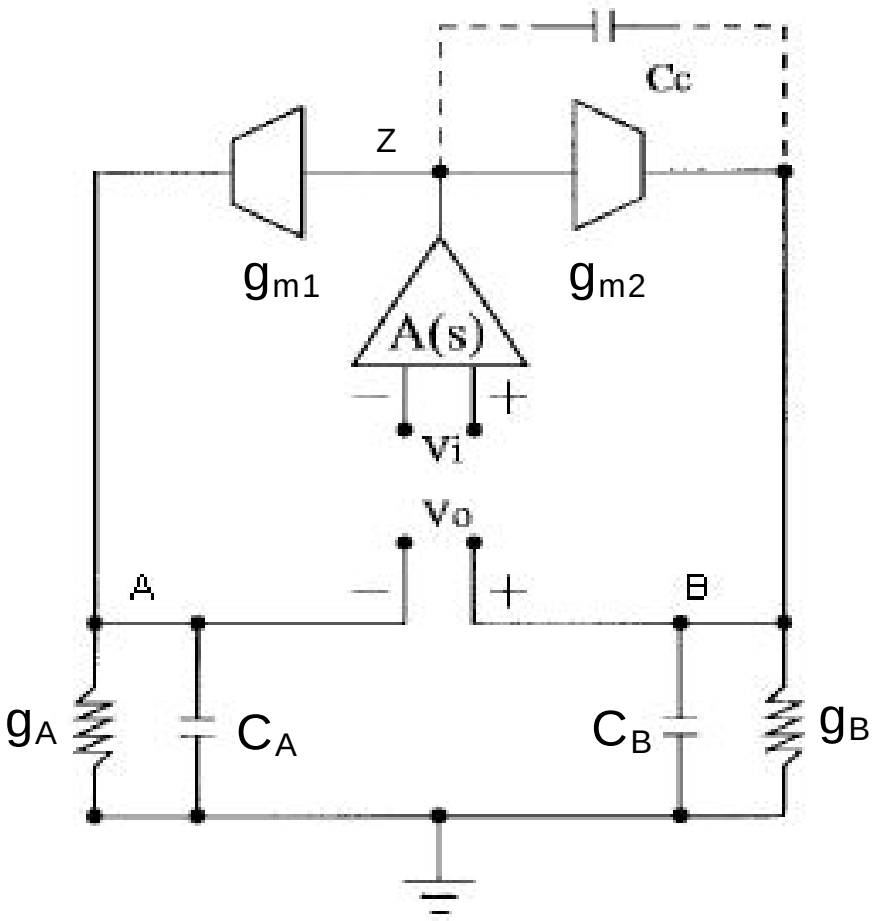
Phase Margin = 47.13º

Cc=1pF



A: (3.42635M 2.07453m) delta: (45.9Ø21K −1Ø5.643)
B: (3.47225M −1Ø5.64) slope: −2.3Ø147m

Cc+R compensation, 1pF+20kOhm
Phase Margin = 74.36º



$$A(s) = \frac{A_0}{1 + sC_Z / g_Z}$$

g_A is the total conductance of node A, and $g_A = g_{o1} + g_A'$,

g_B is the total conductance of node B, and $g_B = g_{o2} + g_B'$,

g_Z is the total conductance of node Z

C_A, C_B and C_Z are the total capacitance at nodes A, B and Z

Then the open loop transfer function from $V_{i+/-}$ to $V_{o+/-}$ is

$$H_{OL}(s) = \frac{v_o(s)}{v_i(s)} = \frac{A_0 g_m (g_A' - g_B')}{g_o(g_o + g_A')} \times \frac{1 + s(C_A - C_B)/(g_A' - g_B')}{(1 + s/p_A)(1 + s/p_B)(1 + s/p_Z)}$$

$$p_Z = \frac{g_Z}{C_Z}, p_B = \frac{g_B}{C_B} = \frac{(g_o + g_B')}{C_B}, p_A = \frac{g_A}{C_A} = \frac{(g_o + g_A')}{C_A}$$

The transfer function with C_C in place is

$$H_{OL}(s) = \frac{A_0 g_m (g_A' - g_B')}{(g_o + g_A')(g_o + g_B')} \times \frac{(1 - s_{Z1})(1 + s_{Z2})}{(1 + s/p_A)(1 + s/p_B')(1 + s/p_Z')}$$

$$z_1 = \frac{g_A' - g_B'}{C_C} \times \frac{g_m}{g_m + g_A'}$$

$$p_B' = \frac{g_m}{C_A + C_B}$$

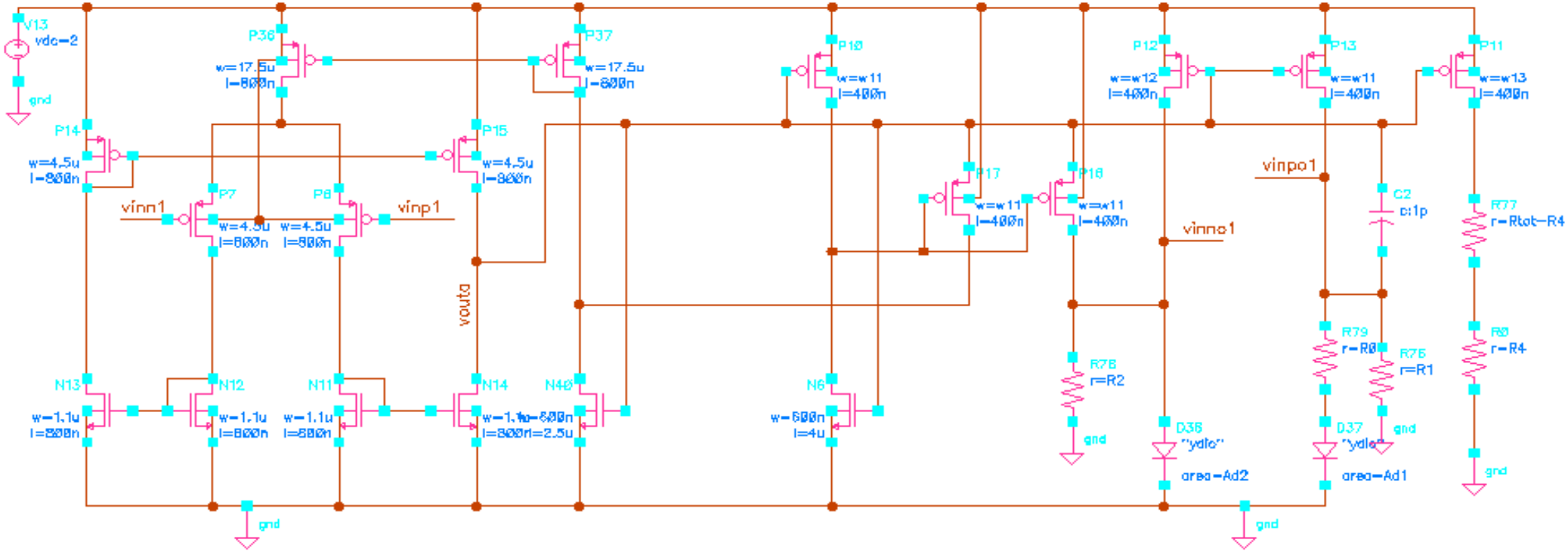
$$z_2 = \frac{g_m}{C_B}$$

$$p_Z' = \frac{g_Z g_o}{g_m C_C}$$

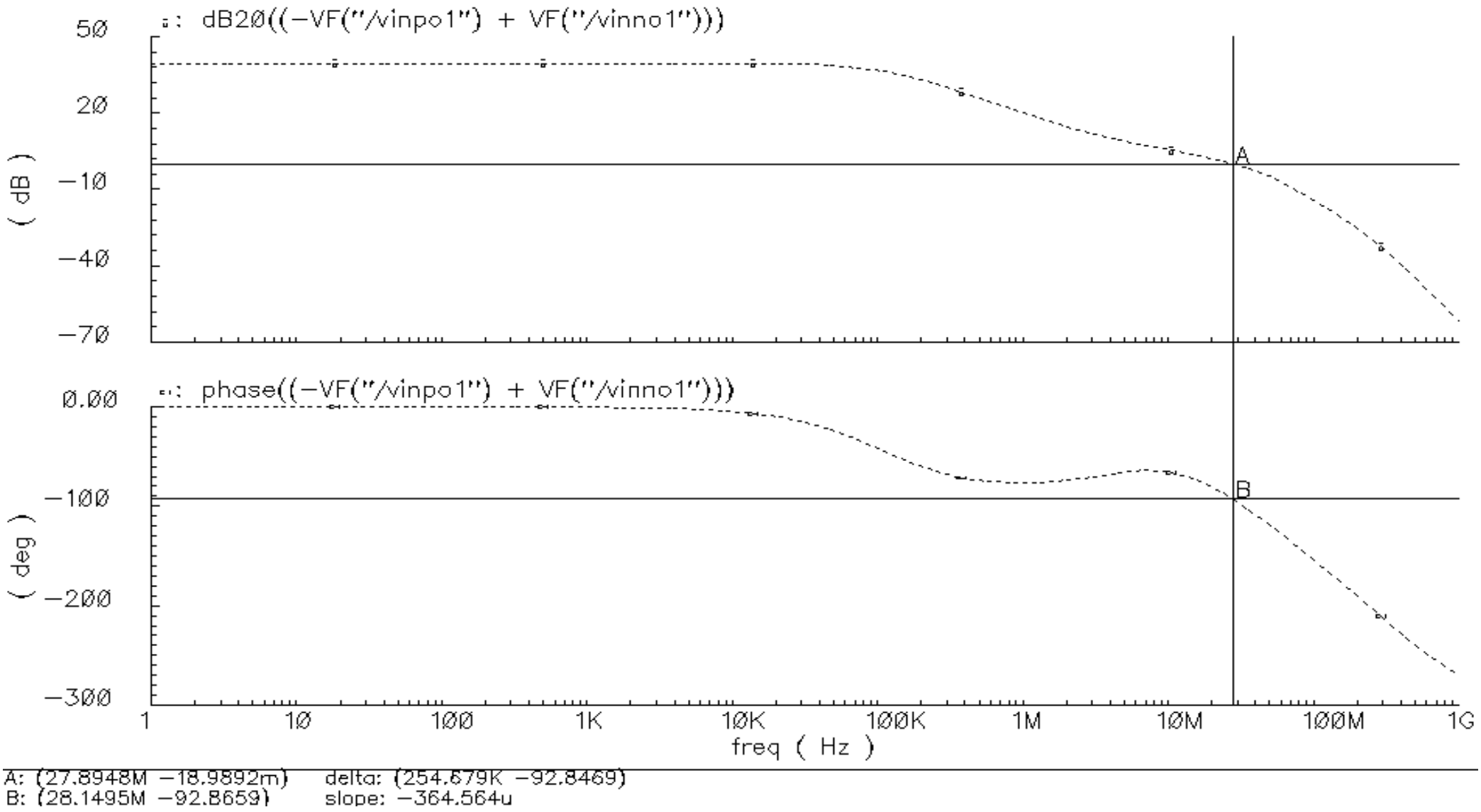
a nulling resistor R_C can be added in series with C_C to push z_1 to higher frequency

$$z_1 = \frac{1}{CC\,(1/g_m + 1/g_A' - R_C)}$$

BG Circuit 3 with modified self-biasd circuit

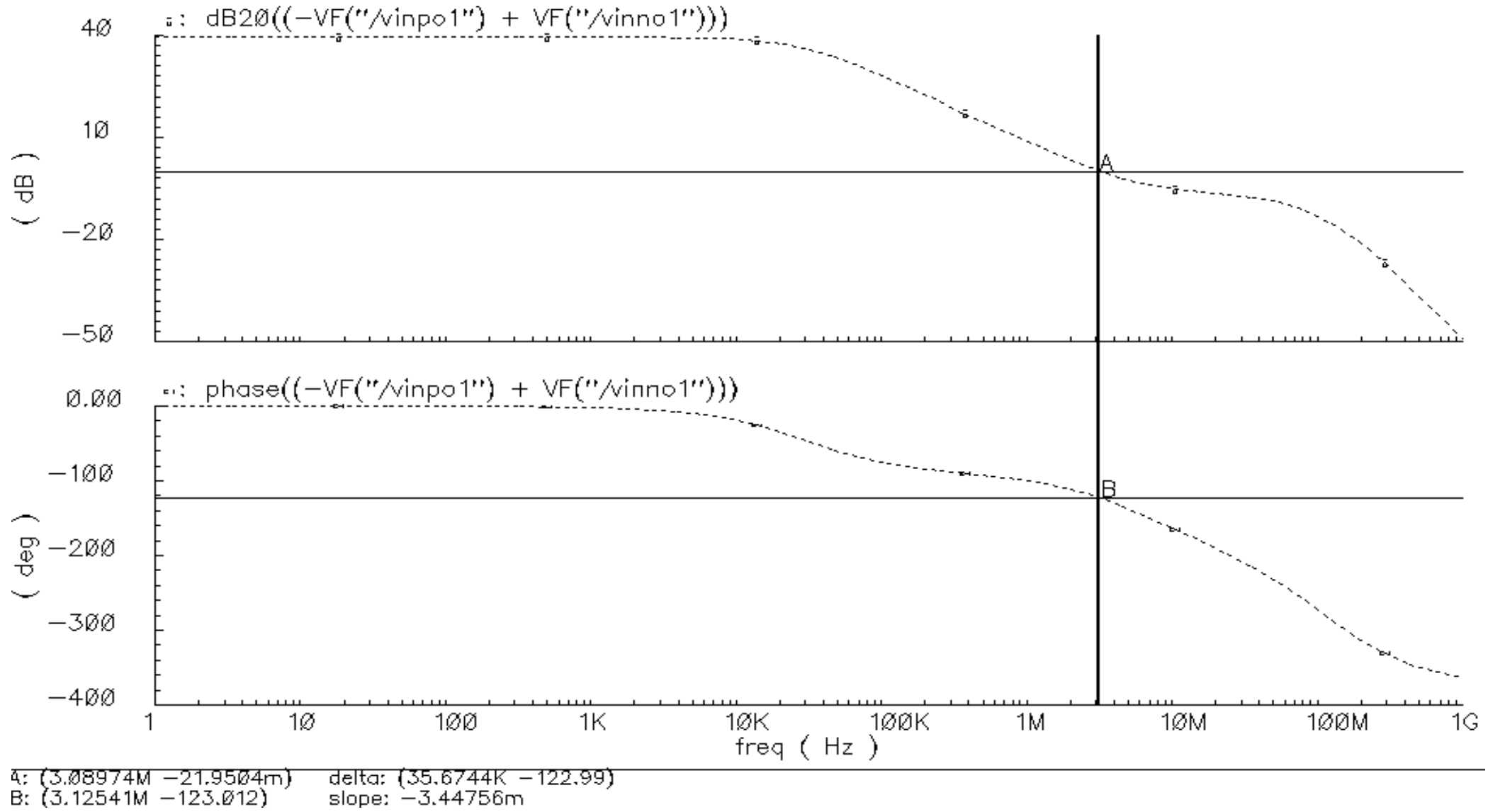


Reduce one transistor in the self-biased loop to change the type of the feedback



A: (27.8948M −18.9892m) delta: (254.679K −92.8469)
B: (28.1495M −92.8659) slope: −364.564u

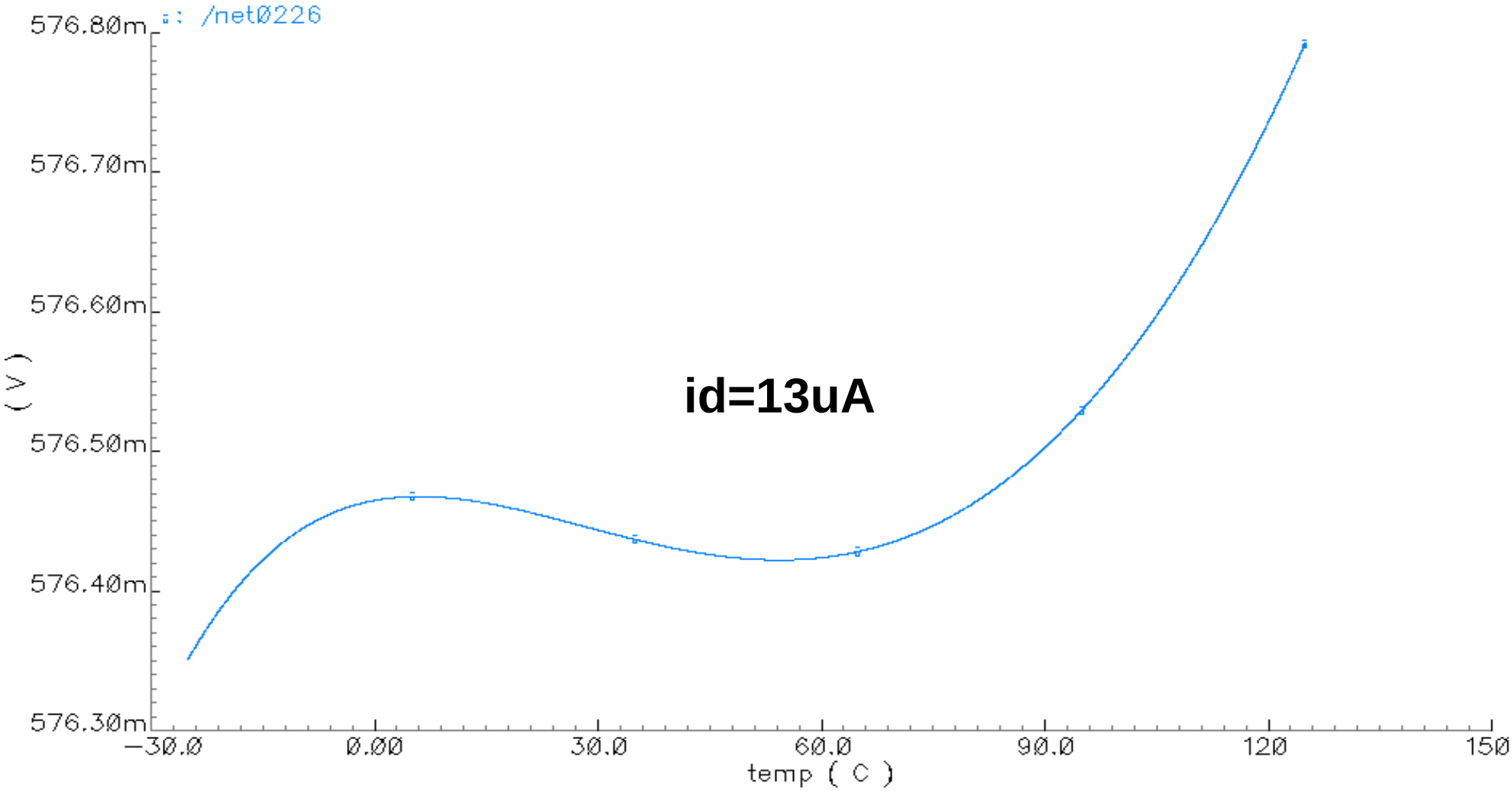
With Cc=0, Phase Margin = 87.13º



A: (3.08974M −21.9504m) delta: (35.6744K −122.99)
B: (3.12541M −123.012) slope: −3.44756m

Cc=1 pF, Phase Margin = 56.99^{o}
Lower bandwidth

BG Simulation for different diode current



Characterization of a bandgap circuit

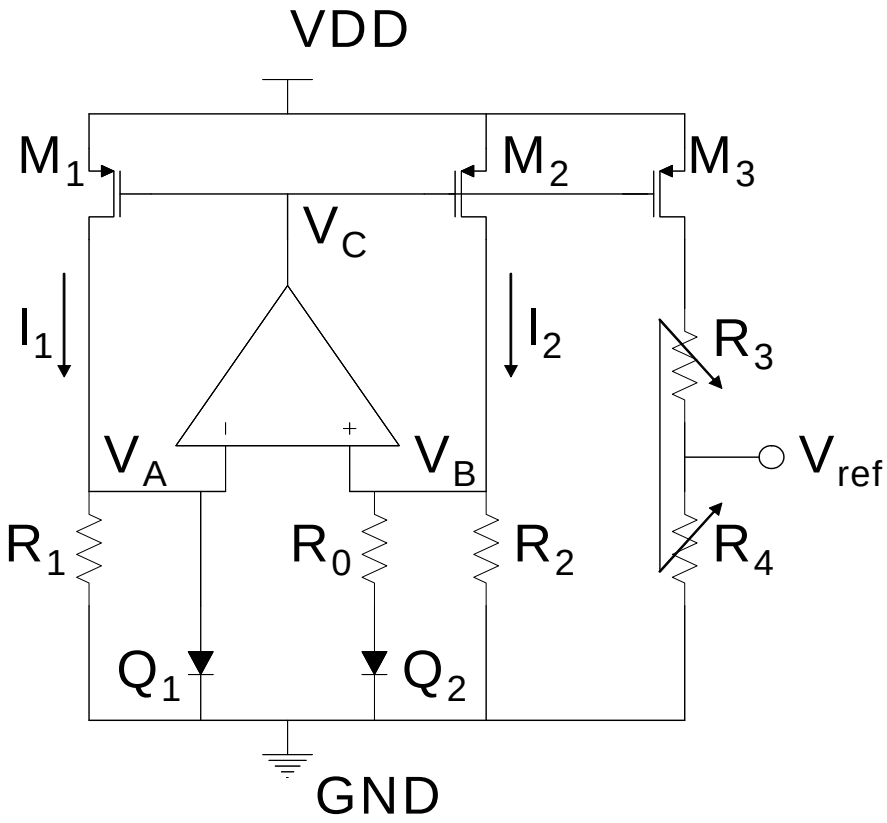
Assuming an ideal op amp with an infinite gain, we have $V_A = V_B$ and $I_1 = I_2$.

$$\frac{V_A}{R_1} + I_{C1} = \frac{V_A}{R_2} + I_{C2},$$

$$V_A = V_{BE2} + I_{C2} R_0.$$

$$I_{C1} = \sigma A_1 T^m \exp\left(\frac{V_A - V_G}{kT/q}\right),$$

$$I_{C2} = \sigma A_2 T^m \exp\left(\frac{V_{BE2} - V_G}{kT/q}\right),$$



Schematic of the current-mode bandgap circuit

$$V_G = V_{G0} - \frac{\alpha T^2}{T+\beta} = V_{G0} - \alpha T + \frac{\alpha\beta}{T+\beta}$$

For the silicon, $\alpha = 7.021\times10^{-4} V/K$, $\beta = 1108K$, $V_G(0) = 1.17V$

Since $R_1 = R_2$, we know $I_{C1} = I_{C2}$. Solving for V_{be2}:

$$\sigma A_1 T^m \exp(\frac{V_A - V_G}{kT/q}) = \sigma A_2 T^m \exp(\frac{V_{BE2} - V_G}{kT/q}),$$

$$\Rightarrow \quad V_{BE2} = V_A + (kT/q)\ln\frac{A_1}{A_2}.$$

Substituting back

$$V_A = V_A + (kT/q)\ln\frac{A_1}{A_2} + R_0\sigma A_1 T^m \exp(\frac{V_A - V_G}{kT/q}),$$

$$\Rightarrow \quad V_A = \frac{kT}{q}\ln(\frac{k}{qR_0\sigma A_1 T^{m-1}}\ln\frac{A_2}{A_1}) + V_G,$$

$$I_{C1} = \frac{kT}{qR_0} \ln \frac{A_2}{A_1}.$$

We know $I_1 = I_{C1} + V_A / R_1$. That gives

$$I_1 = \frac{kT}{qR_0} \ln \frac{A_2}{A_1} + \frac{kT}{qR_1} \ln\left(\frac{k}{qR_0 \sigma A_1 T^{m-1}} \ln \frac{A_2}{A_1}\right) + \frac{V_G}{R_1}.$$

Take partial derivative of I_1 with respect to temperature

$$\frac{\partial I_1}{\partial T} = \frac{k}{qR_0} \ln \frac{A_2}{A_1} + \frac{k}{qR_1} \ln\left(\frac{k}{qR_0 \sigma A_1 T^{m-1}} \ln \frac{A_2}{A_1}\right) - \frac{k(m-1)}{qR_1} - \frac{\alpha}{R_1} - \frac{\alpha\beta}{(T+\beta)^2 R_1}.$$

For a given temperature, set the above to 0 and solve for R1. That tells you how to select R1 in terms of temperature, area ratio, and R0.

Other quantities are device or process parameters.

In most literature, the last two items are ignored, that allows solution of inflection temperature T0 in terms of R0, R1, area ratio:

$$T_0 = \exp[\frac{1}{m-1}\ln(\frac{k}{qR_0\sigma A_1}\ln\frac{A_2}{A_1}) + \frac{1}{m-1}\frac{R_1}{R_0}\ln\frac{A_2}{A_1} - 1]$$

$$= (\frac{k}{qR_0\sigma A_1}\ln\frac{A_2}{A_1})^{\frac{1}{m-1}}(\frac{A_2}{A_1})^{\frac{1}{m-1}\frac{R_1}{R_0}} e^{-1}.$$

The current at the inflection point is

$$I_1\Big|_{T=T_0} = \frac{kT_0}{qR_1}\{[1-\frac{R_1}{R_0}\ln(\frac{A_2}{A_1})] + m - 1\} + \frac{V_{G0}}{R_1}.$$

Curvature and sensitivity

The second-order partial derivative of I_1 wrpt T is

$$\frac{\partial^2 I_1}{\partial T^2} = \frac{-k(m-1)}{qR_1 T} - \frac{2\alpha\beta}{(T+\beta)^3 R_1}.$$

Notice that under a specific temperature, the second-order derivative is inversely proportional to the resistance R_1. We would like to have small variation of I_1 around T_{INF}, so it is preferable to have a large R_1.

Denote the first derivative of I1 by

$$f(T_{INF}, R_0, R_1)$$

$$= \frac{k}{qR_0}\ln\frac{A_2}{A_1} + \frac{k}{qR_1}\ln\left(\frac{k}{qR_0\sigma A_1 T_{INF}^{m-1}}\ln\frac{A_2}{A_1}\right) - \frac{k(m-1)}{qR_1} - \frac{2\alpha T_{INF}}{(T_{INF}+\beta)R_1} + \frac{\alpha T_{INF}^2}{(T_{INF}+\beta)^2 R_1}$$

➔

$$\frac{\partial f}{\partial T_{INF}} = \frac{-k(m-1)}{qR_1 T_{INF}} - \frac{2\alpha\beta}{(T_{INF}+\beta)^3 R_1},$$

$$\frac{\partial f}{\partial R_0} = -\frac{k}{qR_0}\left(\frac{1}{R_0}\ln\frac{A_2}{A_1} + \frac{1}{R_1}\right),$$

$$\frac{\partial f}{\partial R_1} = -\frac{1}{R_1^2}\left[\frac{k}{q}\ln\left(\frac{k}{qR_0\sigma A_1 T_{INF}^{m-1}}\ln\frac{A_2}{A_1}\right) - \frac{k(m-1)}{q} - \frac{2\alpha T_{INF}}{T_{INF}+\beta} + \frac{\alpha T_{INF}^2}{(T_{INF}+\beta)^2}\right]$$

$$= \frac{k}{qR_0 R_1}\ln\frac{A_2}{A_1}.$$

The sensitivity of T_{INF} wrpt R_0 and R_1 are

$$S_{R0}^{TINF} = \frac{\partial T_{INF}}{\partial R_0}\frac{R_0}{T_{INF}} = -\frac{\partial f/\partial R_0}{\partial f/\partial T_{INF}}\frac{R_0}{T_{INF}} = \frac{-k(\frac{R_1}{R_0}\ln\frac{A_2}{A_1}+1)(T_{INF}+\beta)^3}{k(m-1)(T_{INF}+\beta)^3+2q\alpha\beta^2 T_{INF}},$$

$$S_{R1}^{TINF} = \frac{\partial T_{INF}}{\partial R_1}\frac{R_1}{T_{INF}} = -\frac{\partial f/\partial R_1}{\partial f/\partial T_{INF}}\frac{R_1}{T_{INF}} = \frac{k\frac{R_1}{R_0}\ln\frac{A_2}{A_1}(T_{INF}+\beta)^3}{k(m-1)(T_{INF}+\beta)^3+2q\alpha\beta^2 T_{INF}}.$$

For R_1 = 13.74 KOhm and R_0 = 1 KOhm, the sensitivity wrpt R_0 is about -6.75, and about 6.5 wrpt R_1, when A_2/A_1 is equal to 8.

Effects of mismatch errors and the finite op amp gain

First, suppose current mirror mismatch leads to mismatch between Ic1 and Ic2. In particular, suppose:

$$I_{C1} = I_{C2} + \delta_I' = I_{C2}\exp(\delta_I),$$

$$V_A + \delta_V = V_{BE2} + I_{C2}R_0,$$

➔

$$V_{BE2} = V_A - (kT/q)(\ln\frac{A_2}{A_1} + \delta_I).$$

Re-solve for V_A

$$V_A = \frac{kT}{q}\{\ln[\frac{k}{qR_0\sigma A_1 T^{m-1}}(\ln\frac{A_2}{A_1} + \delta_I) + \frac{\delta_V}{R_0\sigma A_1 T^r}] + \delta_I\} + V_G.$$

Finally we get

$$I_1 = \frac{1}{R_0}[\frac{kT}{q}(\ln\frac{A_2}{A_1} + \delta_I) + \delta_V]\exp(\delta_I)$$

$$+ \frac{kT}{qR_1}\{\ln\frac{1}{R_0\sigma A_1 T^m}[\frac{kT}{q}(\ln\frac{A_2}{A_1} + \delta_I) + \delta_V] + \delta_I\} + \frac{V_G}{R_1},$$

the first line is I_{C1} and the second is V_A/R_1

The derivative of I_1 wrpt T becomes

$$\frac{\partial I_1}{\partial T} = \frac{k\exp(\delta_I)}{qR_0}(\ln\frac{A_2}{A_1} + \delta_I) + \frac{k}{qR_1}\{\ln\frac{1}{R_0\sigma A_1 T^m}[\frac{kT}{q}(\ln\frac{A_2}{A_1} + \delta_I) + \delta_V] + \delta_I\}$$

$$- \frac{k}{qR_1}[m - \frac{kT(\ln A_2/A_1 + \delta_I)}{kT(\ln A_2/A_1 + \delta_I) + q\delta_V}] - \frac{2\alpha T}{(T+\beta)R_1} + \frac{\alpha T^2}{(T+\beta)^2 R_1}.$$

Define similar to before:

$$f(T_{INF}, R_0, R_1, \delta_I, \delta_V) = \frac{k}{qR_0}(\ln\frac{A_2}{A_1} + \delta_I)\exp(\delta_I)$$

$$+ \frac{k}{qR_1}\{\ln\frac{1}{R_0\sigma A_1 T_{INF}^m}[\frac{kT_{INF}}{q}(\ln\frac{A_2}{A_1} + \delta_I) + \delta_V] + \delta_I\}$$

$$- \frac{k}{qR_1}[m - \frac{kT_{INF}(\ln A_2/A_1 + \delta_I)}{kT_{INF}(\ln A_2/A_1 + \delta_I) + q\delta_V}] - \frac{2\alpha T_{INF}}{(T_{INF} + \beta)R_1} + \frac{\alpha T_{INF}^2}{(T_{INF} + \beta)^2 R_1} = 0.$$

we can calculate

$$\frac{\partial f}{\partial \delta_I}(\delta_I = \delta_V = 0) = \frac{k}{qR_0}(\ln\frac{A_2}{A_1} + 1) + \frac{k}{qR_1}(\frac{1}{\ln A_2/A_1} + 1),$$

$$\frac{\partial f}{\partial \delta_V}(\delta_I = \delta_V = 0) = 0.$$

The sensitivity of T_{INF} wrpt the current mismatch is

$$S_{\delta I}^{TINF} = -\frac{\partial f / \partial \delta_I}{\partial f / \partial T_{INF}} \frac{1}{T_{INF}} = \frac{\frac{R_1}{R_0}(\ln \frac{A_2}{A_1} + 1) + (\frac{1}{\ln A_2 / A_1} + 1)}{k(m-1)(T_{INF} + \beta)^3 + 2q\alpha\beta^2 T_{INF}} k(T_{INF} + \beta)^3.$$

This sensitivity is larger than those wrpt the resistances.

That requires the current mismatch be controlled in an appropriate region so that the resistances can be used to effectively tune the temperature at the inflection point.

The sensitivity of T_{INF} wrpt the voltage difference is

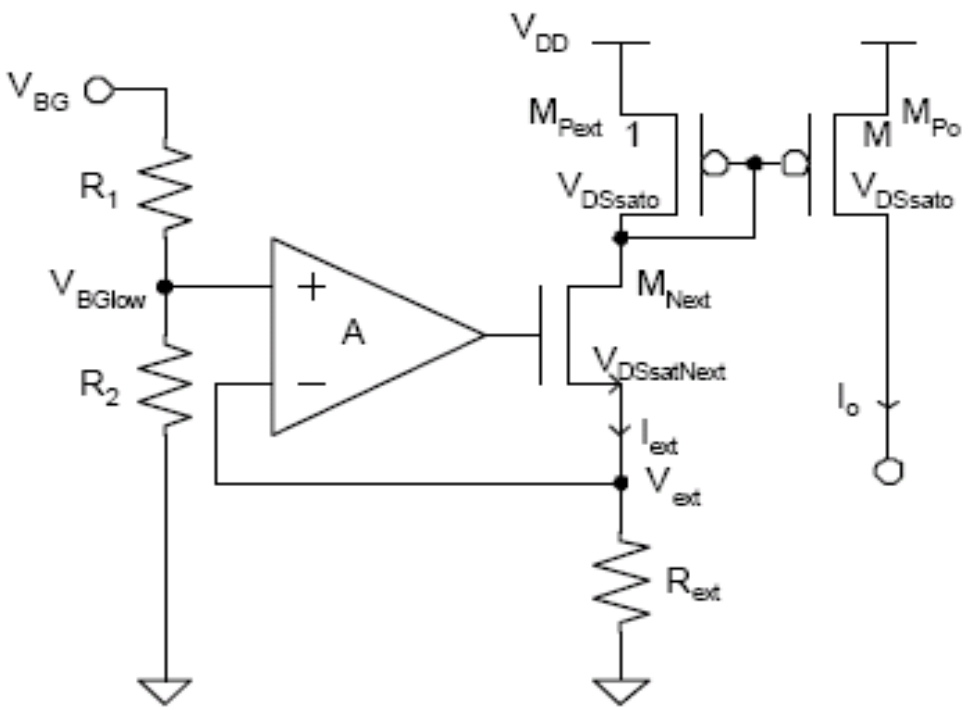
$$S_{\delta V}^{TINF} = 0,$$

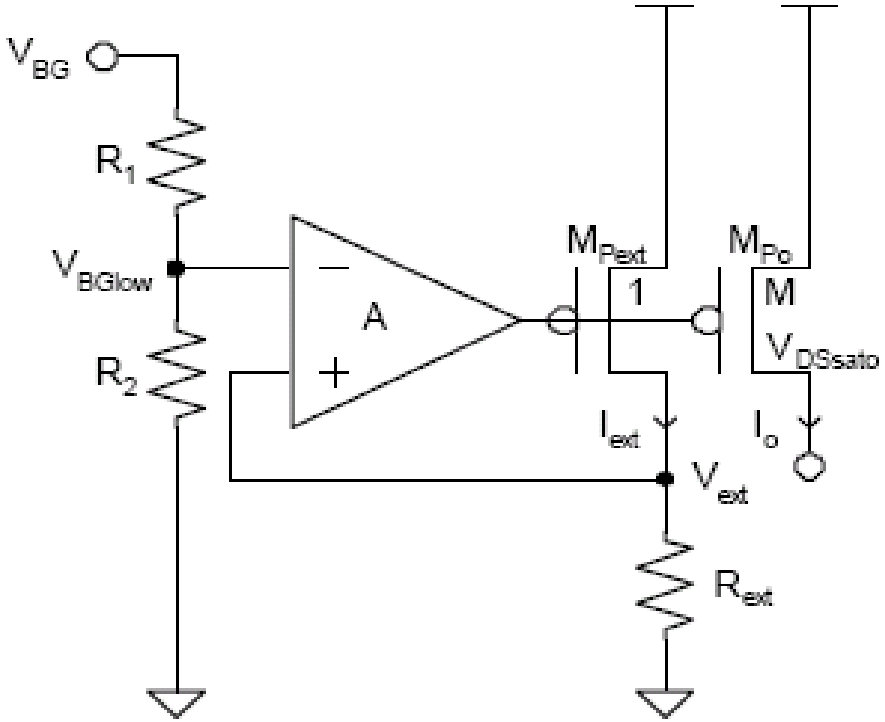
which means the inflection point temperature is not very sensitive to the voltage difference.

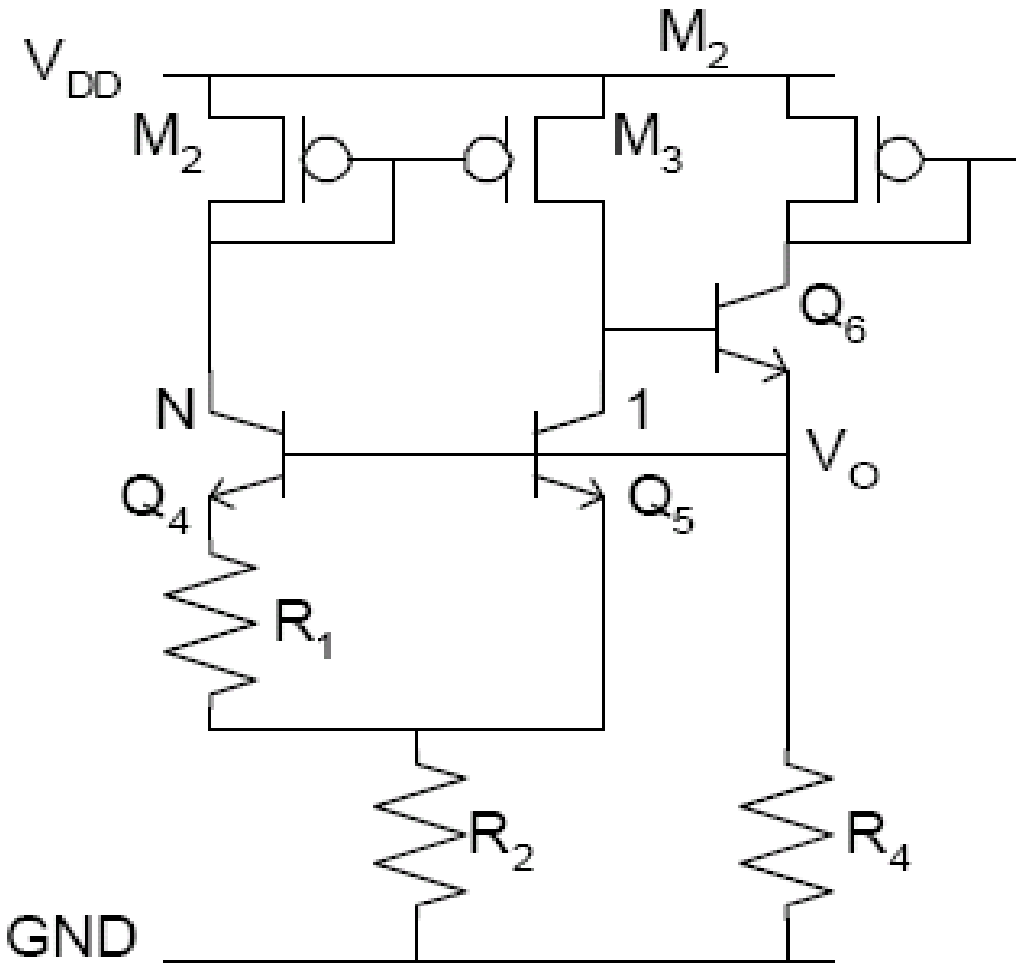
$$\frac{\partial f}{\partial \delta_I} = \frac{k}{qR_0}(\ln \frac{A_2}{A_1} + \delta_I + 1)\exp(\delta_I)$$

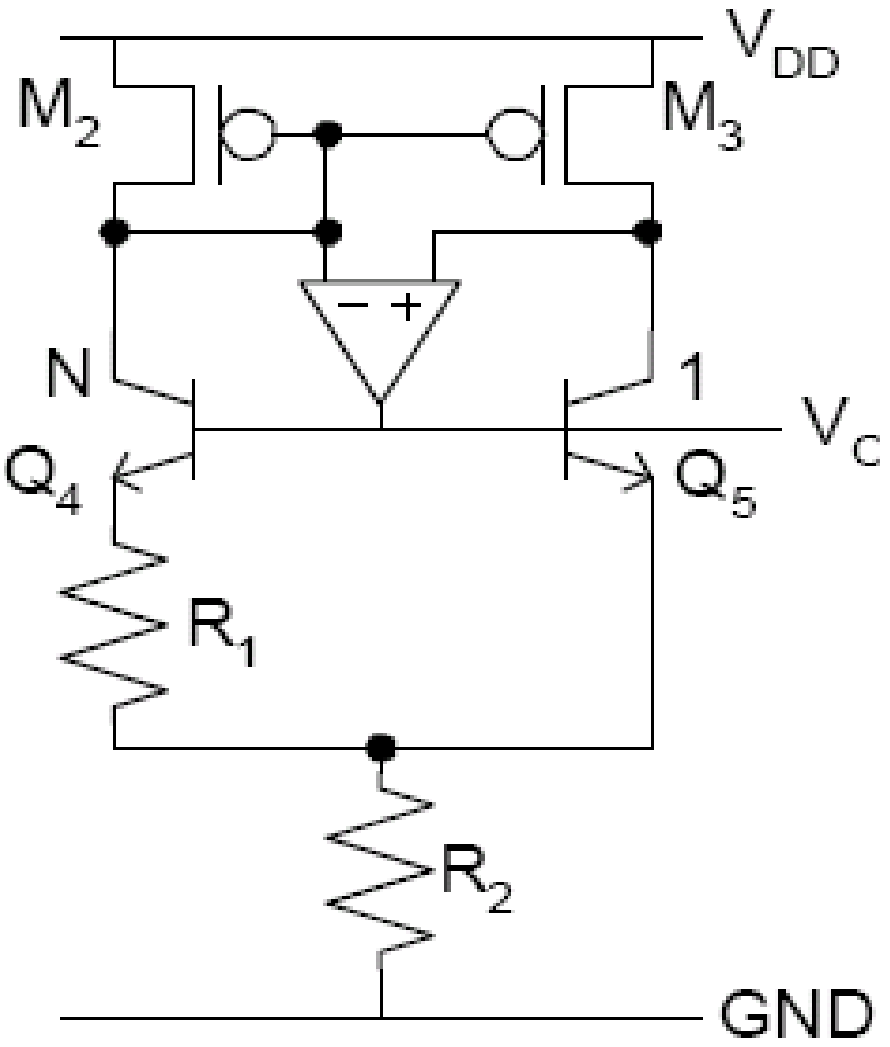
$$+ \frac{k}{qR_1}[1 + \frac{kT_{INF}}{kT_{INF}(\ln A_2/A_1 + \delta_I) + q\delta_V} + \frac{q\delta_V kT_{INF}}{[kT_{INF}(\ln A_2/A_1 + \delta_I) + q\delta_V]^2}]$$

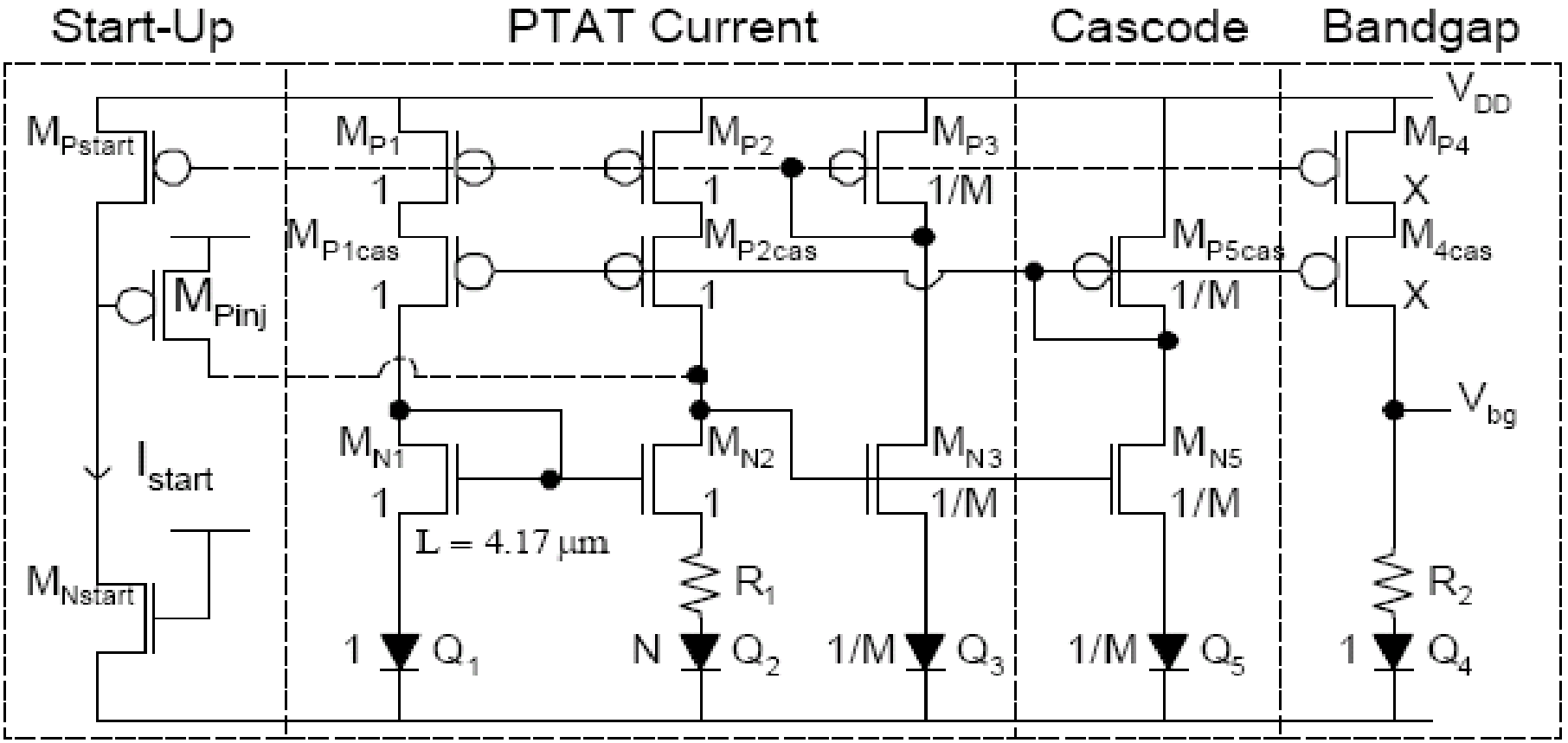
$$\frac{\partial f}{\partial \delta_V} = \frac{k}{R_1}\frac{q\delta_V}{[kT_{INF}(\ln A_2/A_1 + \delta_I) + q\delta_V]^2}$$

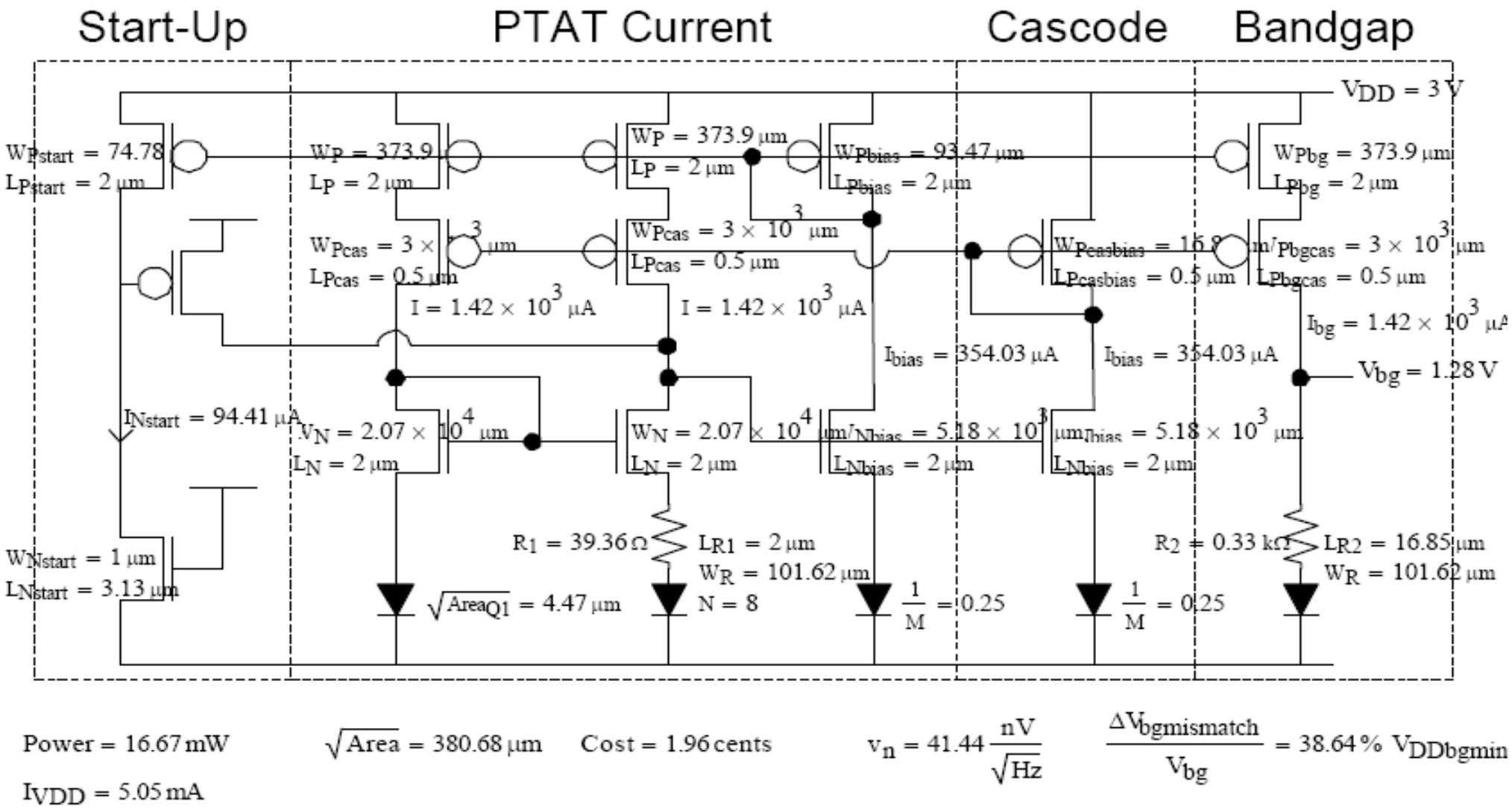

V_{DD}
V_{BG}
M_{Pext}
1
M
M_{Po}
R_1
V_{DSsato}
V_{DSsato}
V_{BGlow}
M_{Next}
A
$V_{DSsatNext}$
R_2
I_o
I_{ext}
V_{ext}
R_{ext}


V_{BG}
R_1
M_{Pext}
M_{Po}
1
M
V_{BGlow}
A
V_{DSsato}
R_2
I_{ext}
I_o
V_{ext}
R_{ext}


V_{DD}
M_2
M_2
M_3
Q_6
N
1
V_O
Q_4
Q_5
R_1
R_2
R_4
GND


V_{DD}
M_2
M_3
N
1
V_C
Q_4
Q_5
R_1
R_2
GND


Start-Up
PTAT Current
Cascode
Bandgap
V_{DD}
M_{Pstart}
M_{P1}
M_{P2}
M_{P3}
M_{P4}
1
1
1/M
X
M_{P1cas}
M_{P2cas}
M_{P5cas}
M_{4cas}
M_{Pinj}
1
1
1/M
X
V_{bg}
I_{start}
M_{N1}
M_{N2}
M_{N3}
M_{N5}
1
1
1/M
1/M
L = 4.17 µm
R_1
R_2
M_{Nstart}
1 Q_1
N Q_2
1/M Q_3
1/M Q_5
1 Q_4



Power = 16.67 mW

$\sqrt{Area} = 380.68\,\mu m$

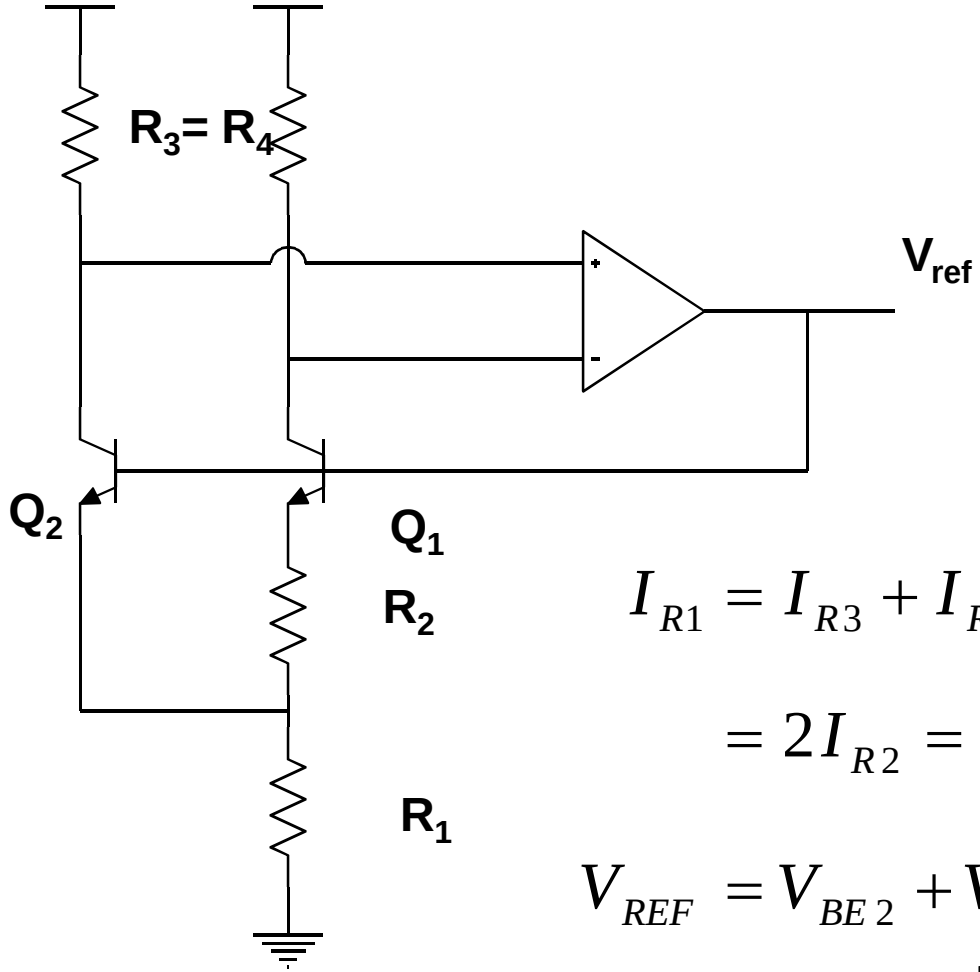
Cost = 1.96 cents

$v_n = 41.44\,\frac{nV}{\sqrt{Hz}}$

$\frac{\Delta V_{bgmismatch}}{V_{bg}} = 38.64\%\ V_{DDbgmin}$

$I_{VDD} = 5.05\,mA$

Curvature corrected bandgap circuit



$$I_{R1} = I_{R3} + I_{R4} = 2I_{R4}$$

$$= 2I_{R2} = 2\frac{V_{BE2} - V_{BE1}}{R_2}$$

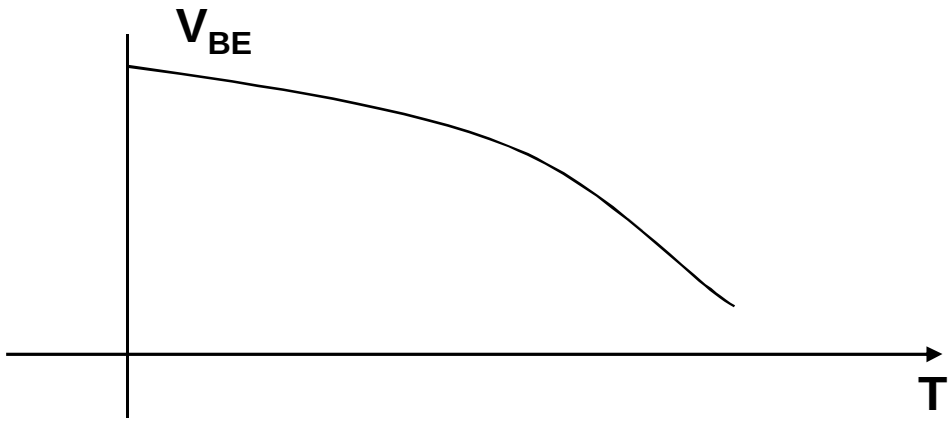
$$V_{REF} = V_{BE2} + V_{R1} = V_{BE2} + I_{R1} \cdot R_1$$

$$= V_{BE2} + \frac{2R_1}{R_2}(V_{BE2} - V_{BE1})$$

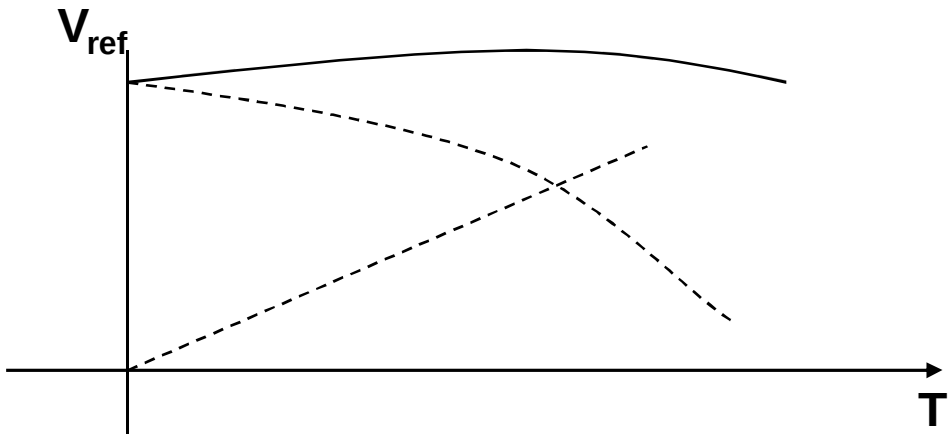
Problem :

$$\frac{\partial}{\partial T}\frac{2R_1}{R_2}\Delta V_{BE} \approx \text{const}, \quad \text{but } \frac{\partial V_{BE}}{\partial T} \neq \text{const}$$

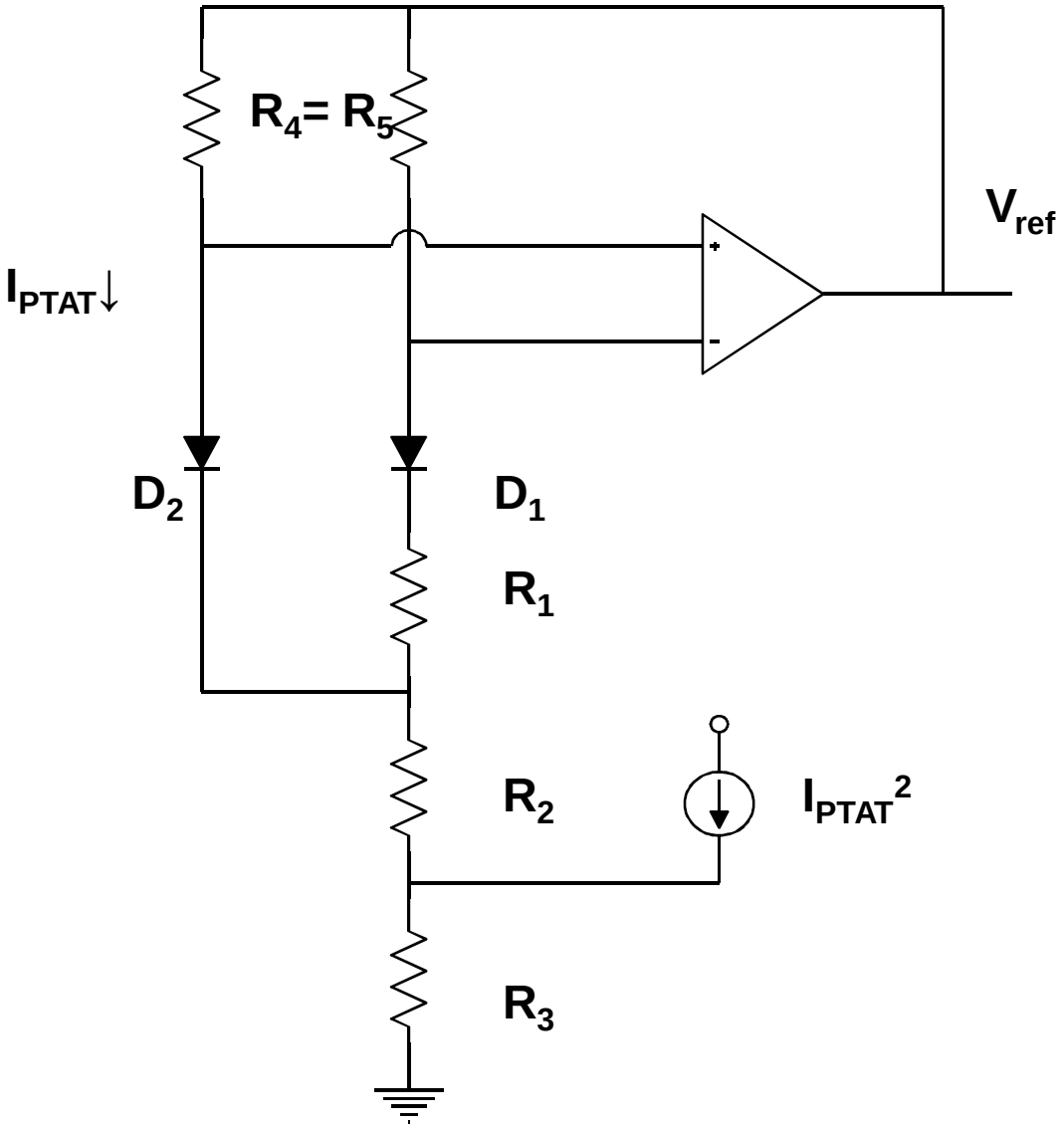
In fact :

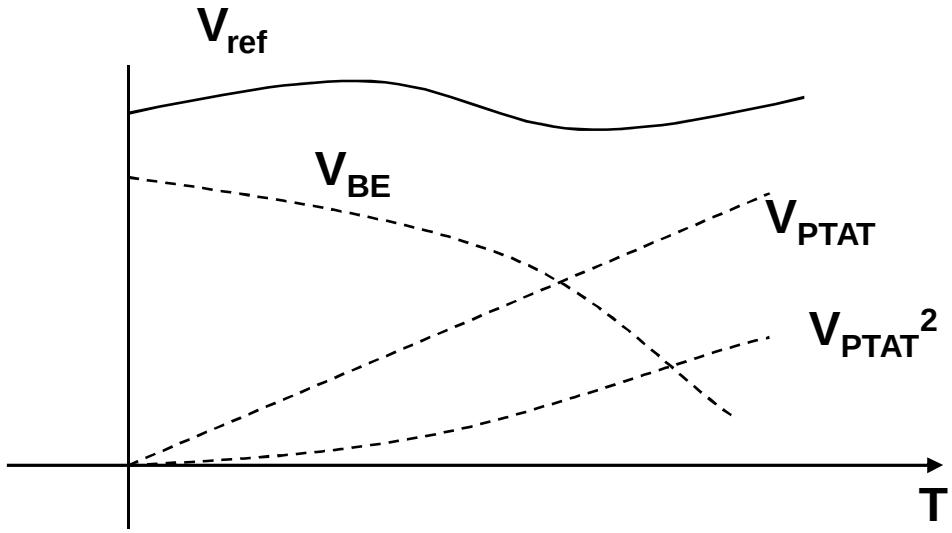


$\therefore$



Solution:





$$V_{ref} = V_{BE2} + 2I_{PTAT}\left(\frac{R_4}{2} + R_2 + R_3\right) + I_{PTAT}^2 \cdot R_3$$

$$I_{PTAT} = \frac{V_{BE2} - V_{BE1}}{R_1}$$

$$= \frac{1}{R_1}\frac{kT}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\right)$$

How to get I_{PTAT}^2 ?

Ex:

1. **Suppose you have an I_{PTAT}^2 source characterized by $I_{PTAT}^2 = \alpha T^2$, derive the conditions so that both first order and second order partial derivative of V_{ref} with respect to T are canceled at a given temperature T_0.**

2. **Suggest a circuit schematic that can be used to generated I_{PTAT}^2 current. You can use some of the circuit elements that we talked about earlier together with current mirrors/amplifiers to construct your circuit. Explain how your circuit work. If you found something in the literature, you can use/modify it but you should state so, give credit, and explain how the circuit works.**

Characterization of a Current-Mode Bandgap Circuit Structure for High-Precision Reference Applications

Hanqing Xing, Le Jin, Degang Chen and Randall Geiger

Iowa State University
05/22/2006

Outline

- Background on reference design
- Introduction to our approach
- Characterizing a multiple-segment reference circuit
- Structure of reference system and curve transfer algorithm
- Conclusion

Background on reference design(1)

- References are widely used in electronic systems.
- The thermal stability of the references plays a key role in the performance of many of these systems.
- Basic idea behind commonly used “bandgap” voltage references is combining PTAT and CTAT sources to yield an approximately zero temperature coefficient (TC).

Background on reference design(2)

- Linearly compensated bandgap references have a TC of about 20~50ppm/^{o}C over 100^{o}C. High order compensation can reduce TC to about 10~20ppm /^{o}C over 100^{o}C.
- Unfortunately the best references available from industry no longer meet the performance requirements of emerging systems.

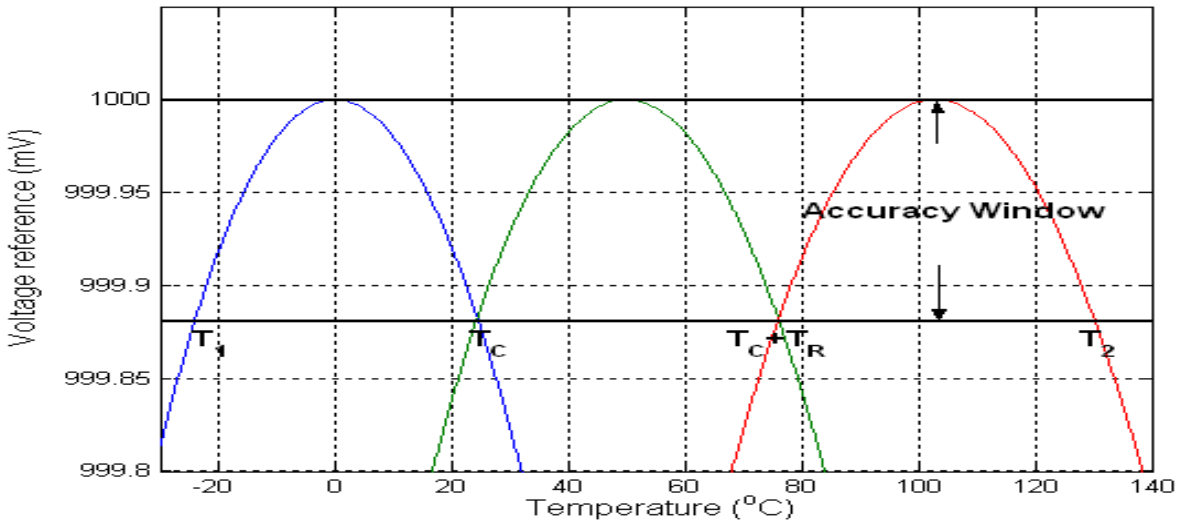
System Resolution	12 bits	14 bits	16 bits
TC requirement on reference	2.44ppm/^{o}C	0.61ppm/^{o}C	0.15ppm/^{o}C

Introduction to our approach(1)

- “Envirostabilized references”
  - The actual operating environment of the device is used to stabilize the reference subject to temperature change.
- Multiple-segment references
  - The basic bandgap circuit with linear compensation has a small TC near its inflection point but quite large TC at temperatures far from the inflection point.
  - High resolution can be achieved only if the device always operates near the inflection point.
  - Multiple reference segments with well distributed inflection points are used.

Introduction to our approach(2)

A three-segment voltage reference



# Curves	3	4	6	9
TC (ppm/°C)	0.8	0.4	0.2	0.1
Accuracy (Bits)	13	14	15	16

Temperature range: -25°C~125°C

Characterization of a bandgap circuit (1)

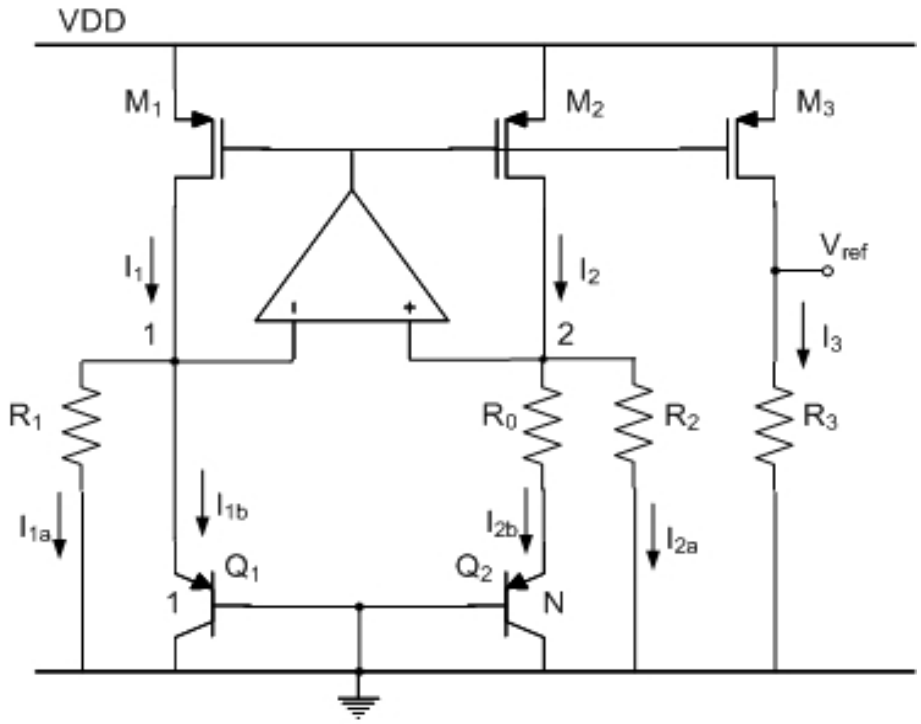
Well known relationship between emitter current and V_{BE}:

$$I_{1b} = \sigma A_1 T^r \exp\left(\frac{|V_{BE1}| - V_G}{kT/q}\right)$$

$$I_{2b} = \sigma A_2 T^r \exp\left(\frac{|V_{BE2}| - V_G}{kT/q}\right)$$

$$V_G = V_{G0} - \frac{\alpha T^2}{T + \beta}$$

For the silicon the values of the constants in (5) are, *α=7.021×10-4V/K*, *β=1108K* and $V_G(0)=1.17V$ [2].



Schematic of the current-mode bandgap circuit

Characterization of a bandgap circuit (2)

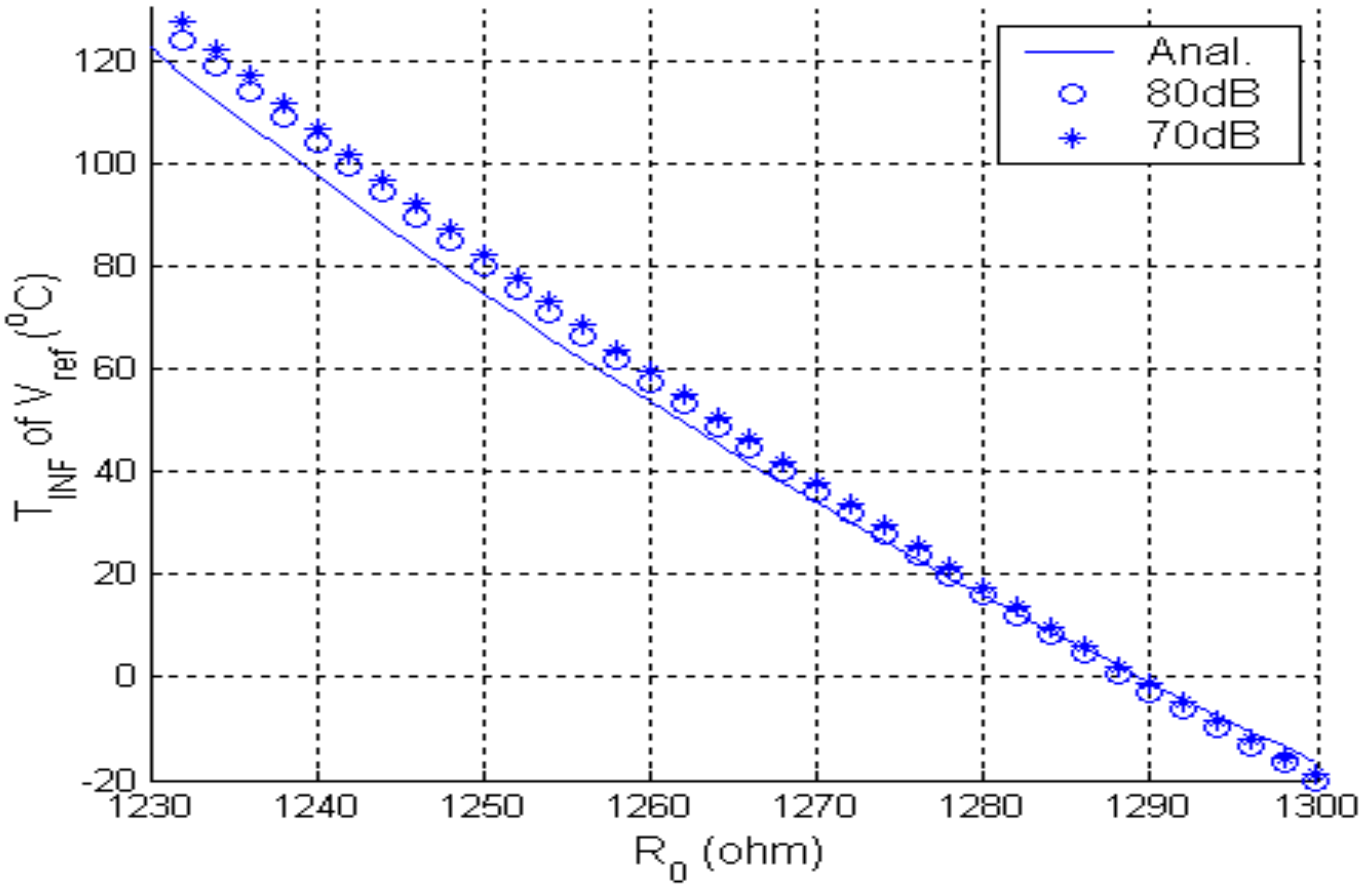
- The inflection point temperature
  - The temperature at the inflection point, T_{INF}, will make the following partial derivative equal to zero.

$$\frac{\partial I_1}{\partial T} = \frac{k}{qR_0}\ln\frac{A_2}{A_1} + \frac{k}{qR_1}\ln\left(\frac{k}{qR_0\sigma A_1 T^{r-1}}\ln\frac{A_2}{A_1}\right) - \frac{k(r-1)}{qR_1} - \frac{2\alpha T}{(T+\beta)R_1} + \frac{\alpha T^2}{(T+\beta)^2 R_1} = 0$$

  - It is difficult to get a closed form solution of T_{INF}. Newton-Raphson method can be applied to find the local maxima of I_1 and the corresponding T_{INF} *associated with different circuit parameters.*

Characterization of a bandgap circuit (3)

- The inflection point of V_{ref} as a function of R_0



Characterization of a bandgap circuit (4)

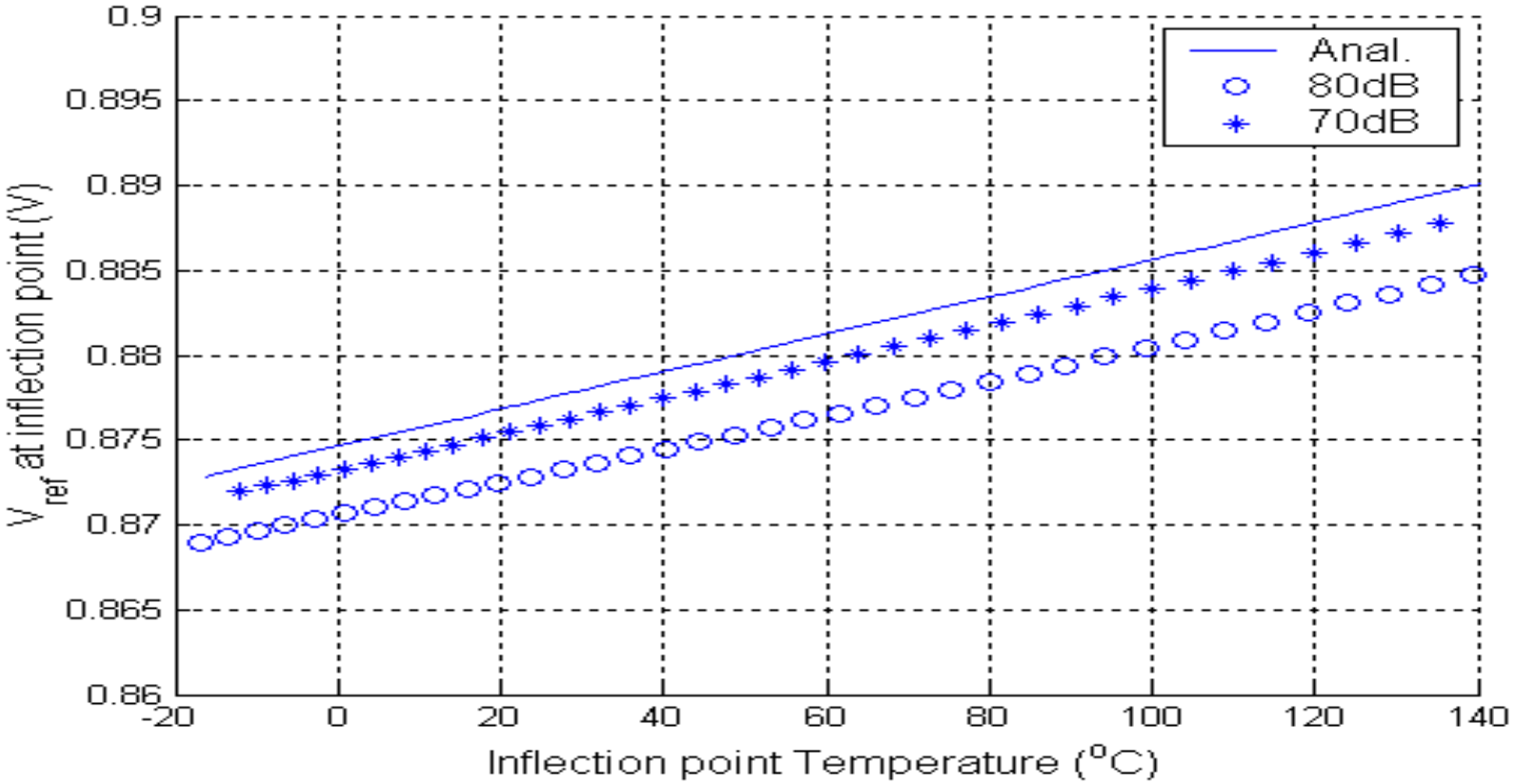
- Output voltage at the inflection point

$$V_{ref}(T_{INF}) = [\frac{kT_{INF}}{q}(r-1) + V_{G0} + \frac{\alpha T_{INF}^{\ 2}}{T_{INF}+\beta} - \frac{\alpha T_{INF}^{\ 3}}{(T_{INF}+\beta)^2}]\frac{R_3}{R_1}$$

- With a fixed resistance ratio R_3/R_1, output voltage at the inflection point changes with the inflection point temperature.
- Voltage level alignment is required.

Characterization of a bandgap circuit (5)

- The reference voltage changing with temperature



Characterization of a bandgap circuit (6)

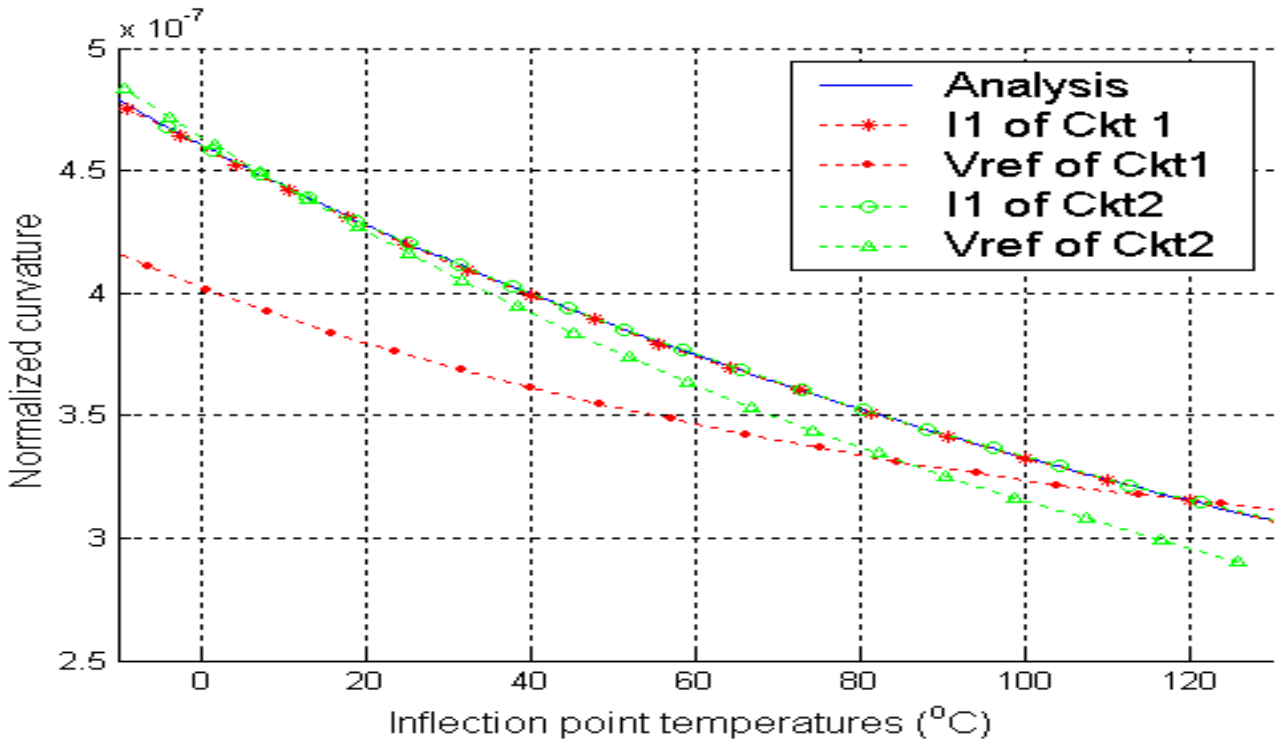
- Curvature of the linear compensated bandgap curve

$$C_{INF} = \frac{\dfrac{-k(r-1)}{qT_{INF}} - \dfrac{2\alpha\beta^{2}}{(T_{INF}+\beta)^{3}}}{\dfrac{kT_{INF}}{q}(r-1) + V_{G0} + \dfrac{\alpha T_{INF}^{2}}{T_{INF}+\beta} - \dfrac{\alpha T_{INF}^{3}}{(T_{INF}+\beta)^{2}}}$$

- There are only process parameters and temperature in the expression of the curvature.
- The curvature can be well estimated although different circuit parameters are used.

Characterization of a bandgap circuit (7)

- 2nd derivative of the bandgap curve at different inflection point temperatures (emitter currents of Ckt1 and Ckt2 are 20uA and 50uA respectively and opamp gain is 80dB)

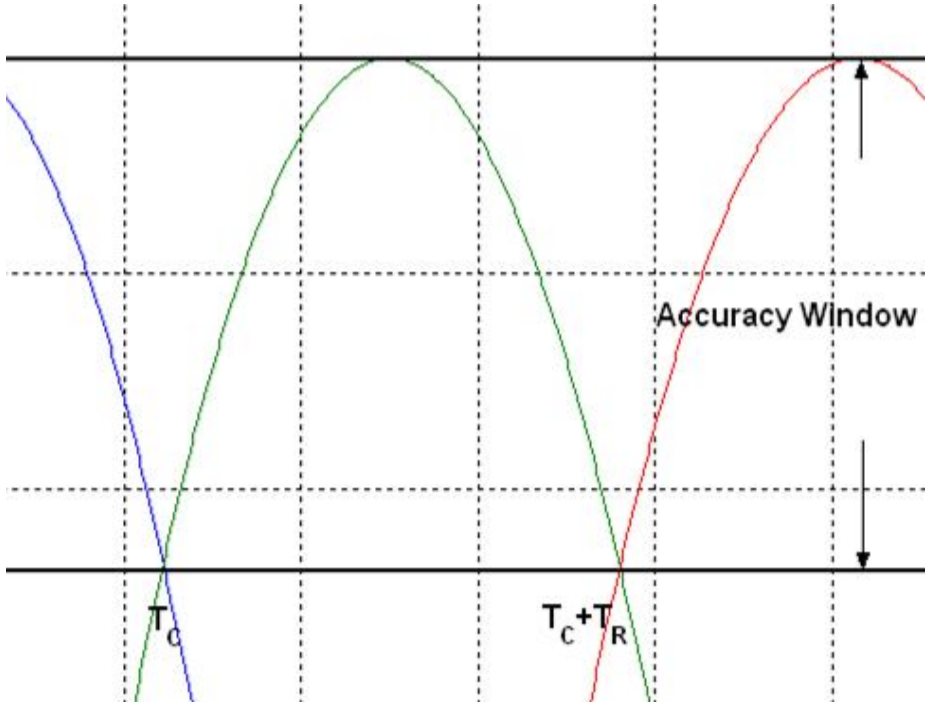


Structure of reference system and curve transfer algorithm (1)

- Three major factors that make the design of a multi-segment voltage reference challenging
  - the precise positioning of the inflection points
  - the issue of aligning each segment with desired reference level and accuracy
  - establishing a method for stepping from one segment to another at precisely the right temperature in a continuous way

Structure of reference system and curve transfer algorithm (2)

- the precise positioning of the inflection points
  - The inflection point can be easily moved by adjusting R_0
  - Equivalent to choosing a proper temperature range for each segment.
  - The same voltage level at two end points gives the correct reference curve.
  - With the information of the curvature, a proper choice of the temperature range makes sure the segment is within desired accuracy window.



Structure of reference system and curve transfer algorithm(3)

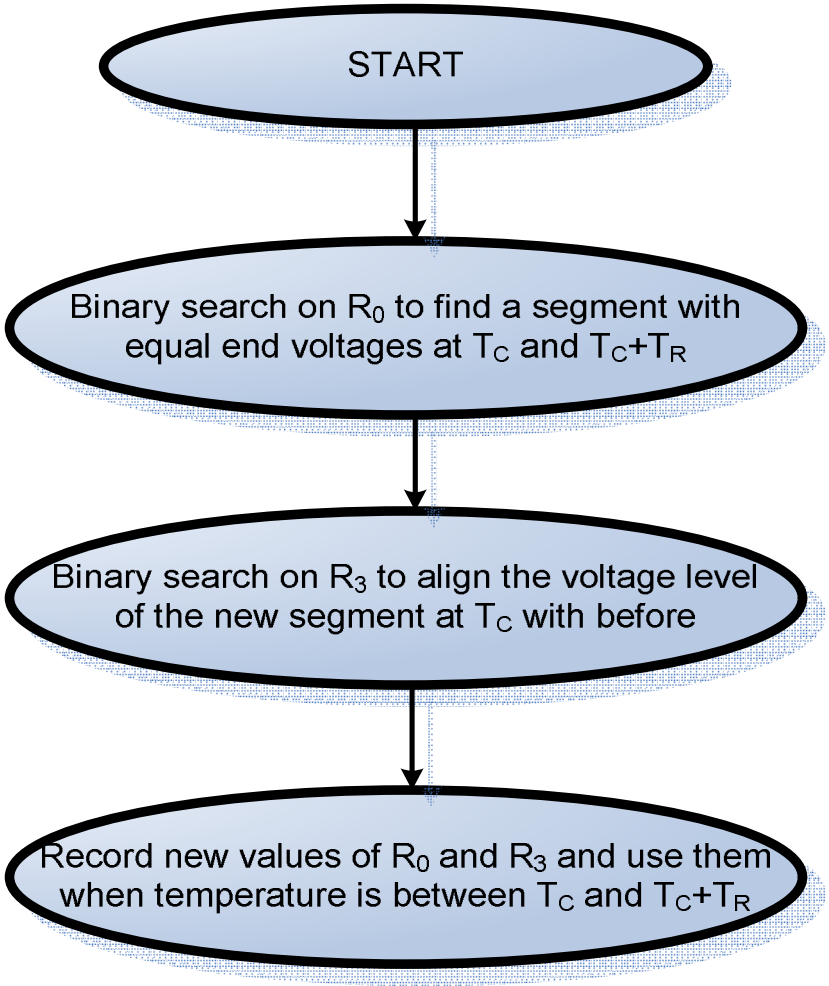
- aligning each segment with desired reference level and accuracy
  - The reference level can be easily adjusted by choosing different values of R_3, which will not affect the inflection point.
  - Comparison circuit with higher resolution is required to do the alignment.

Structure of reference system and curve transfer algorithm(4)

- Algorithm for stepping from one segment to another at precisely the right temperature in a continuous way
  - Determining the number of segments and the temperature range covered by each of them
  - Recording all the critical temperatures that are end points of the segments
  - Calibration done at those critical temperatures
  - Stepping algorithm

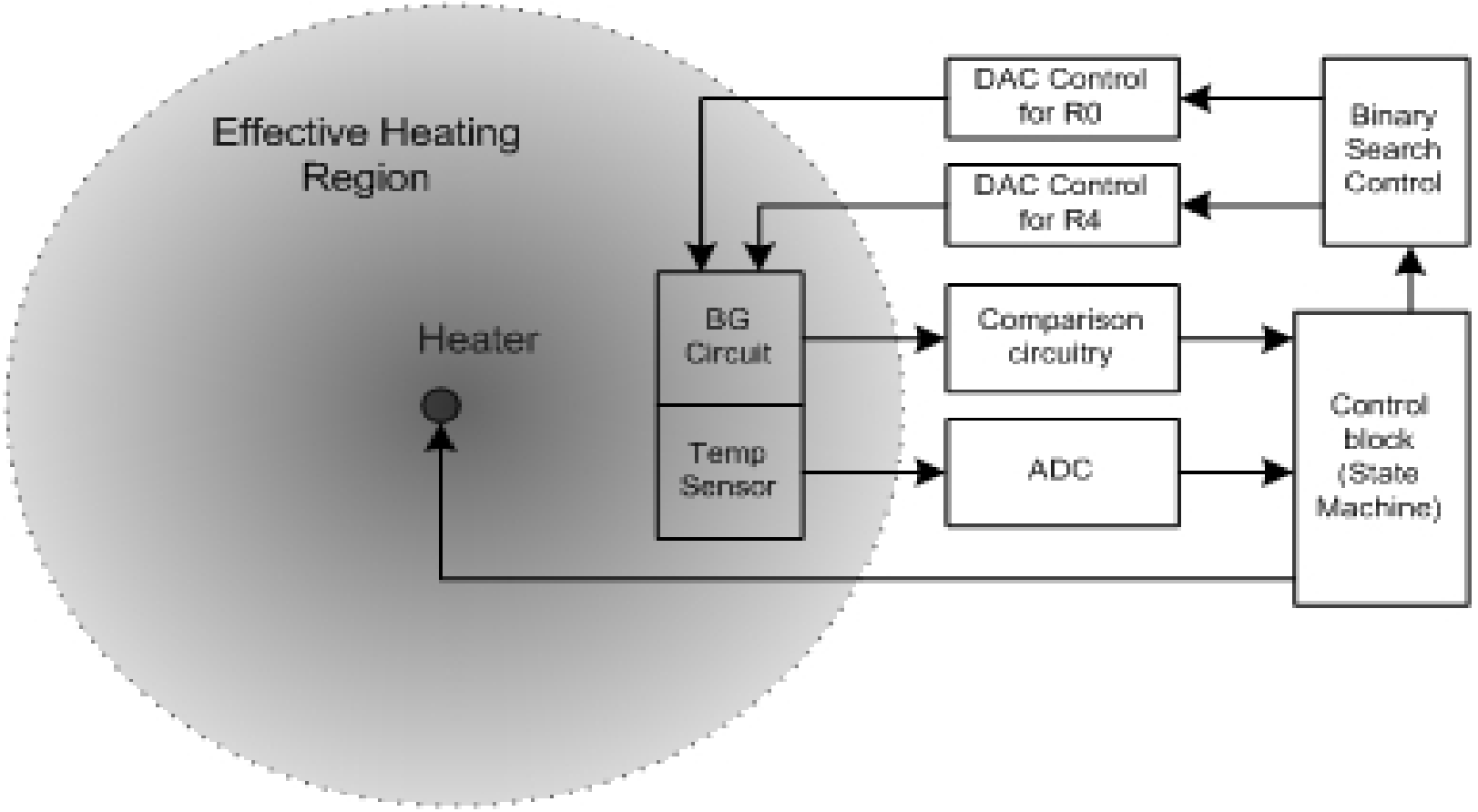
Structure of reference system and curve transfer algorithm(5)

- Stepping algorithm
  - When temperature rises to a critical temperature T_C at first time, find correct R_0 and R_3 values for the segment used for next T_R degrees
  - T_R is the temperature range covered by the new segment



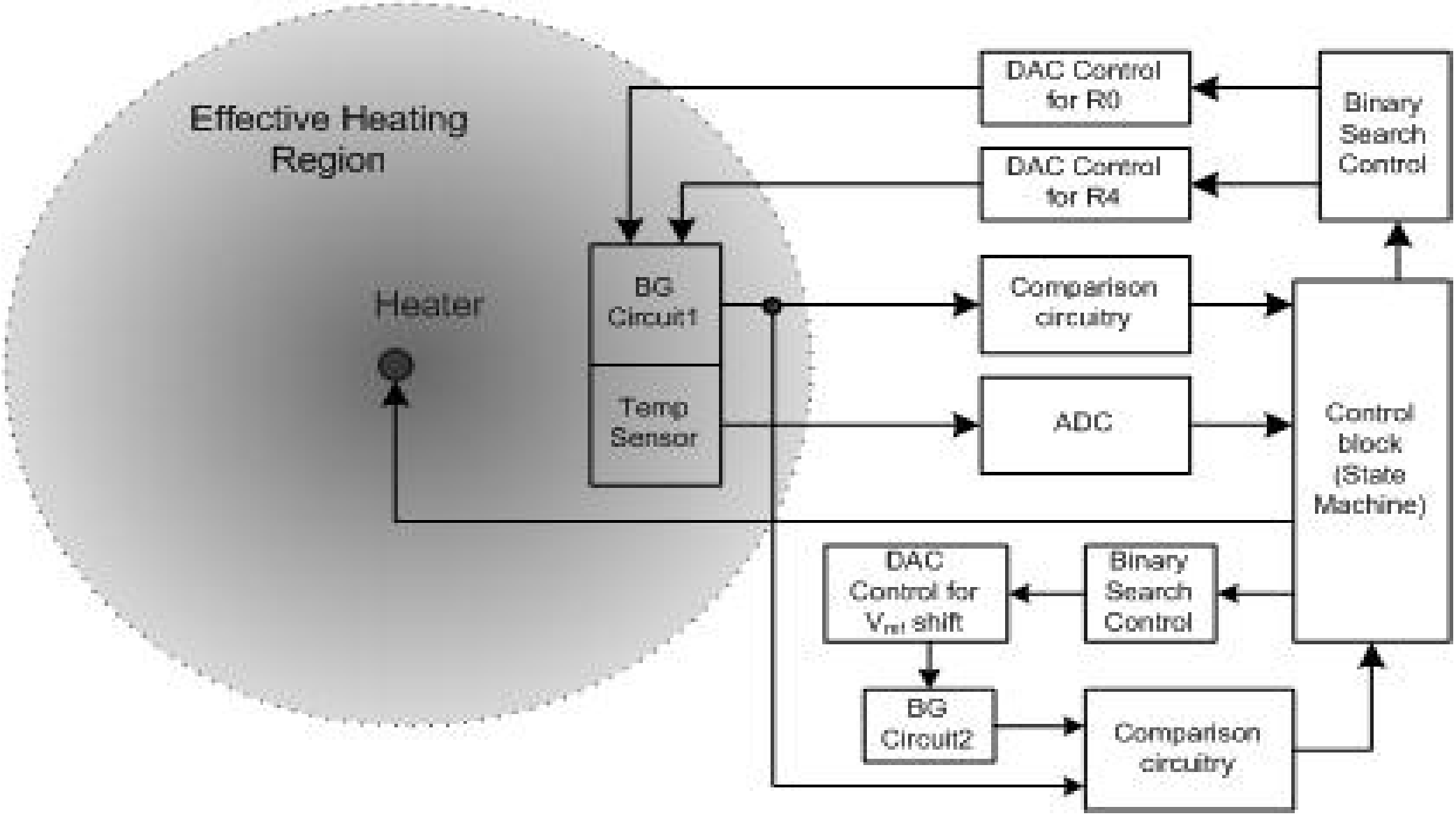
Structure of reference system and curve transfer algorithm(6)

- System diagram



Conclusion

- A new approach to design high resolution voltage reference
- Explicit characterization of bandgap references
- developed the system level architecture and algorithm


Effective Heating Region
Heater
BG Circuit1
Temp Sensor
DAC Control for R0
DAC Control for R4
Binary Search Control
Comparison circuitry
ADC
Control block (State Machine)
DAC Control for V_{ref} shift
Binary Search Control
BG Circuit2
Comparison circuitry

Heater: the dimension of the heater is quite small in comparison with that of the die. It is regarded as a point heat source. The shadow region is where the heater can effectively change the temperature of the die. BG Circuit and Temp Sensor are in the effective heating region.

BG Circuit 1: the whole bandgap circuit includes bandgap structure, current mirror and the amplifier. R0 and R4 are both DAC controlled.

BG Circuit 2: the backup BG reference circuit, the same structure as BG Circuit 1 but with only R4 DAC controlled.

Temp. Sensor: the temperature sensor, which can sense the temperature change instantaneously, is located close to the bandgap circuit and has the same distance to the heater as the bandgap circuit so that the temperature monitored represents the ambient temperature of the bandgap circuit. Need good temperature linearity.

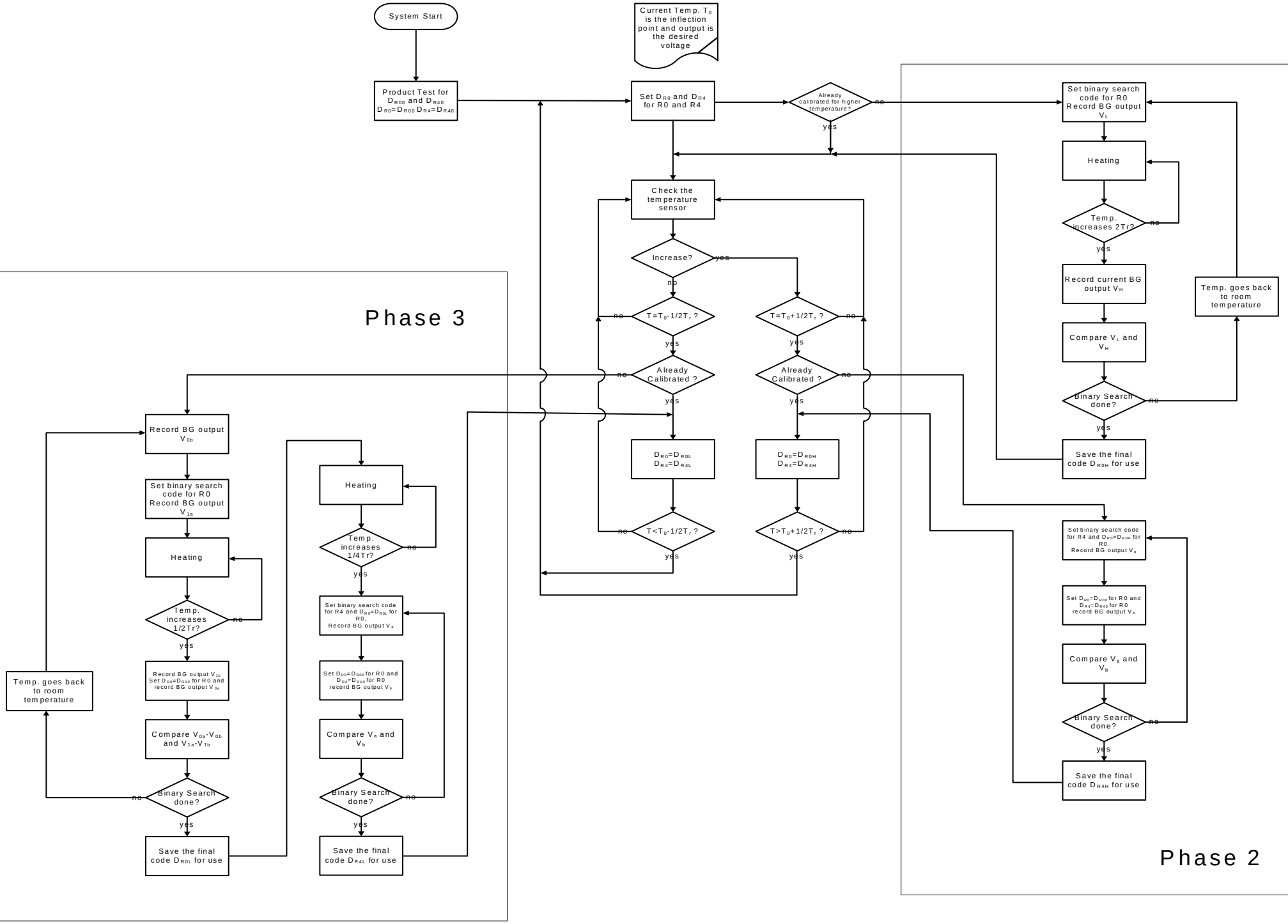
ADC: quantize analog outputs of the temperature sensor. Need 10-bit linearity.

Control Block: state machine is used as a controller, which receives the temperature sensing results and the comparison results and gives out control signals for binary search and heater.

DAC Control for R0 and R4: provide the digital controls for R0 and R4 in bandgap structure.

Binary Search: implement binary search for choosing right control signal for R0 and R4.

Comparison Circuitry: compare the outputs of the bandgap outputs. It is capable of making a comparison differentially or single-ended between the bandgap outputs at two differential moments and two different temperatures. The comparison circuitry should be offset cancelled and have small enough comparison resolution (much higher than 16-bit).


System Start
Product Test for D_{R00} and D_{R40}
$D_{R0}=D_{R00}$ $D_{R4}=D_{R40}$
Current Temp. T_0 is the inflection point and output is the desired voltage
Set D_{R0} and D_{R4} for R0 and R4
Already calibrated for higher temperature?
no
yes
Check the temperature sensor
Increase?
yes
no
$T=T_0-1/2T_r$?
$T=T_0+1/2T_r$?
Already Calibrated ?
Already Calibrated ?
$D_{R0}=D_{R0L}$ $D_{R4}=D_{R4L}$
$D_{R0}=D_{R0H}$ $D_{R4}=D_{R4H}$
$T<T_0-1/2T_r$?
$T>T_0+1/2T_r$?
Phase 3
Record BG output V_{0b}
Set binary search code for R0 Record BG output V_{1a}
Heating
Temp. increases 1/2Tr?
Record BG output V_{1b} Set $D_{R0}=D_{R00}$ for R0 and record BG output V_{0a}
Compare V_{0a}-V_{0b} and V_{1a}-V_{1b}
Binary Search done?
Temp. goes back to room temperature
Save the final code D_{R0L} for use
Heating
Temp. increases 1/4Tr?
Set binary search code for R4 and $D_{R0}=D_{R0L}$ for R0. Record BG output V_a
Set $D_{R0}=D_{R00}$ for R0 and $D_{R4}=D_{R40}$ for R0 record BG output V_b
Compare V_a and V_b
Binary Search done?
Save the final code D_{R4L} for use
Set binary search code for R0 Record BG output V_L
Heating
Temp. increases 2Tr?
Record current BG output V_H
Compare V_L and V_H
Binary Search done?
Temp. goes back to room temperature
Save the final code D_{R0H} for use
Set binary search code for R4 and $D_{R0}=D_{R0H}$ for R0. Record BG output V_a
Set $D_{R0}=D_{R00}$ for R0 and $D_{R4}=D_{R40}$ for R0 record BG output V_b
Compare V_a and V_b
Binary Search done?
Save the final code D_{R4H} for use
Phase 2

Curve transfer algorithm

Prerequisites:

- Calibrate the temperature sensor. The sensor needs to have good linearity. That means the outputs of the sensor is linear enough with the temperature. The ADC also needs good linearity for accurately indicating the temperature, 10-bit linearity for 0.1 degree C accuracy.
- Get the basic characteristics of the bandgap curve, such as the temperature range covered by one curve under the desired accuracy requirement, and the number of curves needed. Assume the temperature range covered by one curve under 16-bit accuracy is T_r, and with T_r degrees' temperature change the output of the sensor changes S_r.

Procedure:

- **Phase 1:** Production test, which gives correct DAC codes D_{R00} and D_{R40} for R0's and R4's controls to achieve a bandgap curve with its inflection point at current room temperature T_0 and its output voltage right now equal to the desired reference voltage V_0.

- **Phase 2:** At the temperature T_0, do the following to obtain R0 and R4 control codes of the next bandgap curve with higher inflection points D_{R0H} and D_{R4H}:
  - **Step 1:** Record the current output of the temperature sensor, as S_0, then reset the control code for R0 (keep the code for R4) to the first code in binary search, the output of the bandgap circuit is V_L.
  - **Step 2:** Activate the heater and monitor the output of the sensor, stop the heater when the output arrives $S_1=S_0+2S_r$ (or a litter bit smaller), the current output of the bandgap circuit is V_H with the R0 code unchanged.
  - **Step 3:** Compare V_L and V_H with the comparison circuitry, continue the binary search for R0 and set the new binary code according to the result of comparison. Wait until the output of the sensor back to S_0, then record the output code for the new code.
  - **Step 4:** Repeat the three steps above until the binary search for R0 is done. The final code for R0 can generate a new bandgap curve with its inflection at T_0+T_r. Store the new R0 control code for future use, denoted as D_{R0H}.

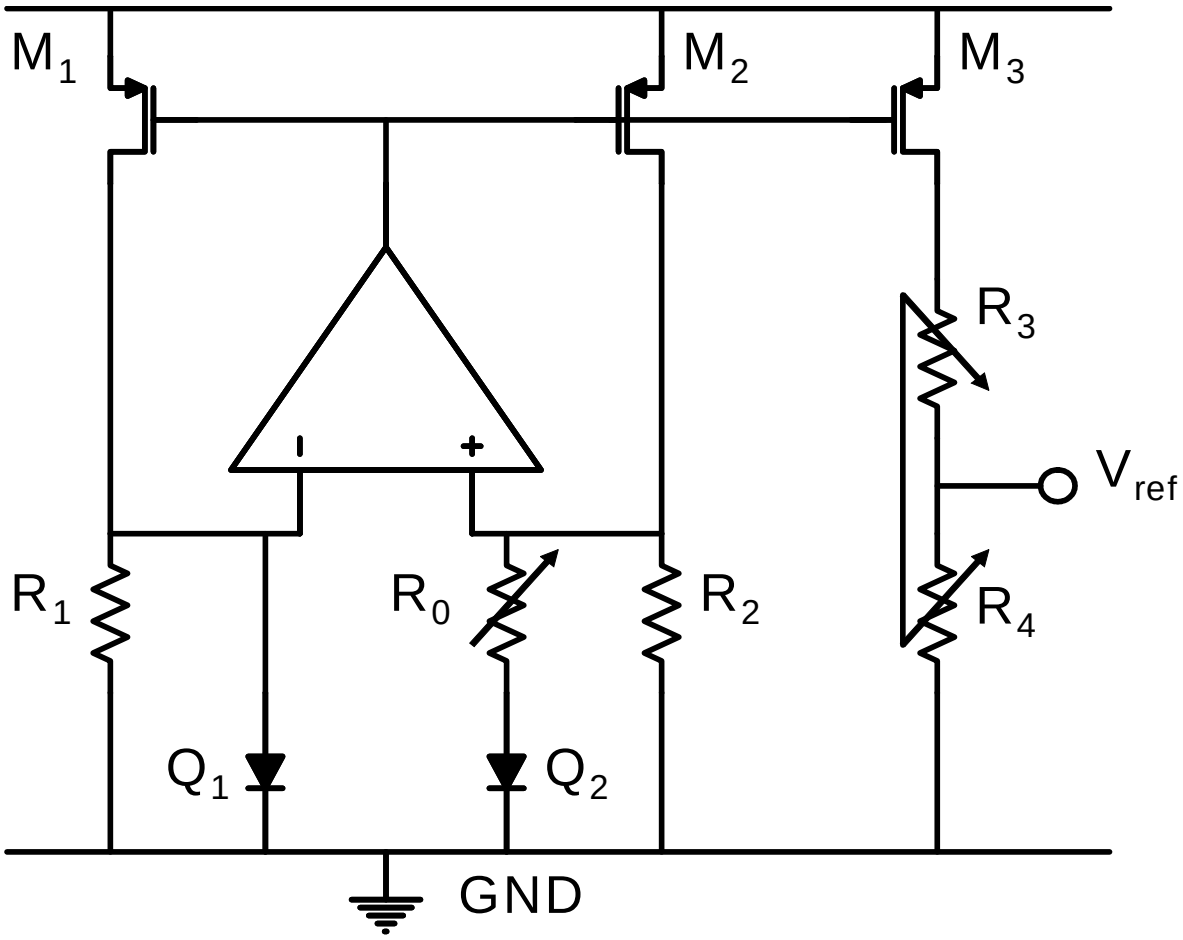
- **Step 5:** Monitor the ambient temperature change using the temperature sensor. When the output of the sensor rises to $S_0+1/2S_r$, start comparing the two bandgap outputs with R0 control code equal to D_{R00} and D_{R0H} respectively. Another binary search is applied to obtain the new R4 control code D_{R4H}, which ensure the two outputs in comparison are very close to each other.
- **Step 6:** Monitor the output of the sensor, when it goes higher than $S_0+1/2S_r$, the new codes for R0 and R4 are used and the curve transfer is finished. Keep monitoring the temperature change, when the output of the sensor goes to S_0+S_r (that means the current temperature is right at the inflection of the current curve), all the operations in the phase 2 can be repeated to get the next pare of codes for higher temperature.

- **Phase 3:** When the ambient temperature goes lower, heater algorithm does not work effectively. Another procedure is developed to transfer to the lower inflection point curves. Temperature lower than room temperature cannot be achieved intentionally. Therefore we can not predict control codes for the ideal next lower curve as what we do in higher temperature case. When the temperature goes to T_0-1/2T_r, in order to maintain the accuracy requirement we have to find another bandgap curve with inflection point lower than T_0, the best we can achieve is the curve with its inflection point right at T_0-1/2T_r. Thus for temperature range lower than initial room temperature T_0, we need curves with doubled density of curves in the higher temperature range.
  - **Step 1:** At the initial time with room temperature T_0, record the bandgap output voltage V_{0a} and the current control code for R0 D_{R00}. Monitor the temperature, when it goes to S_0-1/2S_r, note the bandgap output V_{0b} and then reset the control code for R0 to the first code of binary search, D_{BS0}. Record the bandgap output V_{1a}.

- **Step 2:** Start heating. When the output of the sensor is back to S_0 record the bandgap output V_{1b}.
- **Step 3:** Do differential comparison between V_{0a}-V_{0b} and V_{1a}-V_{1b}.
- **Step 4:** Wait for the sensor output back to S_0-1/2S_r, change the R0 control code according to the comparison result. Record the bandgap output as V_{3a}.
- **Step 5:** Repeat step 2 to 4 until the binary search is done. The final control code for R0 D_{R0L} ensures the difference between V_{0a}-V_{0b} and V_{1a}-V_{1b} is very small and the inflection of the new bandgap curve is close to T_0-1/2T_r. Set R0 control code as D_{R0L}.
- **Step 6:** Activate the heater until the output of the sensor is S_0-1/4S_r and keep this temperature. Initial the binary search for R4. Compare the bandgap outputs of two curves with R0 control codes D_{R00} and D_{R0L} respectively. Set the R4 control code according to comparison results. The final code D_{R4L} is the new control code for R4, which ensures the two voltage in comparison are nearly equal.
- **Step 7:** Set D_{R0L} and D_{R4L} for R0 and R4 to finish the curve transfer. Keep monitoring the temperature change, when the output of the sensor goes to S_0-S_r (that means a new curve transfer needs to start), all the operations in the phase 3 can be repeated to get the next pare of codes for higher temperature.

- **Phase 4:** Monitor the output of the temperature sensor. If a calibrated curve transfer is needed, set the new control codes for R0 and R4 according to the former calibration results. If a new calibration is needed, Phase 2 (temperature goes higher) or Phase 3 (temperature goes lower) is executed to obtain the new control codes.

Proposed Circuit



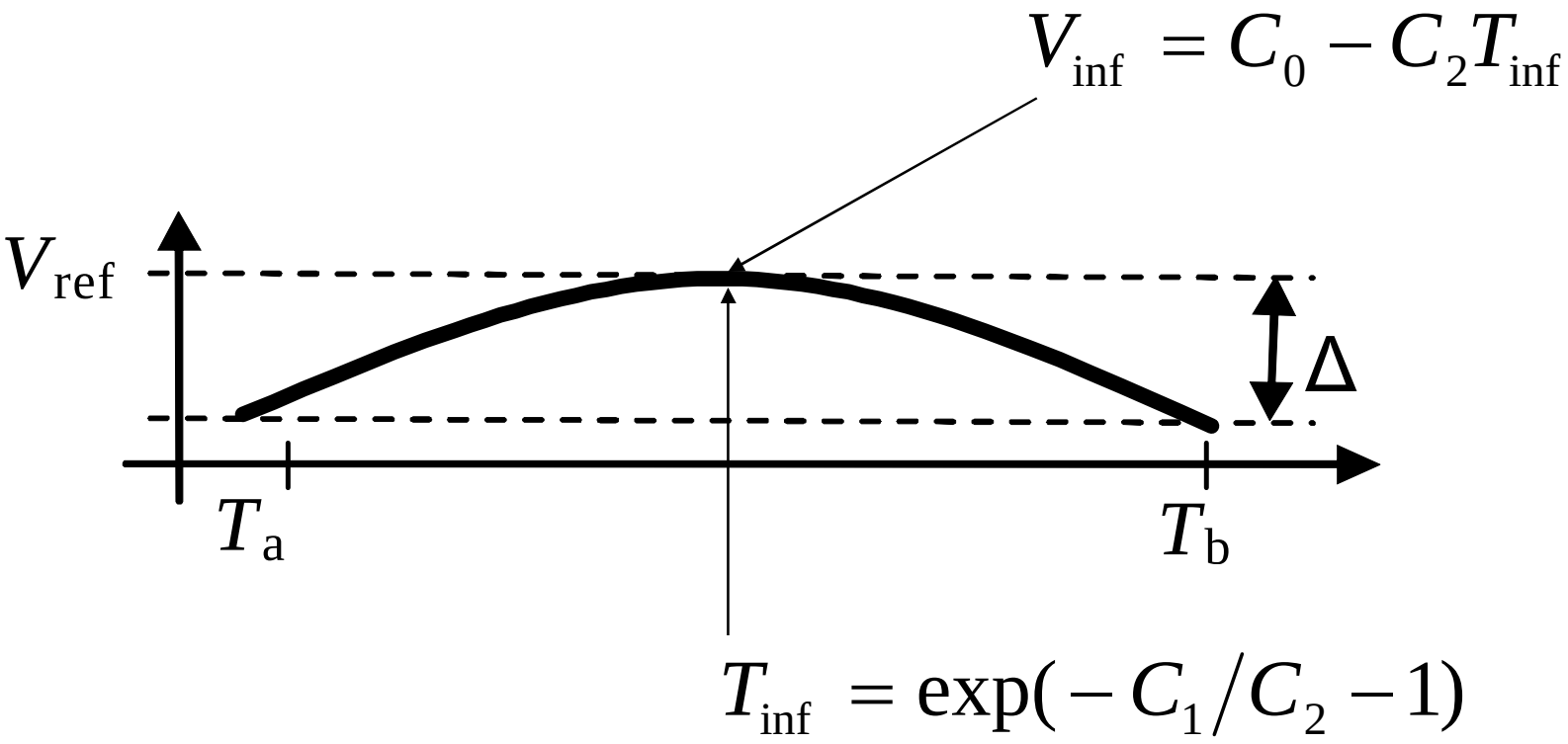
$$V_{ref}(T) = C_0 + C_1 T + C_2 T \ln(T)$$

$$C_0 = \frac{R_4}{R_1} V_G$$

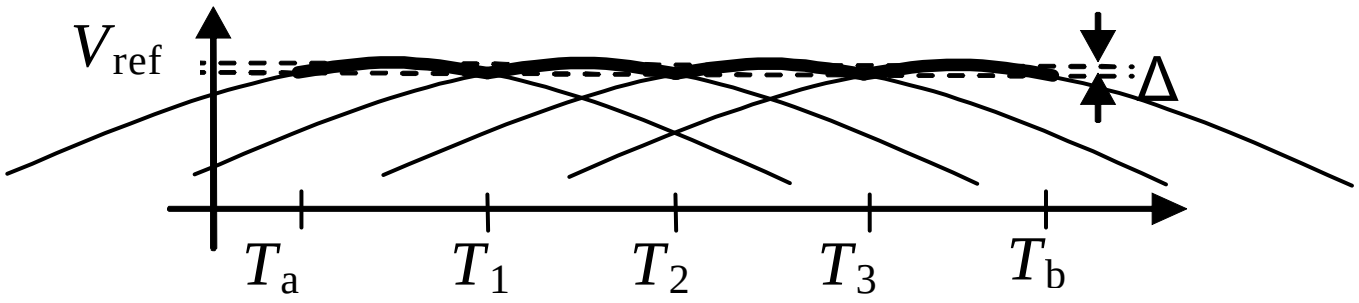
$$C_1 = \frac{kR_4}{q}\left[\frac{1}{R_0}\ln\frac{A_2}{A_1} + \frac{1}{R_1}\ln\left(\frac{k\ln(A_2/A_1)}{qR_0\sigma A_1}\right)\right]$$

$$C_2 = -(r-1)\frac{R_4}{R_1}\frac{k}{q}$$

Multi-Segment Bandgap Circuit

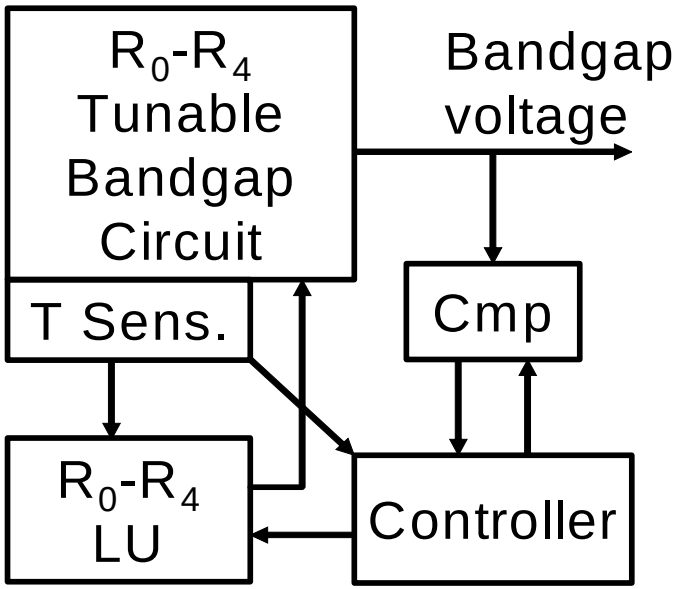


Multi-Segment Bandgap Circuit



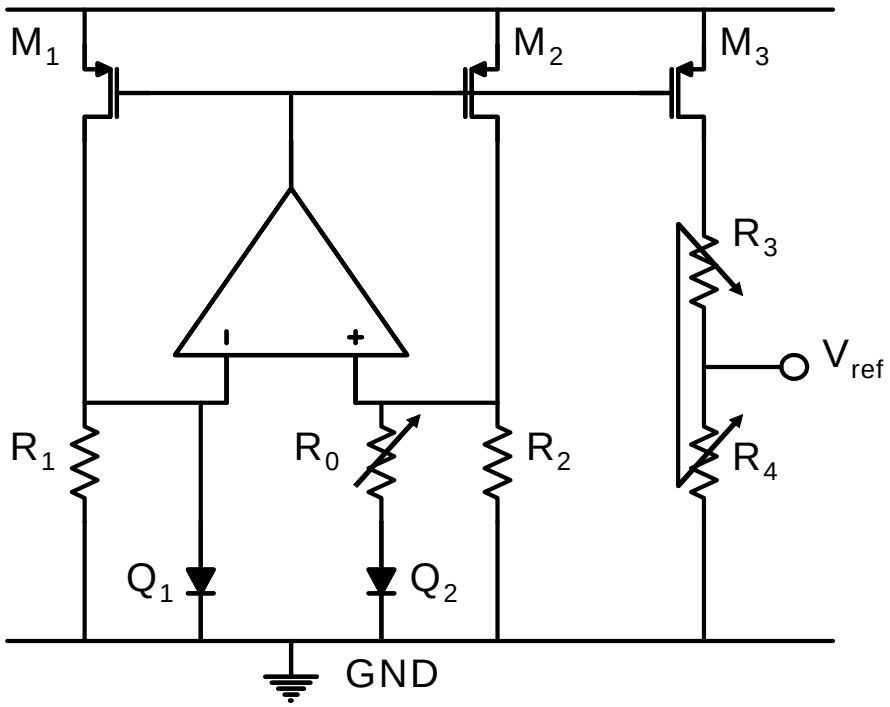
- Observations
  - T_{inf} is a function of R_0
  - V_{inf} can be determined by R_4

Self-Calibration of Bandgap Circuit



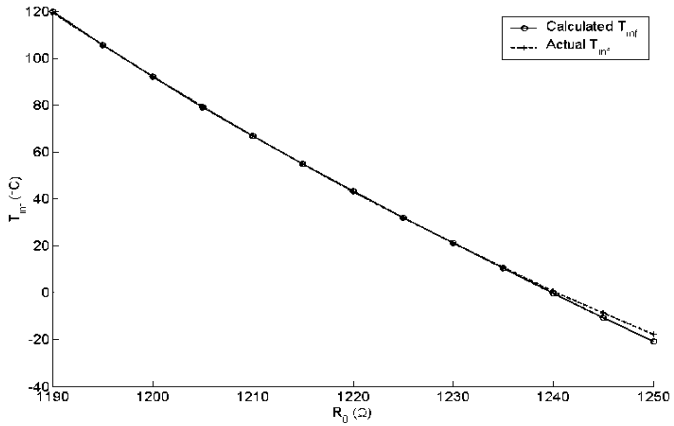
- Partition whole temperature range into small segments
- Identify C_0, C_1 and C_2 as functions of R_0 through measurements
- Use R_0 to set appropriate T_{inf} for each segment
- Change R_4 to set the value of V_{inf}
- Performance guaranteed by calibration after fabrication and packaging

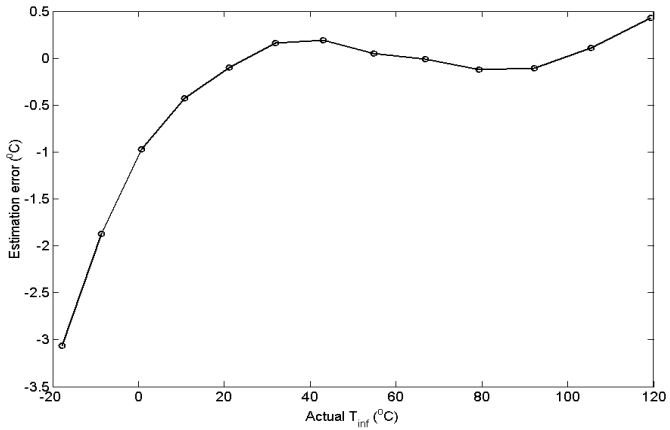
Simulation Setup



- TSMC 0.35 μm process
- Cascoded current mirrors with W/L = 30 μm /0.4 μm
- Diode junction area
  - $A_1 = 10\ \mu m^2$
  - $A_2 = 80\ \mu m^2$
- $R_1 = R_2 = 6\ K\Omega$
- $R_3 + R_4 = 6\ K\Omega$
- 2.5 V supply
- Op amp in Veriloga with 70 dB DC gain

T_{inf}-R_0 Relationship





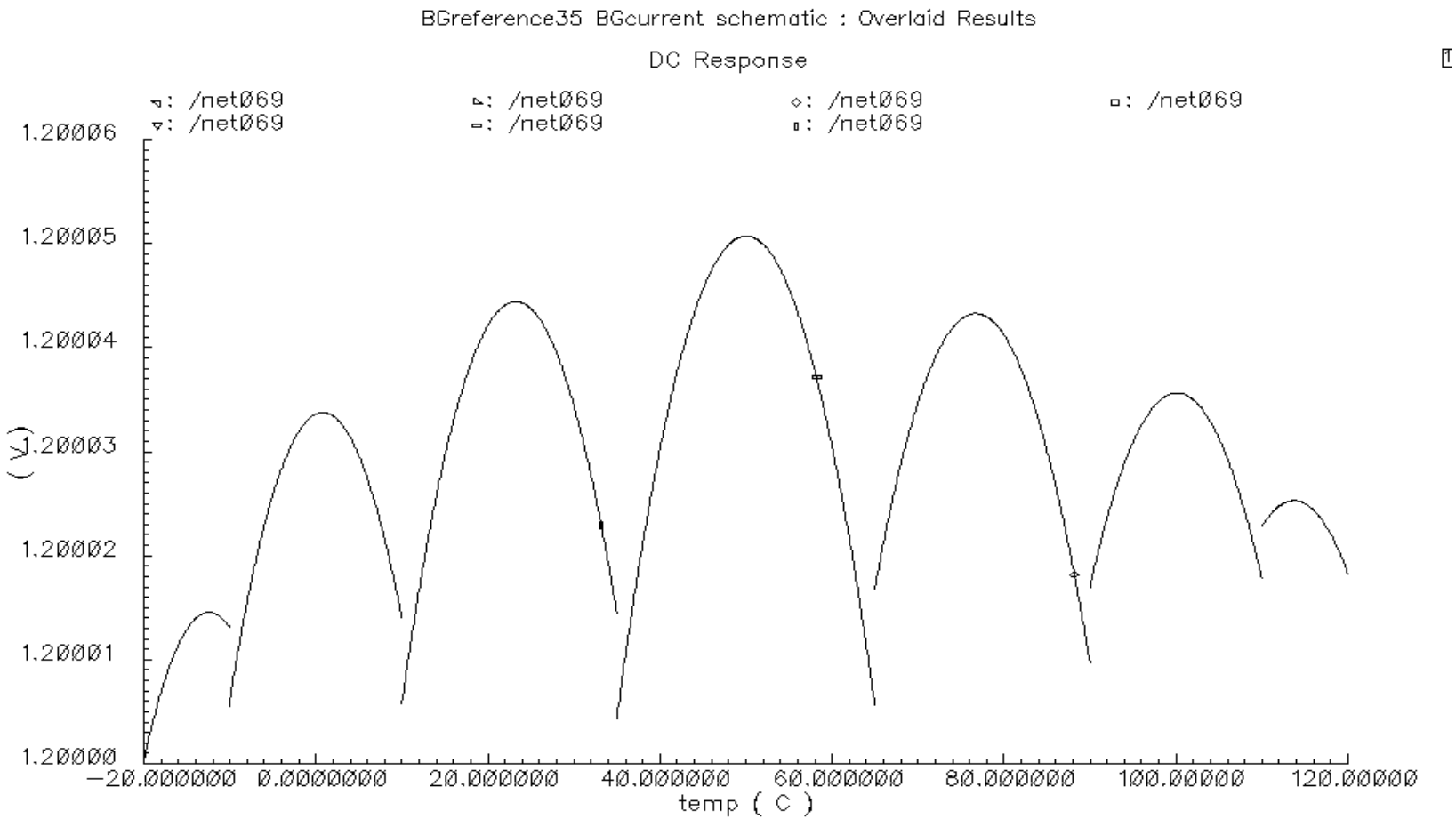
- V_{ref} measurement
  - R_0 ranging from 1150 to 1250 Ω with 1 W
  - T = 20, 22, and 24 °C
  - Measured voltage has accuracy of 1 μV
- Top left: Actual and estimated T_{inf} as a function of R_0
- Bottom left: Error in estimation

T_{inf}-R_0 Relationship

TABLE I. INFLECTION POINT PLACEMENT

T_{inf_des} (°C)	-15	0	22.5	50	77.5	100	115
R_0 (Ω)	1247	1240	1229	1217	1206	1197	1192
T_{inf_act} (°C)	-12.3	0.8	23.3	50.1	76.8	100.2	113.8

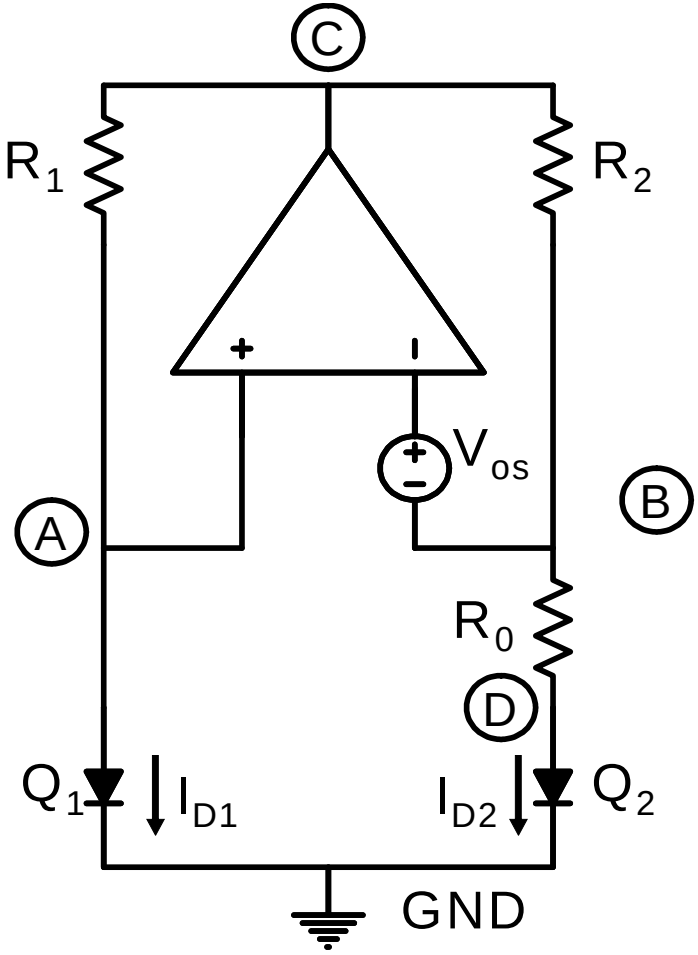
Multi-Segment Bandgap Curve



60-μV variation over 140 °C range gives 0.36 ppm/°C

Analysis of the Bandgap Reference Circuit

Schematic and Nodal Equations

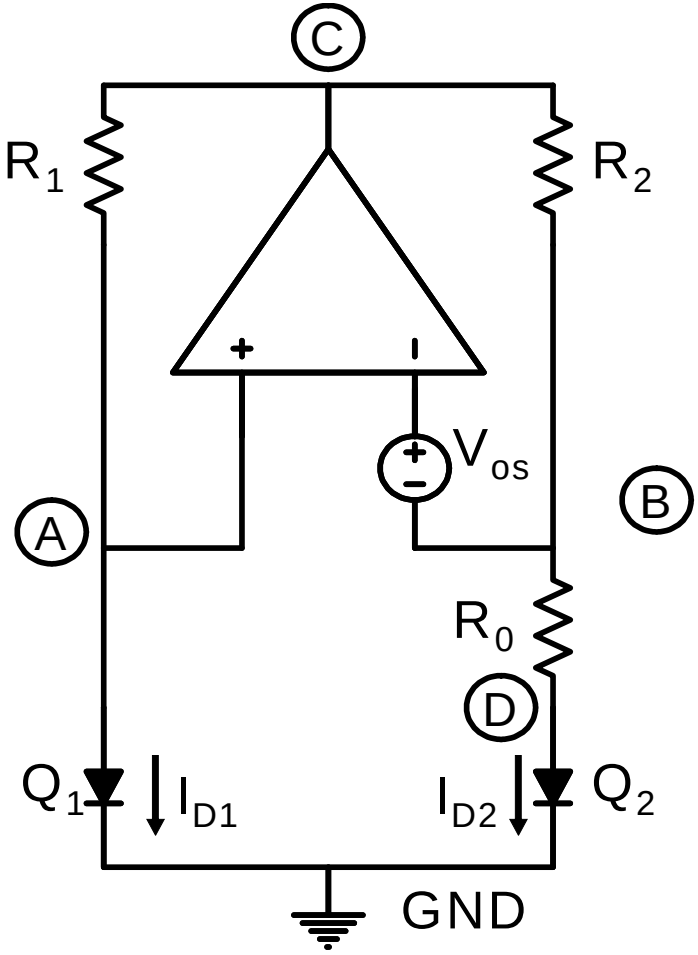


Analytical solution w/o A and Vos

```
eq1='(VA-VC)/R1+ID1=0';
eq2='(VB-VC)/R2+ID2=0';
eq3='VA-VB=0';
eq4='ID2=(VB-VD)/R0';
eq5='ID1=Isx1*exp((VA-VG)/Vt)';
eq6='ID2=Isx2*exp((VD-VG)/Vt)';
S=solve(eq1, eq2, eq3, eq4, eq5, eq6,
    'VA,VB,VC,VD,ID1,ID2');
```

```
VC=
VG
+log(log(Isx2*R2/Isx1/R1)*Vt*R2/R0/Isx1/R1)*Vt
-R2*log(Isx1*R1/Isx2/R2)*Vt/R0
```

Schematic and Nodal Equations

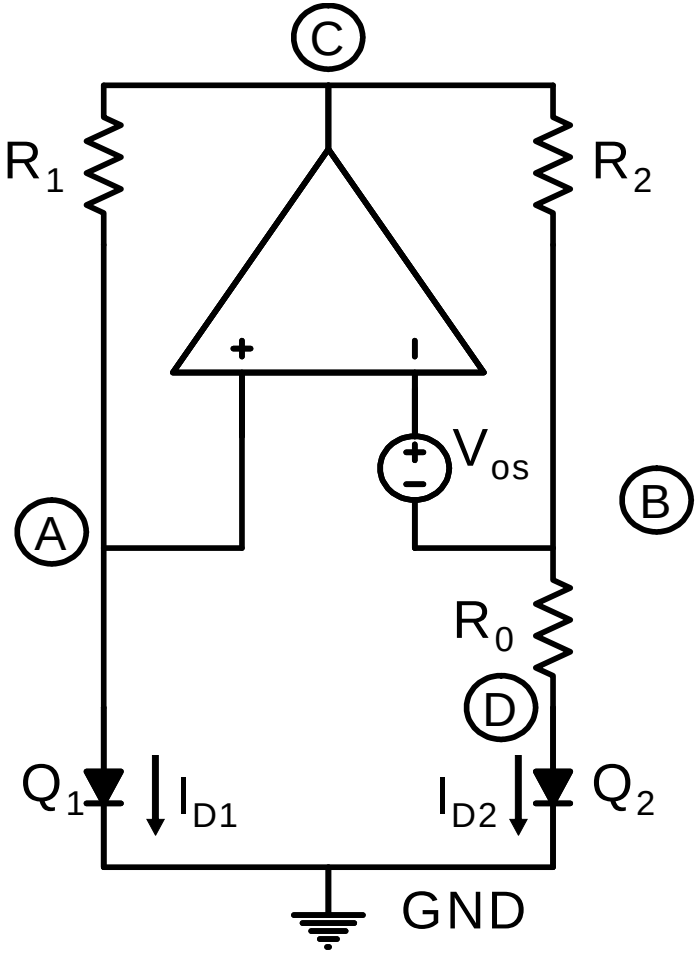


Derivative wrpt Vos: VA-VB=Vos

```
eq1='(pVA-pVC)/R1+pID1=0';
eq2='(pVB-pVC)/R2+pID2=0';
eq3='pVA-pVB=1';
eq4='pID2=(pVB-pVD)/R0';
eq5='pID1=ID1*pVA/Vt';
eq6='pID2=ID2*pVD/Vt';
SpVos=solve(eq1, eq2, eq3, eq4, eq5, eq6,
    'pVA,pVB,pVC,pVD,pID1,pID2');
```

```
pVCpVos=
-(Vt+ID1*R1)*(ID2*R0+Vt+ID2*R2)
/(-Vt*R2*ID2+ID1*R0*R1*ID2+ID1*Vt*R1)
```

Schematic and Nodal Equations

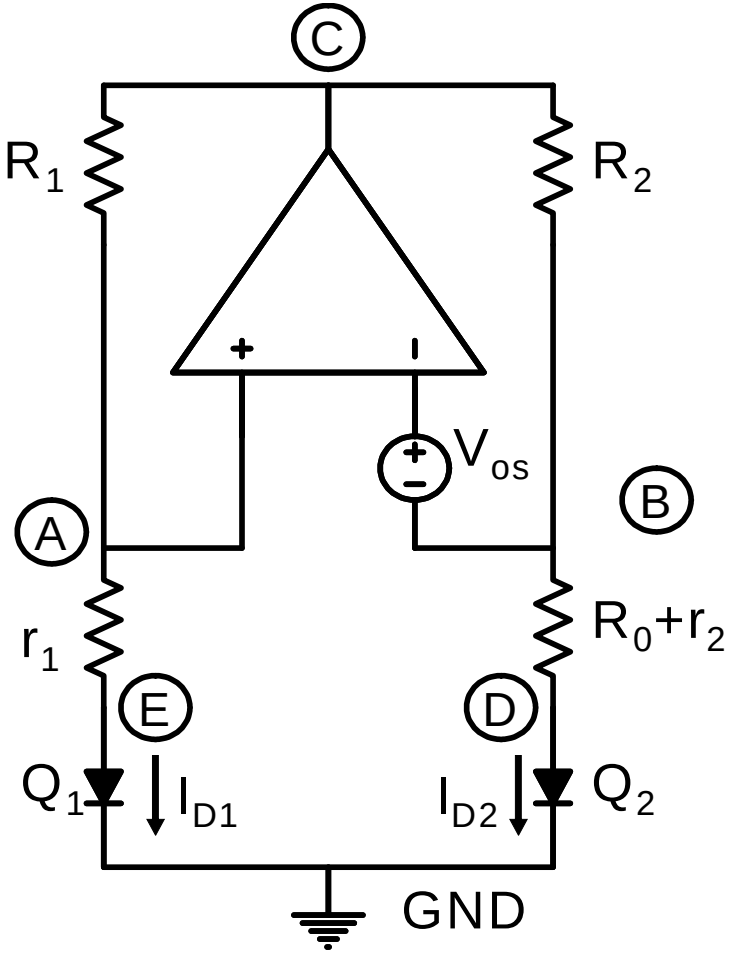


Derivative wrpt to 1/A: VC*(1/A)=VA-VB

```
eq1='(pVA-pVC)/R1+pID1=0';
eq2='(pVB-pVC)/R2+pID2=0';
eq3='VC+pVC/A=pVA-pVB';
eq4='pID2=(pVB-pVD)/R0';
eq5='pID1=ID1*pVA/Vt';
eq6='pID2=ID2*pVD/Vt';
SpA=solve(eq1, eq2, eq3, eq4, eq5, eq6,
    'pVA,pVB,pVC,pVD,pID1,pID2');
```

```
pVCpA=
-VC*A*(Vt^2+Vt*ID2*R0+Vt*R2*ID2
+ID1*Vt*R1+ID1*R0*R1*ID2+ID1*R1*ID2*R2)
/(Vt^2+Vt*ID2*R0-Vt*ID2*A*R2+Vt*R2*ID2
+ID1*A*R1*Vt+ID1*A*R1*ID2*R0
+ID1*Vt*R1+ID1*R0*R1*ID2+ID1*R1*ID2*R2)
```

Schematic and Nodal Equations



pVCpr1 =
ID1^2*R1*(ID2*R0+Vt+ID2*R2)
/(ID1*Vt*R1+ID1*R0*R1*ID2-
R2*Vt*ID2)

pVCpr2 =
-ID2^2*R2*(Vt+ID1*R1)
/(-
R2*Vt*ID2+ID1*Vt*R1+ID1*R0*R1
*ID2);

Bandgap Reference Voltage

VC=

VG+log(log(Ar*R2/R1)*Vt*R2/R0/Isx1/R1)*Vt

+R2*log(Ar*R2/R1)*Vt/R0

+pVCpVos*Vos+pVCpA*(1/A)

+pVCpr1*r1+pVCpr2*r2

Approximation

- pVCpVos = -(Vt+ID1*R1)*(ID2*R0+Vt+ID2*R2)/(ID1*R0*R1*ID2)
- pVCpA = VC*pVCpVos = -VC*(Vt+ID1*R1)*(ID2*R0+Vt+ID2*R2)/(ID1*R1*ID2*R0)
- pVCpr1 = ID1^2*R1*(ID2*R0+Vt+ID2*R2)/(ID1*R0*R1*ID2)
- pVCpr2 = -ID2^2*R2*(Vt+ID1*R1)/(ID1*R0*R1*ID2)

Simplification

- pVCpVos ~= -(1+log(Ar*R2/R1)*R2/R0)*(1+log(Ar*R2/R1)+log(Ar*R2/R1)*R2 /R0) /(log(Ar*R2/R1)^2*R2/R0)
- pVCpA ~= -VC *(1+log(Ar*R2/R1)*R2/R0)*(1+log(Ar*R2/R1)+log(Ar*R2/R1)*R2 /R0) /(log(Ar*R2/R1)^2*R2/R0)
- pVCpr1 ~= Vt*(1+log(Ar*R2/R1)+log(Ar*R2/R1)*R2/R0)*R2/R1/R0
- pVCpr2 ~= -Vt*(1+log(Ar*R2/R1)*R2/R0)/R0

Comparison

- pVCpVos ~=
  -(1+log(Ar*R2/R1)*R2/R0)*(1+log(Ar*R2/R1)+log(Ar*R2/R1)*R2 /R0)
  /(log(Ar*R2/R1)^2*R2/R0)
- pVCpA ~= VC*pVCpVos
- pVCpr1 ~= Vt*(1+log(Ar*R2/R1)+log(Ar*R2/R1)*R2/R0)*R2/R1/R0
- pVCpr2 ~= -Vt*(1+log(Ar*R2/R1)*R2/R0)/R0
- pVBEpT = k/q*(1-r)
  +log(log(Ar*R2/R1)*k*T/q*R2/R1/R0/sigma/A1/(T^r))*k/q+pVGpT
  = - log(Ar*R2/R1)*R2/R0*k/q @ Tinf
- pPTATpT= log(Ar*R2/R1)*R2/R0*k/q
- p^2VBEpT^2 = k/q/T*(1-r)+p^2VGpT^2 @ Tinf

Comparison

- pVCpVos ~= -(1+pPTATpT*q/k)*(R2/R0+pPTATpT*q/k+pPTATpT*q/k*R2/R0) /(pPTATpT*q/k)^2
- pVCpA ~= VC*pVCpVos
- pVCpr1 ~= Vt*(R2/R0+pPTATpT*q/k+pPTATpT*q/k*R2/R0)/R1
- pVCpr2 ~= -Vt*(1+pPTATpT*q/k)/R0
- pVBEpT = k/q*(1-r) +log(log(Ar*R2/R1)*k*T/q*R2/R1/R0/sigma/A1/(T^r))*k/q+pVGpT = - log(Ar*R2/R1)*R2/R0*k/q @ Tinf
- pPTATpT= log(Ar*R2/R1)*R2/R0*k/q log(Ar*R2/R1)*R2/R0=pPTATpT*q/k
- p^2VBEpT^2 = k/q/T*(1-r)+p^2VGpT^2 @ Tinf

Comparison

$$V_{ref} = V_G + V_t \ln\left(\frac{\ln(A_r \frac{R_2}{R_1}) V_t}{R_0 I_{sx1}} \frac{R_2}{R_1}\right)$$

$$+ R_2 \frac{V_t}{R_0} \ln(A_r \frac{R_2}{R_1}) + \frac{\partial V_{ref}}{\partial \Delta R_0} \Delta R_0$$

$$+ \frac{\partial V_{ref}}{\partial V_{os}} V_{os} + \frac{\partial V_{ref}}{\partial (1/A)} \frac{1}{A} + \frac{\partial V_{ref}}{\partial r_1} r_1 + \frac{\partial V_{ref}}{\partial r_2} r_2$$

$$\frac{\partial V_{ref}}{\partial \Delta R_0} = -\frac{T}{R_0} \frac{k}{q}$$

$$\frac{\partial V_{ref}}{\partial V_{os}} \cong -\frac{(\frac{k}{q} + \frac{\partial V_{PTAT}}{\partial T})(\frac{R_2}{R_0} \frac{k}{q} + (1 + \frac{R_2}{R_0}) \frac{\partial V_{PTAT}}{\partial T})}{(\frac{\partial V_{PTAT}}{\partial T})^2}$$

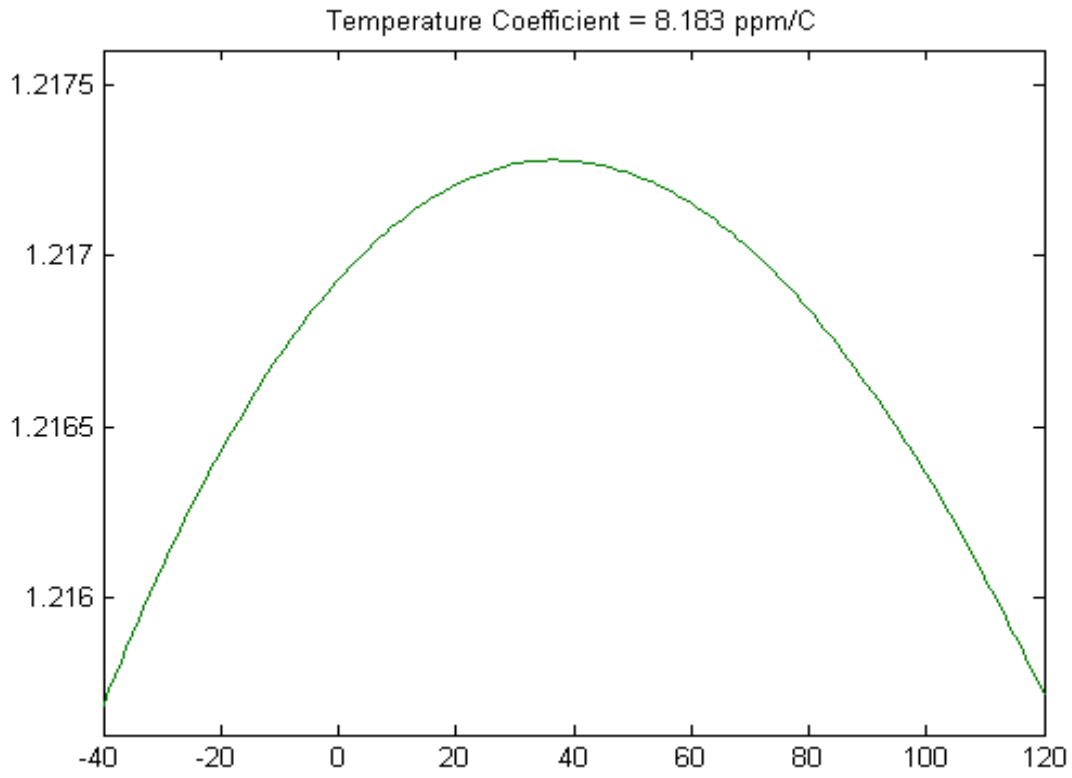
$$\frac{\partial V_{ref}}{\partial (1/A)} \cong V_{ref} \frac{\partial V_{ref}}{\partial V_{os}}$$

$$\frac{\partial V_{ref}}{\partial r_1} \cong \frac{T}{R_1} (\frac{R_2}{R_0} \frac{k}{q} + (1 + \frac{R_2}{R_0}) \frac{\partial V_{PTAT}}{\partial T})$$

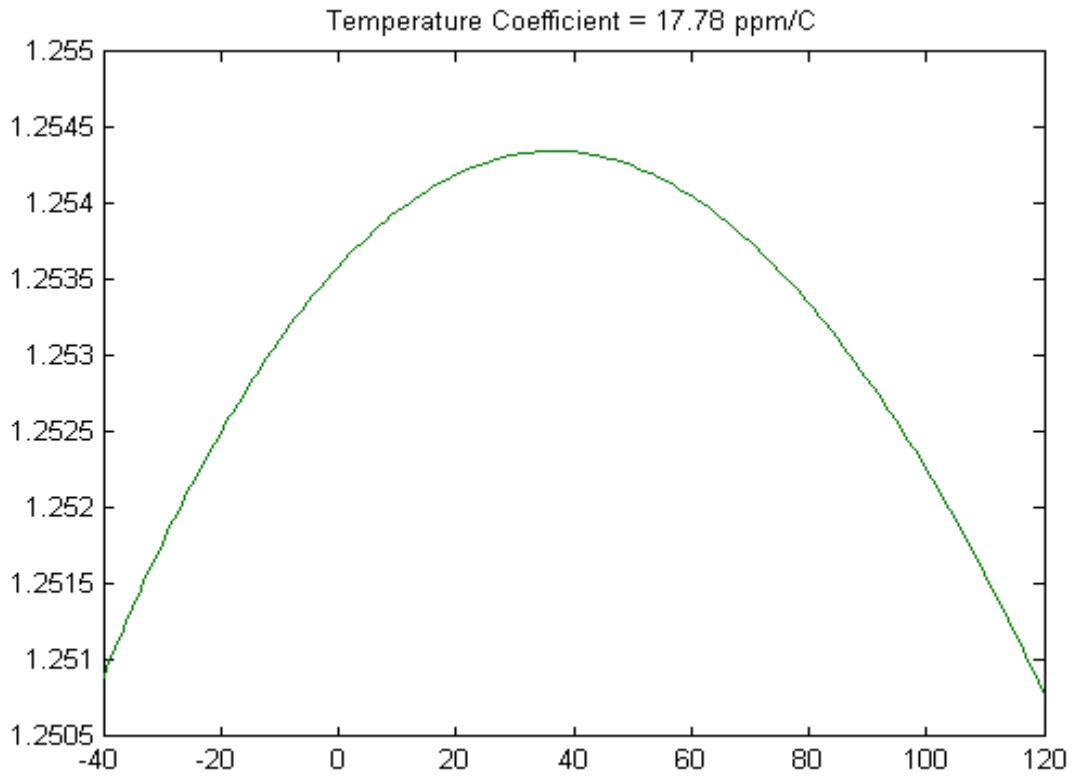
$$\frac{\partial V_{ref}}{\partial r_2} \cong -\frac{T}{R_0} (\frac{k}{q} + \frac{\partial V_{PTAT}}{\partial T})$$

$$\frac{\partial V_{PTAT}}{\partial T} \cong \ln(A_r \frac{R_2}{R_1}) \frac{R_2}{R_0} \frac{k}{q}$$

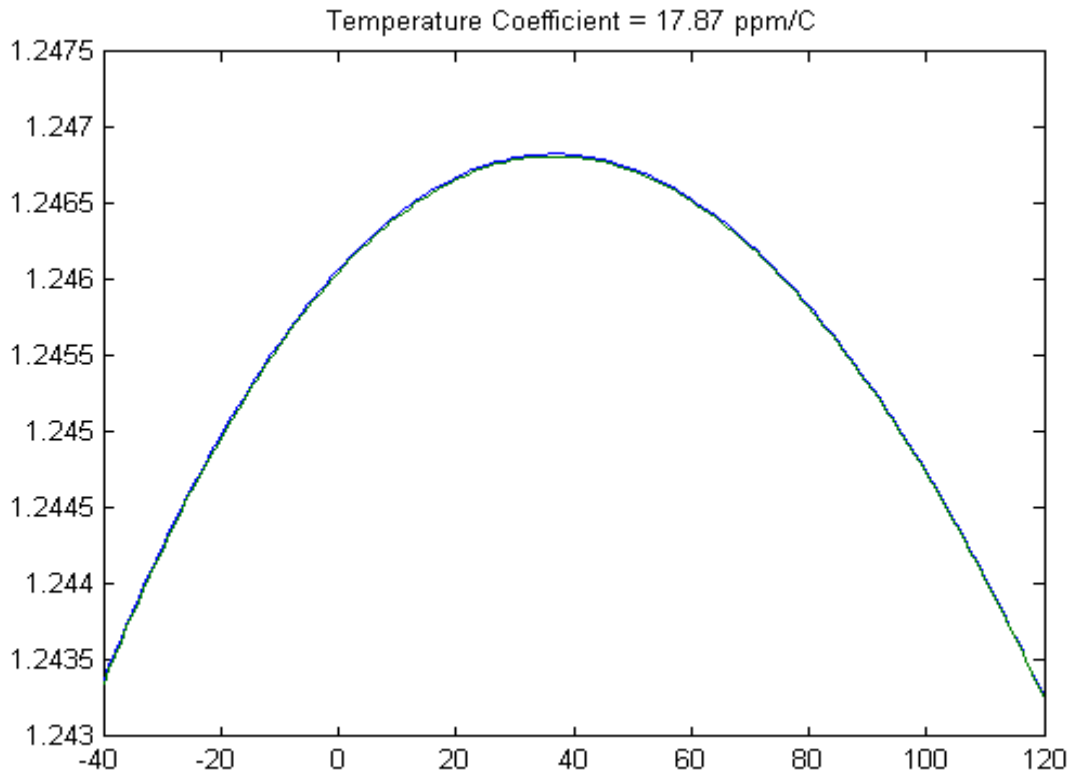
R0 = 1225 ohm, Vos = 0
T-independent Silicon Bandgap



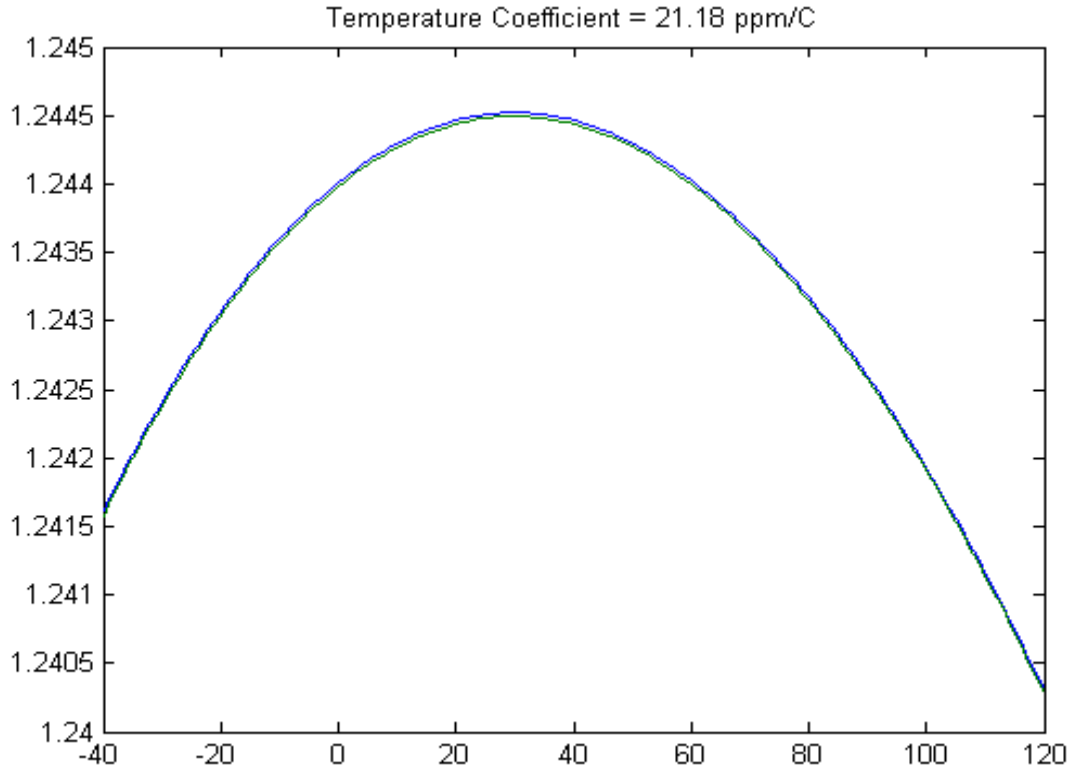
R0 = 1109 ohm, Vos = 0
T-dependent Silicon Bandgap



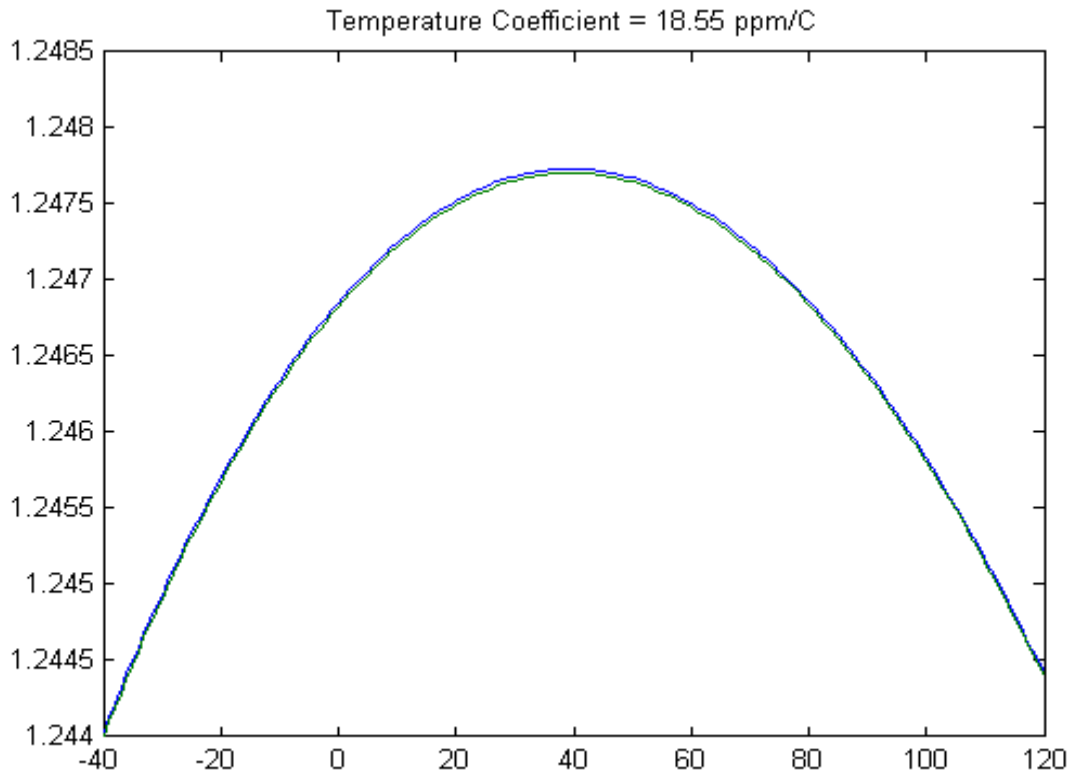
R0 = 1109 ohm, Vos = 1 mV with no TC
T-dependent Silicon Bandgap



R0 = 1109 ohm, Vos = 1 mV with 1000 ppm TC T-dependent Silicon Bandgap



R0 = 1100 ohm, Vos = 1 mV with 1000 ppm TC T-dependent Silicon Bandgap



- Vref = VG+log(log(Ar*R2/R1)*Vt*R2/R1/R0/Isx1)*Vt
  +log(Ar*R2/R1)*Vt*R2/R0
- VBE = VG + log(log(Ar*R2/R1)*Vt*R2/R1/R0/Isx1)*Vt
  = VG + log(log(Ar*R2/R1)*(k*T/q)*R2/R1/R0/(sigma*A1*T^r))*(k*T/q)
- PTAT = log(Ar*R2/R1)*R2/R0*k*T/q
- pVBEpT = k/q*(1-r)
  +log(log(Ar*R2/R1)*k*T/q*R2/R1/R0/sigma/A1/(T^r))*k/q+pVGpT
  = - log(Ar*R2/R1)*R2/R0*k/q @ Tinf
- pPTATpT= log(Ar*R2/R1)*R2/R0*k/q
- p^2VBEpT^2 = k/q/T*(1-r)+p^2VGpT^2 @ Tinf

Simplification

- pVCpr1 ~=
  ID1^2*R1*(ID2*R0+Vt+ID2*R2)/(ID1*R0*R1*ID2)
  = Vt*(1+log(Ar*R2/R1)+log(Ar*R2/R1)*R2/R0)*R2/R1/R0
- pVCpr2 ~= -Vt(1+log(Ar*R2/R1)*R2/R0)/R0
- ID1=log(Ar*R2/R1)*Vt*R2/R1/R0
- ID2=log(Ar*R2/R1)*Vt/R0