Department of Electronics and Communication Engineering

Sub Code/Name: BEC6L3-COMMUNICATION ENGINEERING-II LAB

Name : ..............................................
Reg No : ..............................................
Branch : ..............................................
Year & Semester : ..............................................
### LIST OF EXPERIMENTS

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<td></td>
</tr>
</tbody>
</table>
FSK MODULATION AND DEMODULATION.

AIM:
To design and plot a graph for FSK modulator and Demodulator circuit.

APPARATUS REQUIRED:

<table>
<thead>
<tr>
<th>SL NO.</th>
<th>APPARATUS</th>
<th>RANGE</th>
<th>QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IC 555</td>
<td>-</td>
<td>1No</td>
</tr>
<tr>
<td>2</td>
<td>Transistor</td>
<td>BC 557-PNP</td>
<td>1No</td>
</tr>
<tr>
<td>3</td>
<td>Resistor</td>
<td>(4.7KΩ, 600Ω)</td>
<td>1No</td>
</tr>
<tr>
<td>4</td>
<td>Potentiometer</td>
<td>(50KΩ)</td>
<td>2No</td>
</tr>
<tr>
<td>5</td>
<td>Capacitor</td>
<td>(0.01µF)</td>
<td>2No</td>
</tr>
<tr>
<td>6</td>
<td>AFO with dc shift</td>
<td>(0-1MHz)</td>
<td>1No</td>
</tr>
<tr>
<td>7</td>
<td>DSO</td>
<td>-</td>
<td>1No</td>
</tr>
<tr>
<td>8</td>
<td>RPS</td>
<td>(0-30v)</td>
<td>1No</td>
</tr>
<tr>
<td>9</td>
<td>Connecting wires and breadboard</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

SPECIFICATIONS:

IC555- 4 to 18V, -55 to 125C
PNP Transistor- 50V, 1A, 5W, and 150MHz
All resistors are carbon film ¼ watt resistors.
Capacitors :-0. 01µF-ceramic capacitor.

THEORY:

Frequency Shift Keying (FSK):

Frequency shift keying is defined as a signaling technique in which the amplitude of the carrier signal is keyed or switched based on the incoming data or signal.

In digital data communication, shifting a carrier frequency between two preset frequencies transmits binary code. This type of transmission is called frequency shift keying (FSK) technique. A 555 timer in astable mode can be used to generate FSK signal.

The standard digital data input frequency is 150Hz when input is HIGH, the transistor Q is off and 555 timer works in the normal astable mode of operation. The frequency of the output waveform is given by
\[ f_0 = \frac{1.45}{(R_A + 2R_B)C} \]

In a tele-typewriter using a modulator–demodulator (MODEM), a frequency between 1070Hz to 1270Hz is used as one of the standard FSK Signals. The components \( R_A \) and \( R_B \) and the capacitor \( C \) can be selected so that \( f_0 \) is 1070Hz.

**CIRCUIT DIAGRAM: FSK Modulator**

![Circuit Diagram](image-url)
FSK Demodulator Circuit:

PIN DIAGRAM (TOP VIEW):

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ground</td>
</tr>
<tr>
<td>2</td>
<td>Trigger</td>
</tr>
<tr>
<td>3</td>
<td>Output</td>
</tr>
<tr>
<td>4</td>
<td>Reset</td>
</tr>
<tr>
<td>cc</td>
<td></td>
</tr>
<tr>
<td>Ischarge</td>
<td></td>
</tr>
<tr>
<td>threshold</td>
<td></td>
</tr>
<tr>
<td>control voltage</td>
<td></td>
</tr>
</tbody>
</table>
When the input is LOW, Q goes on & connects the resistance $R_c$ across $R_A$. The output frequency is now given by

$$f_0 = \frac{1.45}{(R_A - R_c + 2R_B)}$$

The resistance $R_c$ can be adjusted to get an output frequency 1270Hz.

**PROCEDURE:**
1. The circuit connections are made as shown in figure.
2. The free running frequency of the astable multivibrator is measured using CRO.
3. The input square wave (digital data) is given from the AFO.
4. The FSK waveform is noted from the CRO and plotted.

**RESULT:**

Thus the FSK modulation and demodulation circuits were designed and graph plotted.
FREQUENCY SHIFT KEYING MODULATION & DETECTION

AIM: To generate FSK modulation and demodulation signals.

EQUIPMENT REQUIRED:

- FSK modulation and demodulation kit
- CRO
- BNC probes
- Patch cards.

BLOCK DIAGRAM:
THEORY:

In FSK systems two sinusoidal carrier waves of same amplitude AC but different frequencies \( f_{C1} \) and \( f_{C2} \) are used to represent binary symbols 1 and 0 respectively.

\[
\text{I.e. } S(t) = A_c \cos(2 \pi f_{C1} t) \quad \text{symbol 1} \\
= A_c \cos(2 \pi f_{C2} t) \quad \text{symbol 2}
\]

The FSK is essentially a superposition of two ASK waveforms one with frequency \( f_{C1} \) and the other with \( f_{C2} \). Hence the PSD of FSK is the sum of two ASKS specter at frequencies \( f_{C1} \) and \( f_{C2} \). The bandwidths of FSK are higher than that of psk and ask. The application of FSK signals is in low speed digital data transmission.

Generation of FSK:

The FSK signal can be generated by applying the incoming binary data to a frequency modulator and to other input a sinusoidal carrier wave of amplitude \( A_c \) and frequency \( f_c \) is applied. As the binary data changes form one level to another (but non zero being pear) the output changes its frequencies is the corresponding manner.

Detection of FSK:

FSK can be demodulated using synchronous or coherent detector. This type of detection or digital communication reception is also known as correlation reception. The coherent detection requires phase and time synchronization.

PROCEDURE:

1. Switch 'ON' the power to the Trainer.
2. Observe the clock frequency on the oscilloscope.
3. Apply the clock to the decade counter (7490). And vary the data outputs and draw the data outs.
4. Select one data output of the decade counter to the data input point of the FSK modulator and observe the same signal one channel of a dual trace oscilloscope.

5. Observe the output of the FSK modulator on the second channel of the CRO.

6. Apply the FSK modulator output to demodulator input. Adjust the potentiometers P1 & P2 until we get the demodulated output equivalent to the modulating data signal.

MODEL GRAPHS:

RESULT: Hence generated frequency modulated and demodulated signals
VIVA QUESTIONS:

1. Define Binary FSK signal?
2. What is meant by carrier swing?
3. Define Frequency deviation of FSK signal?
4. What are the advantages of this FSK signal?
5. Give the differences between FSK & FM?
PHASE SHIFT KEYING GENERATION & DETECTION

AIM:

To study the operation of phase Shift Key Modulation and Demodulation.

EQUIPMENT REQUIRED:

PSK Modulations and Demodulation Trainer kit
CRO
BNC probes
Patch cards

BLOCK DIAGRAM:
Phase shift keying or discrete phase modulation is another technique available for communicating digital information over band pass channels. The psk is a form of angle modulated, constant amplitude digital modulation. In binary phase shift keying two output phases are possible for a single carrier frequency as the input digital signal changes state, the phase of the output carrier shifts between $180^0$ out of phase.

In binary phase shift keying modulation the balanced modulator acts as a phase reversing switch. Depending on the logic condition of the digital input, the carrier is transferred to the output either in phase or $180^0$ with reference carrier oscillators and for proper operation the digital input voltages must be greater than the peak carrier voltage as it has to control ON-OFF of diodes.

The coherent detection also called synchronous detection is used for binary phase shift keying detection. It is more complicated than envelope detector, and results in a lower probability of error for a given S/N input. Synchronous detection requires a carrier recovery circuit to generate local carrier component exactly synchronized to the transmitted carrier.

The primary advantage of the psk signaling scheme lies in its superior performance over the amplitude shift-keying scheme operating under the same peak power limitations and noise environment.
PROCEDURE: -

1. Switch ON the experimental board.
2. Apply the carrier signal to the input of the modulator.
3. Apply the modulating data signal to the modulator input and observe this signal on one channel 1 of the CRO.
4. Observe the output of the PSK modulator on the channel 2 of the CRO.
5. Apply this PSK output to the demodulator input and also apply the carrier input.

6. Observe the demodulator output and compare it with the modulating data signal applied to the modulator input.

**RESULTS:** Hence generated Phase modulated and demodulated signals

**VIVA QUESTIONS:**

1. Define PSK?
2. Explain the generation proven of PSK?
3. Differentiate PSK & PM?
4. Give the application of PSK?
5. PSK is which type of modulation?
6. Compare PSK & FSK?
7. Give the advantages PSK?
Differential Phase Shift Keying Modulation & Demodulation

AIM:

To study the various steps involved in generating the differential binary signal and differential phases shift keyed signal at the modulator end and recovering the binary signal from the received DPSK signal.

EQUIPMENT REQUIRED:

DPSK modulations and demodulation trainer kit
CRO
BNC probes
Patch cards

BLOCK DIAGRAM:
THEORY:

The differentially phase shift keying makes use of a technique designed to get around the need for a coherent reference signal at the receiver. In the differential phase shift keying scheme. The phase reference for the demodulation is derived form the phase of the carrier during the preceding signaling interval and the receiver decodes the digital information“s based on the differential phase. If the channel perturbations and other disturbances are slowly varying compared to the bit rate than the phase of the RF pulse are affected by the same manner, thus preserving the information contained in the phase difference. If the digital information had been differentially encoded in the carrier phase the transmitter the decoding at the receiver can be accomplished without a coherent load oscillator signal.

MODULATION:

The differential signal to the modulating signal is generated using an Exclusive OR gate and 1-bit delay circuit (It is shown in figure). CD4051 is an analog multiplexer to which carrier is applied with and without $180^\circ$ phase shift (created by using an operational amplifier connected in inverting amplifier mode) to the two inputs of the ICTL084. Differential signal generated by Ex-OR gate (IC7486) is given to the multiplier“s control signal input. Depending upon the level of control signal, carrier signal applied with or without phase shift is steered to the output.1- bit delay generation of differential signal to the input is created by using a D- flip-flop (IC7474).

DEMODULATION:

During the demodulation, the DPSK signal is converted into a $+5V$ Square Wave signal using a transistor and is applied to one input of an EX-OR gate. To
signal. So the EX-OR gate output is equivalent to the differential signal of the modulating data. This differential data is applied to one input of an EX-OR gate and to the second input, after 1-bit delay the same signal is given. So the output of this Ex-OR gate is modulating signal.

PROCEDURE:

1. Switch ON' the experimental board.
2. Check the carrier signal and the data generator signals initially.
3. Apply the carrier signal to the carrier input of the DPSK modulator and give the data generator to the data input of DPSK modulator and bit clock output to the input of DPSK modulator.
4. Observe the DPSK modulating output with respect to the input data generator signal of dual trace oscilloscope (observe the DPSK modulating signal on channel 1 and the data generator signal on channel 2).
5. Give the output of the DPSK modulator signal to the input of demodulator, give the bit clock output to the bit clock input to the demodulator and also give the carrier output to the carrier input of demodulator.
6. Observe the demodulator output with respect to data generator signal (modulating signal)
RESULT:
Hence generated the differential binary signal and differential phases shift keyed signal at the modulator end and recovered the binary signal from the received DPSK signal.
PULSE AMPLITUDE MODULATION & DEMODULATION

Aim: To generate the Pulse Amplitude modulated and demodulated signals.

Apparatus required:

<table>
<thead>
<tr>
<th>Name of the Apparatus</th>
<th>Specifications/Range</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistors</td>
<td>1K, 10K, 100K, 5.8K, 2.2K</td>
<td>Each one</td>
</tr>
<tr>
<td>Transistor</td>
<td>BC 107</td>
<td>2</td>
</tr>
<tr>
<td>Capacitor</td>
<td>10μF, 0.001μF</td>
<td>Each one</td>
</tr>
<tr>
<td>CRO</td>
<td>30MHz</td>
<td>1</td>
</tr>
<tr>
<td>Function generator</td>
<td>1MHz</td>
<td>1</td>
</tr>
<tr>
<td>Regulated Power Supply</td>
<td>0-30V, 1A</td>
<td>1</td>
</tr>
<tr>
<td>CRO Probes</td>
<td>---</td>
<td>1</td>
</tr>
</tbody>
</table>

Theory:

PAM is the simplest form of data modulation. The amplitude of uniformly spaced pulses is varied in proportion to the corresponding sample values of a continuous message m(t).

A PAM waveform consists of a sequence of flat-topped pulses. The amplitude of each pulse corresponds to the value of the message signal x(t) at the leading edge of the pulse.

The pulse amplitude modulation is the process in which the amplitudes of regularity spaced rectangular pulses vary with the instantaneous sample values of a continuous message signal in a one-one fashion. A PAM wave is represented mathematically as,

\[ S(t) = \sum_{n=-\infty}^{\infty} [1+K_a x(nT_s)] P(t-nT_s) \]

Where
$x(nT_s) =>$ represents the $n^{th}$ sample of the message signal $x(t)$

$K =>$ is the sampling period.

$K_a =>$ a constant called amplitude sensitivity

$P(t) =>$ denotes a pulse

PAM is of two types

1) Double polarity PAM => This is the PAM wave which consists of both positive and negative pulses shown as

2) Single polarity PAM => This consists of PAM wave of only either negative (or) positive pulses. In this the fixed dc level is added to the signal to ensure single polarity signal. It is represented as

![Fig: 1 Bipolar PAM signal](image1)

![Fig: 2 Single polarity PAM](image2)
Circuit Diagram:

Fig: Pulse Amplitude Modulation Circuit

Fig: Demodulation Circuit

Procedure:

1. Connect the circuit as per the circuit diagram shown in the fig 3
2. Set the modulating frequency to 1KHz and sampling frequency to 12KHz
3. Observe the o/p on CRO i.e. PAM wave.
4. Measure the levels of $E_{\text{max}}$ & $E_{\text{min}}$.
5. Feed the modulated wave to the low pass filter as in fig 4.
6. The output observed on CRO will be the demodulated wave.
7. Note down the amplitude (p-p) and time period of the demodulated wave. Vary the amplitude and frequency of modulating signal. Observe and note down the changes in output.
8. Plot the wave forms on graph sheet.

RESULT: Thus the Pulse Amplitude modulated waves were generated and demodulated.
Aim: To generate the pulse width modulated and demodulated signals

Apparatus required:

<table>
<thead>
<tr>
<th>Name of the Apparatus</th>
<th>Specifications/Range</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistors</td>
<td>1.2k, 1.5k, 8.2k</td>
<td>1, 1, 2</td>
</tr>
<tr>
<td>Capacitors</td>
<td>0.01 μF, 1 μF</td>
<td>2, 2</td>
</tr>
<tr>
<td>Diode</td>
<td>0A79</td>
<td>1</td>
</tr>
<tr>
<td>CRO</td>
<td>0-30 MHz</td>
<td>1</td>
</tr>
<tr>
<td>Function Generator</td>
<td>1MHz</td>
<td>1</td>
</tr>
<tr>
<td>RPS</td>
<td>0-30V, 1A</td>
<td>1</td>
</tr>
<tr>
<td>IC 555</td>
<td>Operating temp: SE 555 -55°C to 125°C</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>NE 555 0°C to 70°C</td>
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</tr>
<tr>
<td></td>
<td>Supply voltage: +5V to +18V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Temperature stability: 50 PPM/°C</td>
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<tr>
<td>CRO Probes</td>
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</tr>
</tbody>
</table>

Theory:

Pulse Time Modulation is also known as Pulse Width Modulation or Pulse Length Modulation. In PWM, the samples of the message signal are used to vary the duration of the individual pulses. Width may be varied by varying the time of occurrence of leading edge, the trailing edge or both edges of the pulse in accordance with modulating wave. It is also called Pulse Duration Modulation.
**Circuit Diagram:**

- **Fig: 1 Pulse Width Modulation Circuit**

- **Fig: 2 Demodulation Circuit**

**Procedure:**

1. Connect the circuit as per circuit diagram shown in fig 1.
2. Apply a trigger signal (Pulse wave) of frequency 2 KHz with amplitude of 5v (p-p).
3. Observe the sample signal at the pin3.
4. Apply the ac signal at the pin 5 and vary the amplitude.
5. Note that as the control voltage is varied output pulse width is also varied.
6. Observe that the pulse width increases during positive slope condition & decreases under negative slope condition. Pulse width will be maximum at the +ve peak and minimum at the –ve peak of sinusoidal waveform. Record the observations.
7. Feed PWM waveform to the circuit of Fig.2 and observe the resulting demodulated waveform.

**Observations:**

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Control voltage ($V_{pp}$)</th>
<th>Output pulse width (m sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

**Result:**

Thus the PWM modulation and Demodulation circuits were constructed and graph was plotted.
PULSE POSITION MODULATION & DEMODULATION

Aim: To generate pulse position modulation and demodulation signals and to study the effect of amplitude of the modulating signal on output.

Apparatus required:

<table>
<thead>
<tr>
<th>Name of the apparatus</th>
<th>Specifications/Range</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistors</td>
<td>3.9k, 3k, 10k, 680k</td>
<td>Each one</td>
</tr>
<tr>
<td>Capacitors</td>
<td>0.01µF, 60µF</td>
<td>2,1</td>
</tr>
<tr>
<td>Function Generator</td>
<td>1MHz</td>
<td>1</td>
</tr>
<tr>
<td>RPS</td>
<td>0-30V, 1A</td>
<td>1</td>
</tr>
<tr>
<td>CRO</td>
<td>0-30MHz</td>
<td>1</td>
</tr>
<tr>
<td>IC 555</td>
<td>Operating tem :SE 555 -55°C to 125°C</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>NE 555 0° to 70°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Supply voltage :+5V to +18V</td>
<td></td>
</tr>
<tr>
<td>CRO Probes</td>
<td>----</td>
<td>1</td>
</tr>
</tbody>
</table>

Theory:

In Pulse Position Modulation, both the pulse amplitude and pulse duration are held constant but the position of the pulse is varied in proportional to the sampled values of the message signal. Pulse time modulation is a class of signaling techniques that encodes the sample values of an analog signal on to the time axis of a digital signal and it is analogous to angle modulation techniques. The two main types of PTM are PWM and PPM. In PPM the analog sample value determines the position of a narrow pulse relative to the clocking time. In PPM rise time of pulse decides the channel bandwidth. It has low noise interference.
Circuit Diagram:

Fig: 1 Pulse Position Modulation Circuit

Fig: 2 Demodulation Circuit

Procedure:

1. Connect the circuit as per circuit diagram as shown in the fig 1.
2. Observe the sample output at pin 3 and observe the position of the pulses on CRO and adjust the amplitude by slightly increasing the power supply. Also observe the frequency of pulse output.
3. Apply the modulating signal, sinusoidal signal of 2V \((p-p)\) \((ac\ \text{signal})\) 2v \((p-p)\) to the control pin 5 using function generator.
4. Now by varying the amplitude of the modulating signal, note down the position of the pulses.
5. During the demodulation process, give the PPM signal as input to the demodulated circuit as shown in Fig.2.
6. Observe the o/p on CRO.
7. Plot the waveform.
Observations:

<table>
<thead>
<tr>
<th>Modulating signal Amplitude($V_{p-p}$)</th>
<th>Time period(ms)</th>
<th>Pulse width ON (ms)</th>
<th>Pulse width OFF (ms)</th>
<th>Total Time period(ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tbody>
</table>

RESULT: Thus pulse position modulation and demodulation signals were generated and the Output was plotted
Ex No: 8
Date:

PULSE CODE MODULATION AND DEMODULATION

AIM:
To analyze a PCM system and interpret the modulated and demodulated waveforms for a given sampling frequency.

EQUIPMENT REQUIRED:
1. Pulse code modulation and demodulation trainer kit.
2. Connecting chords.
3. Power supply.
4. 30 MHz Dual Storage Oscilloscope.

THEORY:
The sine waves (analog signal) of frequency 500Hz and 1 KHz and DC signal DC1 and DC2 whose amplitude can be varied accordingly are generated on board on DCL-03. These signals are fed to the input of the sampling logic CH0 & CH1 and their samples are multiplexed by interleaving them properly in their time slots.

The crystal oscillator generates a clock of 6.4 MHz from which all the transmitter data and timing signals are derived for fast mode operation the transmitter clock is 240 KHz, and sampling clock is 16KHz. For slow mode operation depending on jumper position the transmitter clock is 1.23Hz or 0.6Hz and sampling clock is 0.088Hz or 0.044 i.e. the sampling rate per channel is 11 or 22 seconds and serial data transmission rate is 813 milliseconds or 1.6 seconds.

The multiplexed data is pulse code modulated before transmission. At the receiver after the pulse code modulation, the recovered multiplexed data is sent to de-multiplexing logic. The two demultiplexed samples are fed to reconstruction unit which consists of 4th order low pass butter-worth filter, where frequency components are filtered out to recover the original base band signal at the receiver output CH0 and CH1.
Block Diagram DESCRIPTION

Function generator

Transmitter timing logic two different frequencies say 16 KHz & 8 KHz are taken. This signal is fed to parallel shift register U25, U27 (IC 74HC164), which generates the sine wave, by serial shift operations. The serial to parallel shift register (IC74HC164) has resistive ladder network at the output. For 16 shifts of the register, one stair case sine wave is produced. So if a 16 KHz clock is fed to the shift register, 1KHz sine wave is generated and similarly 500Hz sine waveform with amplitude variable form 0-5volts. Two amplitude variable DC levels are also generated which are used as analog information signals for both FAST and SLOW mode operations.

Clock generator

This block consists of crystal Oscillator, which generates a 6.4 MHz clock, from IC 74LS04 and supplied to U2 (IC74390) decade counter from which all the transmitter data and timing signals are derived.

Transmitter timing logic

This logic generates the various timing signals for the transmitter two synchronized amplitude variable sine waves are generated which are used as analog information signals for fast mode operations. The 6.4MHz crystal oscillators generate a 7.4Mhz clock. It is divided by 2-decade counter U2 (IC74LS30) and ripple counter U3 (IC 74LS393) to get the 32KHz, 16KHZ, 8KHz and 4KHz frequencies. This logic also generates 240 KHz transmitter clock with the help of two input mux U6 (IC74LS157) and JK flip-flop U11 (IC74LS74) 16KHz sampling clock for FAST mode operations, and 1.23Hz & 0.6Hz Transmitter clock and 0.088hz & 0.044Hz sampling clock for SLOW mode operations. A frame sync signal is also generated By U3, U10 and U11 this logic for synchronization purposes.
Sample and hold logic

This logic samples the two information signals from the signals from the two analog input, using (IC4016)U30.

Multiplexer logic

Two signals available at CH0 IN &CH1IN are multiplexed their samples by interleaving them properly in their assigned time slots controlled by timing signals TM1and TM-2 generated from U9(IC74LS74).The capacitor is provided at the output of the third buffer to provide a sample and hold mode to U30,which is a sampling switch CD4016.

Analog to digital converter

The analog to digital converter converts the analog samples to digital bits. This device performs both quantizing and encoding operations. The analog to digital converter IC, AD673 forms the heart of this logic .AD673 is used for the analog to digital conversion of the multiplexed data. The timing of the A/D conversion is controlled by the convert pulse, which is generated in the transmitter timing logics. As soon as the data is ready, the AD673 gives a data ready (DR Active low) output. The data latch is used for latching the valid outputs A/D converter. The timing and latching interval of data latch is controlled by the latch enable signal U22 (74HCT374).Each sample is coded to a 7 bit data by the AD673.

Quantising And Encoding

The signal level of the input signal assumed to vary from 0volts to 4.96 volts. The entire level is dividing to 128 uniform steps .Each step corresponds to 4.96V/128=40mV

The quantizing level is chosen to be midway of steps .If the signal level falls below the quantizing level, and then the signal is rounded off to lower level. If signal level falls above the quantizing level, and then, the signal is rounded off to the upper level. This type of quantizing is called “uniform quantizing, where the step levels are uniform. Then the corresponding to the level chosen, code words are assigned to the samples. The code words vary from 0000000 to 1111111 for the 0 to 4.96V.Thus analog to digital converter assigns the code words for all the samples
PROCEDURE:
1) Connect power supply in proper polarity to the kits DCL-03 and DCL-04 and switch it on.
2) Connect sine wave of frequency 500Hz and 1KHz to the input CH0 and CH1 of the sample and hold logic.
3) Connect OUT0 to CH0 IN &CH IN.
4) Set the speed selection switch SW1 to FAST mode.
5) Select parity selection switch to NONE mode on both the kit DCL-03 and DCL-04 as shown in switch setting diagram.
6) Connect TXDATA, TXCLK and TXSYNC of the transmitter section DCL-03 to the corresponding RX DATA, RXCLK and RXSYNC of the receiver section DCL-04.
7) Connect DACOUT to IN post of demultiplexer section in DCL-04.
8) Ensure that FAULT SWITCH SF1 as shown in switch setting diagram introduces no fault.
9) Take the observations as mentioned below.
10) Repeat the above experiment with DC signal at the inputs of the channel CH0 and CH1.
11) Connect the ground points of both the kits with the help of connecting chord provided during all experiments.

OBSERVATIONS:

<table>
<thead>
<tr>
<th>PCM Modulation</th>
<th>Amplitude</th>
<th>Time Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC input</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sample and hold signal</td>
<td></td>
<td></td>
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<tr>
<td>Clock signal(4 KHz)</td>
<td></td>
<td></td>
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<tr>
<td>Clock signal(64 KHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCM Output</td>
<td></td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>PCM Demodulation</th>
<th>Amplitude</th>
<th>Time Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>D/A Converter output Signal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LPF output signal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Demodulated output</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
PRECAUTIONS

1) Connect the power supply with proper polarity.
2) Do not make any interconnections when the power supply is on.
3) Keep all the switch faults in off position.

RESULT:

Thus the PCM system was analyzed and interpreted, the modulated and demodulated waveforms for a given signal also plotted.
DELTA MODULATION AND DEMODULATION

Aim:
To analyze a Delta modulation system and interpret the modulated and demodulated waveforms

HARDWARE REQUIRED

1. PCM Modulator trainer - AET-73M
2. PCM Demodulator trainer - AET-73D
3. Storage Oscilloscope
4. Digital Multimeter
5. Co-axial cables (standard accessories with AET-73 trainer)

INTRODUCTION

Delta Modulation is a form of pulse modulation where a sample value is represented as a single bit. This is almost similar to differential PCM, as the transmitted bit is only one per sample just to indicate whether the present sample is larger or smaller than the previous one. The encoding, decoding and quantizing process become extremely simple but this system cannot handle rapidly varying samples. This increases the quantizing noise.

The trainer is a self sustained and well organized kit for the demonstration of delta modulation & demodulation. The system consist of:

DM Modulator (AET-73M) trainer kit
1. Regulated power supply
2. Audio Frequency signal generator
3. Buffer/signal shaping network
4. Voltage comparator
5. 4 Bit UP/DOWN counter
6. Clock generator/Timing circuit
7. 4 Bit D/A converter
8. DC source

DM Demodulator (AET-73D) trainer kit
1. Regulated power supply
2. 4 Bit UP/DOWN counter
3. 4 Bit D/A converter
4. Clock generator
5. Passive low pass filter

Audio amplifier

**Regulated power supply (73M & 73D):**

This consists of a bridge rectifier followed by Capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of +5V and +12V@ 300mA each to the on board circuits. These supplies have been internally connected to the circuits. so no external connections are required for operation.

**Audio Frequency (AF) S signal generator (73M):**

Sine wave signal of 100 Hz is generated to use as a modulating (message or information) signal to be transmitted. This is an Op-Amp based Wein bridge Oscillators using IC TL084 is a FET.input general purpose Operational Amplifier .Amplitude control is provided in the circuit to vary the output amplitude of AF signal.

**Clock generator/Timing circuit (73M & 73D):**

A TTL compatible clock signal of 4 KHz frequency is provided on board to use as a clock to the various circuits in the system. This circuit is a astable multivibrator using 555 timer followed by a buffer.

**DC Source (73M):**

A 0 to +5V variable DC voltage is provided on board to use as a modulating signal instead of AF Signal. is useful to study step by step operation of Delta modulation and Demodulation. This is a simple circuit consists of potentiometer and fixed power supply.

**Buffer/Signal shaping circuit (73M):**

A non inverting buffer using IC TL 084 is provided at the input of the DM modulator followed by a level shifting network. Buffer provides the isolation between DM circuit and the signal source. Signal Shaping super imposes the 1.5V DC on incoming modulating signal so that the input of the comparator lies between 0 and +3V maximum.
4.4 BLOCK DIAGRAM

**Fig.4.1. DM Modulator**

**Fig.4.2. DM Demodulator**

**Voltage comparator (73D):**

This circuit is build with IC LM339. The LM339 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2mV for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the common mode voltage range includes ground, even though operated from a single power supply voltage. Application areas include limit comparators simple analog to digital converters: pulse, square and time delay generators, wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power
supplies, they will directly interface with MOS logic where the low power drain of the LM339 is a distinct advantage over standard comparators. For circuit connections and other operating conditions.

**Low pass filters (73D):**

This is a series of simple RC networks provided on board to smoothen the output of the D/A converter output. RC values are chosen such that the cutoff frequency would be at 100 Hz.

**Amplifiers (73D):**

This is an Op-amp (IC TL084) based non-inverting variable gain amplifiers provided on board to amplify the recovered message singles i.e. output of low pass filter to desired level. Amplitude control is provided in circuit to vary the gain of the amplifier between 0 and 6. AC/DC Switch facilitates to couple the input signal through capacitor to directly to the amplifier input.

**4 Bit UP/DOWN Counter (73M & 73 D):**

This circuit is made using Synchronous 4-Bit Up/Down Counter with Mode Control IC 74LS191. The DM 74LS191 circuit is a synchronous, reversible, counter. Synchronous operation is provided by having all flip-flops clocked simultaneously. so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with the asynchronous counters. The outputs of the four master slave flip flops are triggered on a LOW to HIGH level transition of the clock input. if the enable input is LOW a HIGH at the enable input inhibits counting .Level changes at either the enable input or the down/up input should be made only when the clock input is HIGH. The direction of the count is determined by the level of the down/up input. When LOW the counter counts up and when HIGH it counts down. The counter is fully programmable that is the outputs may be preset to either level by placing a LOW on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. The clock, down/up and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers required for parallel words. The ripple clock input produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be easily
cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high speed operation.

4 Bit D/A converter (AET-73M & 73D):

This has been constructed with a popular 8 bit D/A Converter IC DAC 0808. The DAC0808 is an 8-bit monolithic DAC featuring a full scale output current settling time of 150 Ns while dissipating only 33 mW with +5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically \pm 1 LSB of 255 I_{REF}/256. Relative accuracies of better than \pm 0.19% assure 8 bit monotonic and linearity while zero level output current of less than 4 \mu A provides 8-bit zero accuracy for I_{REF} [greater than or equal] 2 math power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range. 4 LSB Bits are permanently grounded to make 4 bit converter. For complete specifications and operating conditions please refer the data sheet of DAC0808.

DM Operation:

Figure 4.1 shows the basic block diagram of the PCM system. The modulating signal is applied to buffer /signal shaping network. This applied signal will be superimposed by +1.5V DC so that the negative portion the modulating signal will clamped to positive, this process is needed, because input of the comparator should be between 0 and +3V.

After level shifting is done the signal will be passed to inverting input of the comparator. On inverting input of the comparator is connected to output of the 4 Bit D/A converter. Comparator is operating at +5V single supply. So output of the comparator will be high (i.e. +ve V_{ast}) when modulating signal is less than the reference signal i.e. D/A output, otherwise it will be 0V. And this signal is transmitted as DM signal. Same signal is also connected as UP/DOWN control to the UP/DOWN counter (74LS 191).

UP/DOWN counter is programmed for 0000 starting count. So initially output of the counter is at 0000 and the D/A converter will be at 0V. Comparator compares the modulating signal is greater than the reference signal. For next clock pulse depending on the UP/DOWN input counter will count up or down. If the UP/DOWN input is low (nothing but comparator output).
Counter will make up and output will be 0001. So the D/A converter will convert this 0001 digital input to equivalent analog signal (i.e. 0.3V 1 LSB Value). Now the reference signal is 0.3V. If still modulating signal is greater than the D/A output again comparator output (DM) will be low and UP count will occur. If not DOWN Count will take place. This process will continue till the reference signal and modulating signal voltages are equal. So DM signal is a series of 1 and 0.

DM signal is applied to a UP/DOWN input of the UP/DOWN counter at the receiver. This UP/DOWN counter is programmed for 1001 initial value (i.e. power on reset) and mode control is activated. So depend on the UP/DOWN input for the next clock pulse counter will count UP or DOWN. This output is applied to 4 Bit D/A converter. A logic circuit is added to the counter which keeps the output of the counter in between 0000 to 1111 always. Output of the D/A converter will be a staircase signal lies between 0 and +4.7V. This staircase signal is applied a low pass filter. This low pass will smoothen the staircase signal so that original AF signal will be recovered.

We can use a voltage amplifier at the output of the low pass filter to amplify the recovered AF signal to desired voltage level.

**PROCEDURE:**

**DM Modulator:**
1. Study the theory of operation
2. Connect the trainer (AET-73M)
3. Observe the output of AF generator using CRO; it should be a Sine wave of 100 Hz frequency with 3Vpp amplitude.
4. Verify the output of the DC source with multimeter/scope; output should vary 0 to +4V
5. Observe the output of the clock generator using Crotchety should be 4 KHz frequency of square wave with 5 Up amplitude.

**Note:** This clock signal is internally connected to the up/down counter so no external connection is required.

**DM With DC Voltage as modulating signal:**
6. Connect DC signal from the DC source to the inverting input of the comparator and set some voltage says 3V.
7. Observe and plot the signals at D/A converter output (i.e. non-inverting input of the comparator), DM signal using CRO and compare them with the waveforms given in figure.

8. Connect DM signal (from 73M) to the DM input of the demodulator.

9. Connect clock (4KHz) from modulator (73M) to the clock input of the demodulator (73D). Connect clock input of UP/DOWN counter (in 73D) to the clock from transmitter with the help of springs provided.

10. Observe digital output (LED indication) of the UP/DOWN counter (in 73 D) and compare it with the output of the UP/DOWN (in 73M) . By this you can notice that the both the outputs are same.

11. Observe and plot the output of the D/A converter and compare it with the waveforms given in figure.

12. Measure the demodulated signal (i.e. output of the D/A converter 73D with the help of multimeter and compare it with the original signal 73 M. From the above observation you can notice that both the voltages are equal and there is no loss in process of modulation, transmission and demodulation.

13. Similarly you can verify the DM operation for different values of modulating signal.
Fig 4.3 DM Waveforms for AC input signal
RESULT

Thus the Delta modulation and demodulation were performed and graphs were plotted.
**DIFFERENTIAL PULSE CODE MODULATION**

**AIM:**
To Study differential pulse code modulation & demodulation technique.

**EQUIPMENT REQUIRED:**
1. Differential pulse code modulation trainer kit (FALCON ADCL-07)
2. Connecting chords.
3. Power supply.
4. 20MHz Dual Trace Oscilloscope

**THEORY:**
DPCM is a good way to reduce the bit rate for voice transmission. However, it causes some other problems that deals with voice quality. DPCM quantizes and encodes the difference between a previous sample input signal and a sample input signal. DPCM quantizes the difference signal using uniform quantization. Uniform quantization generates an SNR that is small for small input sample signals and large for large input sample signals. Therefore, the voice quality is better at higher signals.

**CIRCUIT DESCRIPTION:**
**DPCM MODULATOR**

**Clock Generator**
The crystal oscillator generates a 2.048MHz clock. 1.024MHz clock is generated by dividing the 2.048MHz clock. 512KHz, 256KHz, 128KHz, and 64KHz clocks are generated using U(74HCT393) a 4-bit binary counter.

**Timing Logic**
This logic generates the various timing signals for the transmitter. The operation of ADC673 is controlled by two inputs: CONVERT and /DATA ENABLE. The transmitted clock is fed to a 4-bit binary counter(IC74LS393) whose output is ANDED using(IC74HC08). A pulse(plrst) is generated which is further fed to D flipflop to generate the CONVERT pulse and the /DATA ENABLE signal.
**Sine Wave Generator**

8 KHz frequency is fed to serial to parallel shift register (IC74HC164) which generates the sine wave, by serial shift operations. The serial to parallel shift register (IC74HC164) has resistive ladder network at the output. For 8 shifts of register, one staircase sine wave is generated. So if 8KHz clock is fed to the shift register, 500Hz sine wave is generated with amplitude variable from 0 to 4Vpp.

**Sample and Hold Logic**

This logic samples the information signal with the clock frequency of 16KHz, (IC4016) is used for sampling. It is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals.

**Analog to Digital Converter**

The analog to digital converter converts the analog samples to digital bits. This device performs both the quantizing and encoding operations. The analog to digital converter IC, AD673 forms the heart of this logic. The timing of the A/D conversion is controlled by the convert pulse, which is generated in the timing logics. As soon as the data is ready, the AD673 gives a data ready (DR active low) output. The data latch is used for latching the valid outputs of the A/D converter. The timing and latching interval of the data latch is controlled by the latch enable signal (74HCT374). Each sample is coded to a 8 bit data by AD673. These coded data is fed to a parallel to serial shift register, which gives a serial 8-bit quantized data.

**Quantising**

The signal level of the input signal assumed to vary from 0 volt to 4.96 volts. The entire level is dividing to 126 uniform steps. Each step corresponds to 4.96/128=40mv

The quantizing level is chosen to be the midway of the steps. If the signal level falls below the quantizing level, and then the signal level is rounded off to the upper level. This type of quantizing is called “uniform quantizing”, where the step levels are uniform. Then corresponding to the level chosen, code words are assigned to the samples. The code words vary from 0000000 to 1111111 for the 0 to 4.96V. Thus the analog to digital converter assigns the code
MODEL WAVEFORMS:

**Linear Predictor**

D flip-flops (74HCT74) are used as delay elements to give two bit delays in the quantized data. The two delayed data’s are ORED using (IC74HC32). The ORED data is fed to the integrator circuit, which is built around (ICTLO84)
**Comparator**

The comparator circuit is built around (ICLM311). This circuit compares the two inputs and the differenced output is fed to the quantizer.

**DPCM DEMODULATOR**

**Linear Predictor**

D flip-flops (74HCT74) are used as delay elements to give two bit delays. The received data and the delayed is ORED using (74HC32). The delay element is placed in feedback loop with the OR circuit.

**Integrator**

The integrator is built around (ICTL084). Integrator output is the integration of the input signal applied.

**Butterworth Filter**

The butterworth low pass filter is built around (ICTL084), which filters out the sampling frequency components from the demodulation output.

**PROCEDURE:**

1. Connect the circuit as per the block diagram and switch settings.
2. Connect power supply in proper polarity to the kit ADCL-07 and switch it ON.
3. Keep the clock frequency at 512KHz, by changing the jumper position of JP1 in the clock generator section.
4. Keep the amplitude of the onboard sine wave, of frequency 500Hz to 1Vpp.

**DPCM modulation:**

5. Connect the 500Hz sine wave to the IN post of analog buffer.
6. Connect OUT post of analog buffer to IN post of DPCM modulator section.
7. Observe the sample output at the given test point. The input signal is sampled at clock frequency of 16KHz.
8. Observe the linear predicted output at the PREDICTED OUT post of the linear predictor in the DPCM modulator section.
9. Observe the differential pulse code modulated data (DPCM) at the DPCM OUT post of DPCM modulator section.
10. Observe the DPCM data at DPCM OUT post by varying input signal from 0 to 2 volts

**DPCM demodulation:**
11. Connect the DPCM modulated data from the DPCM OUT post of the DPCM modulator to the IN post of the DPCM demodulator.

12. Observe the demodulated data at the output of summation block.

13. Observe the integrated demodulated data at the DEMOD OUT post of the DPCM demodulator.

14. Connect the demodulated data from the DEMOD OUT post of the DPCM demodulator to the IN post of low-pass filter.

15. Observe the reconstructed signal at the OUT post of the filter. Use RST switch for clear observation of the output.

16. Now, simultaneously reduce the clock frequencies from 512KHz to 256KHz, and 128KHz by changing the jumper position of JP1 and observe the difference in the DPCM modulated and demodulated data. As the frequency of clock decreases, DPCM demodulated data at DEMOD OUT becomes distorted.

17. Observe various waveforms for different frequencies.

**OBSERVATIONS:**

DPCM→At 64 KHZ

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DATA CLK</th>
<th>Sinusoidal output</th>
<th>Predicted output</th>
<th>DPCM output</th>
<th>Summation output</th>
<th>Demodulated output</th>
<th>Filter output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td></td>
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<td></td>
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<tr>
<td>Vpp</td>
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<tr>
<td>V amp</td>
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</tr>
</tbody>
</table>

**RESULT:**

Thus the differential pulse code modulation & demodulation process was done..
DATA FORMATTING

Aim:
To identify the various encoding schemes for a given data stream.

HARDWARE REQUIRED
1. Coding Kits.
2. CRO

THEORY:
‘1’ and ‘0’ can be represented in various formats in different levels and waveforms. The selection of coding technique depends on system band width, systems ability to pass dc level information, error checking facility.

Non return to Zero (level):
The NRZ(L) waveform simply goes low for one bit time to represent a data ‘0’ and high to represent data ‘1’. For lengthy data the clock is lost in asynchronous mode. The maximum rate at which NRZ can change is half the data clock.[when alternate 0’s and 1’s are there.

DC Level:
A length data will have only a dc level as its waveform, a dc voltage cannot be used in circuits which involve transformers like telephone, AC coupled amplifiers, capacitors, filter etc.

Manchester Biphase:
‘0’ is encoded low during first half of bit time & high for other half of bit & vice versa for ‘1’. There is no synchronization problem in the receiver. It is independent of DC levels, since there is a transition occurring in each bit. Its max frequency is equal to data clock rate. There is at least one transition per bit. Since there is midway transition, it makes clock regeneration difficult so we use special bi phase clock recovery circuit
**Return to Bias:**

It is a 3 level code it consist of positive, negative and zero. Easy clock synchronization is possible. '1' for positive, '0' for negative in first half and zero bias for second half. Maximum frequency is equal to data clock frequency. DC levels of waveforms depends on strings of 1's and 0's. Hence we cannot use AC coupled communication link. Timing information is easily obtained. The system is referred to as 'self clocking system', as magnitude of waveform is original data signal. It requires complex transmitters.

**PRELEB QUESTIONS**

1. Compare NRZ-I and NRZ-L.
2. What is the use of data formatting?
3. Compare NRZ and biphase encoding.
4. What is the relationship between quantization levels and number of bits in a code word?
5. Give the advantages of Manchester encoding.

**PROCEDURE**

1. Connect the data generator output to code generator kit. This gives the random binary sequence of the kit.
2. Connect the clock signal to the trainer kit.
3. Connect the output to the CRO channel along with the clock signal.
4. Observe the waveforms with respect to clock on a dual channel CRO, and compare with the model graph.
5. Plot the waveforms for different codes.

**RESULT**

Thus the different coding techniques were studied and observed for a given binary data, and their corresponding waveforms plotted.
BER COMPARISON OF DIFFERENT MODULATION SCHEMES IN AWGN CHANNEL IN MATLAB, SIMULINK

Aim
The main aim of this experiment is to perform the following objectives using communication toolbox in MATLAB and Simulink:

- **Part I**: To perform digital modulation/demodulation techniques and plot the signal constellation associated with a modulation process using communications toolbox.
- **Part III**: To generate BER data for analyzing communication systems (modulator-channel-demodulator) using BERTool.
- **Part I**: To perform simulations for digital modulation/demodulation techniques using Simulink.

### Part I
**Simulations of digital Modems using communications toolbox**

#### Representing Digital Signals

To modulate a signal using digital modulation with an alphabet having Msymbols, start with a real message signal whose values are integers from 0 to M-1. Represent the signal by listing its values in a vector, \( x \). Alternatively, you can use a matrix to represent a multichannel signal, where each column of the matrix represents one channel. For example, if the modulation uses an alphabet with eight symbols, then the vector \( [2 \ 3 \ 7 \ 1 \ 0 \ 5 \ 5 \ 2 \ 6] \)' is a valid single-channel input to the modulator. As a multichannel example, the two-column matrix

\[
\begin{bmatrix}
2 & 3 \\
3 & 3 \\
7 & 3 \\
0 & 3 \\
\end{bmatrix}
\]

defines a two-channel signal in which the second channel has a constant value of 3.

#### Digital Modulation and Demodulation (m files, communications toolbox)

This section contains examples that illustrate how to use the digital modulation and demodulation functions.

To plot the signal constellation associated with a modulation process, follow these steps:

1. If the alphabet size for the modulation process is M, then create the signal \([0:M-1]\). This signal represents all possible inputs to the modulator.
2. Use the appropriate modulation function to modulate this signal. If desired, scale the output. The result is the set of all points of the signal constellation.
Example (1): Computing the Symbol Error Rate

The example generates a random digital signal, modulates it, and adds noise. Then it creates a scatter plot, demodulates the noisy signal, and computes the symbol error rate.

\[ M = 16; \] % Alphabet size
\[ x = \text{randi}([0 \ M-1],5000,1); \] % Create a random digital message
\[ \text{hMod} = \text{modem.qammod}(M); \] % Use 16-QAM modulation.
\[ \text{hDemod} = \text{modem.qamdemod}(	ext{hMod}); \]

\[ \text{scatterPlot} = \text{commscope.ScatterPlot}('\text{SamplesPerSymbol}',1,'\text{Constellation}',\text{hMod.Constellation}); \]

\[ \text{scatterPlot}.\text{PlotSettings.Constellation} = \text{'on'}; \] % Modulate
\[ y = \text{modulate}(	ext{hMod},x); \] % Transmit signal through an AWGN channel.
\[ \text{ynoisy} = \text{awgn}(y,15,\text{'measured'}); \]
\[ \text{update}(	ext{scatterPlot},\text{ynoisy}); \] % Create scatter plot from noisy data.
\[ z = \text{demodulate}(	ext{hDemod},\text{ynoisy}); \] % Demodulate ynoisy to recover the message.
\[ \text{[num,rt]} = \text{symerr}(x,z); \] % Check symbol error rate.
To generate BER data for analyzing communication systems using BERTool

BERTool is an interactive GUI for analyzing communication systems’ bit error rate (BER) performance. Using BERTool you can

- Generate BER data for a communication system using
  - Closed-form expressions for theoretical BER performance of selected types of communication systems.
  - Calculating BER using semi-analytical technique.
  - Simulations contained in MATLAB simulation functions or Simulink models. After you create a function or model that simulates the system, BERTool iterates over your choice of Eb/N0 values and collects the results.

- Plot one or more BER data sets on a single set of axes. For example, you can graphically compare simulation data with theoretical results or simulation data from a series of similar models of a communication system.

- Fit a curve to a set of simulation data.

- Send BER data to the MATLAB workspace or to a file for any further processing you might want to perform.

There are three different methods by which BERTool can generate BER data. They are

- Theoretical
- Semianalytic
- Monte Carlo
Computing Theoretical BER

You can use BERTool to generate and analyze theoretical BER data. Theoretical data is useful for comparison with your simulation results. However, closed-form BER expressions exist only for certain kinds of communication systems. To access the capabilities of BERTool related to theoretical BER data, use the following procedure:

1. Open BERTool, and go to the Theoretical tab.

![Theoretical BER Tool interface](image)

   - **Channel type:** AWGN
   - **Modulation type:** PSK
   - **Modulation order:** 2
   - **Channel Coding:** None
   - **Synchronization:** Perfect synchronization

2. Set the parameters to reflect the system whose performance you want to analyze. Some parameters are visible and active only when other parameters have specific values. See “Available Sets of Theoretical BER Data” on page 5-11 for details.
Example 2: Using the Theoretical Tab in BERTool

This example illustrates how to use BERTool to generate and plot theoretical BER data. In particular, the example compares the performance of a communication system that uses an AWGN channel and QAM modulation of different orders.

Running the Theoretical Example

1. Open BERTool, and go to the Theoretical tab.

2. Set the parameters as shown in the following figure.

3. Click Plot.

4. Change the Modulation order parameter to 16, and click Plot. BERTool creates another entry in the data viewer and plots the new data in the same BER Figure window.

5. Change the Modulation order parameter to 64, and click Plot. BERTool creates another entry in the data viewer and plots the new data in the same BER Figure window.

6. To recall which value of Modulation order corresponds to a given curve, click the curve. BERTool responds by adjusting the parameters in the Theoretical tab to reflect the values that correspond to that curve.
To remove the last curve from the plot (but not from the data viewer), clear the check box in the last entry of the data viewer in the **Plot** column. To restore the curve to the plot, select the check box again.

### Performance Results via the Semianalytic Technique

To access the semi analytic capabilities of BER Tool, open the **Semi analytic** tab.

![Image of BER Tool interface](image)

**Example 3: Procedure for Using the Semianalytic Tab in BER Tool**

The procedure below describes how you typically implement the Semi analytic technique using BERTool:

- **E/N0 range:** 0:18 dB
- **Channel type:** AWGN
- **Modulation type:** PSK
- **Modulation order:** 2
- **Differential encoding:** Off
- **Samples per symbol:** 16
- **Transmitted signal:** `reedpuls(reedmaccrandint(10, 1, 2, 0.573), 2, 13)`
- **Received signal:** `reedpuls(reedmaccrandint(15, 1, 2, 0.973), 2, 13)`
- **Receiver filter coefficients:**
  - **Numerator:** `ones(16, 1)/16`
  - **Denominator:** `1`

Click the **Plot** button to generate the plot.
1. Generate a message signal containing at least ML symbols, where M is the alphabet size of the modulation and L is the length of the impulse response of the channel in symbols. A common approach is to start with an augmented binary pseudonoise (PN) sequence of total length \((\log_2 M)M\). An augmented PN sequence is a PN sequence with an extra zero appended, which makes the distribution of ones and zeros equal.

2. Modulate a carrier with the message signal using baseband modulation. Shape the resultant signal with rectangular pulse shaping, using the oversampling factor that you will later use to filter the modulated signal. Store the result of this step as txsig for later use.

3. Filter the modulated signal with a transmit filter. This filter is often a square-root raised cosine filter, but you can also use a Butterworth, Bessel, Chebyshev type 1 or 2, elliptic, or more general FIR or IIR filter. If you use a square-root raised cosine filter, use it on the nonoversampled modulated signal and specify the oversampling factor in the filtering function. If you use another filter type, you can apply it to the rectangularly pulse shaped signal.

4. Run the filtered signal through a noiseless channel. This channel can include multipath fading effects, phase shifts, amplifier nonlinearities, quantization, and additional filtering, but it must not include noise. Store the result of this step as rxsig for later use.

5. On the **Semianalytic** tab of BERTool, enter parameters as in the table below.

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eb/No range</td>
<td>A vector that lists the value of Eb/No for which you want to collect BER data. The value in this field can be a MATLAB expression or the name of a variable in the MATLAB workspace.</td>
</tr>
<tr>
<td>Modulation type</td>
<td>These parameters describe the modulation scheme you used earlier in this procedure.</td>
</tr>
<tr>
<td>Modulation order</td>
<td></td>
</tr>
<tr>
<td>Differential encoding</td>
<td>This check box, which is visible and active for MSK and PSK modulation, enables you to choose between differential and nondifferential encoding.</td>
</tr>
<tr>
<td>Samples per symbol</td>
<td>The number of samples per symbol in the transmitted signal. This value is also the sampling rate of the transmitted and received signals in Hz.</td>
</tr>
<tr>
<td>Transmitted signal</td>
<td>The txsig signal that you generated earlier in this procedure.</td>
</tr>
<tr>
<td>Received signal</td>
<td>The rxsig signal that you generated earlier in this procedure.</td>
</tr>
<tr>
<td>Numerator</td>
<td>Coefficients of the receiver filter that BERTool applies to the received signal.</td>
</tr>
<tr>
<td>Denominator</td>
<td></td>
</tr>
</tbody>
</table>

6. Click Plot.

**Example 4: Using the Semianalytic Tab in BERTool**
This example illustrates how BERTool applies the semianalytic technique, using 16-QAM modulation.

Running the Semianalytic Example

1. To set up the transmitted and received signals run the following commands:

   ```
   % Step 1. Generate message signal of length >= M^L.
   M = 16; % Alphabet size of modulation
   L = 1; % Length of impulse response of channel
   msg = [0:M-1 0]; % M-ary message sequence of length > M^L
   % Step 2. Modulate the message signal using baseband modulation.
   modsig = qammod(msg,M); % Use 16-QAM.
   Nsamp = 16;
   modsig = rectpulse(modsig,Nsamp); % Use rectangular pulse shaping.
   % Step 3. Apply a transmit filter.
   txsig = modsig; % No filter in this example
   % Step 4. Run txsig through a noiseless channel.
   rxsig = txsig*exp(1i*pi/180); % Static phase offset of 1 degree
   ```

2. Open BERTool and go to the Semianalytic tab.

3. Set parameters as shown in the following figure.

4. Click Plot.
III F) Running MATLAB Simulations

You can use BERTool in conjunction with your own MATLAB simulation functions to generate and analyze BER data. The MATLAB function simulates the communication system whose performance you want to study. BERTool invokes the simulation for Eb/N0 values that you specify, collects the BER data from the simulation, and creates a plot. BERTool also enables you to easily change the Eb/N0 range and stopping criteria for the simulation.

Example: Using a MATLAB Simulation with BERTool

This example illustrates how BERTool can run a MATLAB simulation function. The function is viterbisim, one of the demonstration files included with Communications Toolbox software. To run this example, follow these steps:

1. Open BERTool and go to the Monte Carlo tab.
2. Set parameters as shown in the following figure.

<table>
<thead>
<tr>
<th>Theoretical</th>
<th>Semi Analytic</th>
<th>Monte Carlo</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eb/N0 range: 0.5 dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Simulation M-file or model: viterbisim.m

BER variable name: |

Simulation limits:

- Number of errors: 100 |
- Number of bits: 1e8 |

3. Click Run.

BERTool runs the simulation function once for each specified value of Eb/N0 and gathers BER data. (While BERTool is busy with this task, it cannot process certain other tasks, including plotting data from the other tabs of the GUI.) Then BERTool creates a listing in the data viewer. BERTool plots the data in the BER Figure window.
4 To change the range of Eb/N0 while reducing the number of bits processed in each case, type \([5 5.2 5.3]\) in the \textbf{Eb/No range} field, type \(1e5\) in the \textbf{Number of bits} field, and click \textbf{Run}. BERTool runs the simulation function again for each new value of Eb/N0 and gathers new BER data. Then BERTool creates another listing in the data viewer.

BERTool plots the data in the BER Figure window, adjusting the horizontal axis to accommodate the new data.

The two points corresponding to 5 dB from the two data sets are different because the smaller value of \textbf{Number of bits} in the second simulation caused the simulation to end before observing many errors.
Part III
Simulink BER calculations

This example starts from a Simulink model originally created as an example in the Communications Blockset Getting Started documentation, and shows how to tailor the model for use with BERTool. The example also illustrates how to compare the BER performance of a Simulink simulation with theoretical BER results.

To prepare the model for use with BERTool, follow these steps, using the exact case-sensitive variable names as shown:

**III.Q1. (demo)**

1. Open the model by entering the following command in the MATLAB Command Window.
   
   ```matlab
doc_bpsk
   ```

2. To initialize parameters in the MATLAB workspace and avoid using undefined variables as block parameters, enter the following command in the MATLAB Command Window:
   ```matlab
   EbNo = 0; maxNumErrs = 100; maxNumBits = 1e8;
   ```

3. To ensure that BERTool uses the correct amount of noise each time it runs the simulation, open the dialog box for the AWGN Channel block by double-clicking the block. Set **Es/No** to **EbNo** and click **OK**. In this particular model, **Es/N0** is equivalent to **Eb/N0** because the modulation type is BPSK.

4. To ensure that BERTool uses the correct stopping criteria for each iteration, open the dialog box for the Error Rate Calculation block. Set **Target number of errors** to **maxNumErrs**, set **Maximum number of symbols** to **maxNumBits**, and click **OK**.

5. To enable BERTool to access the BER results that the Error Rate Calculation block computes, insert a Signal to Workspace block in the model and connect it to the output of the Error Rate Calculation block.
To configure the newly added Signal to Workspace block, open its dialog box. Set **Variable name** to BER, set **Limit data points to last** to 1, and click **OK**.

(Optional) To make the simulation run faster, especially at high values of Eb/N0, open the dialog box for the Bernoulli Binary Generator block. Select **Frame-based outputs** and set **Samples per frame** to 1000.

Save the model in a folder on your MATLAB path using the file name bertool_bpskdoc.mdl.

Open BERTool and go to the **Monte Carlo** tab.

Set parameters on the **Monte Carlo** tab as shown in the following figure.
Click Run.
To compare these simulation results with theoretical results, go to the Theoretical tab in BERTool and set parameters as shown below.

<table>
<thead>
<tr>
<th>Theoretical</th>
<th>Semi-analytic</th>
<th>Monte Carlo</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_b/N_0$ range:</td>
<td>$nR$</td>
<td>$nR$</td>
</tr>
</tbody>
</table>

Channel type: AWGN

Modulation type: PSK
Modulation order: 2

Denodulation type: Coherent

Differential encoding

Channel Coding:
- None
- Convolutional
- Block

Synchronization:
- BERTool synchronization

Normalized timing error: 0
RMS phase noise (rad): 0

Click Plot.

BERTool plots the theoretical curve in the BER Figure window along with the earlier simulation results.
Repeat III.Q1 for the following models.

III. Q2. Describe the modulation/demodulation and receiver of system, PLOT performance curve.

RESULT:

BER comparison of different modulation schemes in AWGN channel using MATLAB, Simulink were done.