(Declared u/s 3 of UGC Act, 1956)

Department of
Electronics and Communication Engineering

Subject Code: **BEC3L1**

Subject Name: **Electron Devices and Circuits lab**

Name : ……

Reg No : ……

Branch : ……

Year & Semester : ……

LIST OF EXPERIMENTS

INDEX

Expt. No.	Expt. Date	Name of the Experiment	Marks	Staff Signature

Ex.No:1 COMMON EMITTER TRANSISTOR CHARACTERISTICS

Date:

AIM:

To determine the characteristics of BJT under Common Emitter configuration.

APPARATUS REQUIRED:

S.No.	Apparatus required	Range	Quantity
1.	RPS	(0-30)V	2
2.	Voltmeter	(0-1)V	2
3.	Ammeter	(0-500)μA	2
4.	Resistance	1KΩ	1
5.	Transistor	BC 107	1
6.	Bread board		2
7.	Connecting wires		As required

FORMULA USED:

(1) Input impedance hie $= \Delta V_{BE} / \Delta I_B$, with V_{CE} as constant

(2) Output Admittance $h_{oe} = \Delta I_c / \Delta V_{CE}$, with I_B as constant

(3) Forward Current gain $h_{fe} = \Delta I_c / \Delta I_B$, with V_{CE} as constant

(4) Reverse voltage gain $h_{re} = \Delta V_{BE} / \Delta V_{CE}$, with I_B as constant

THEORY:

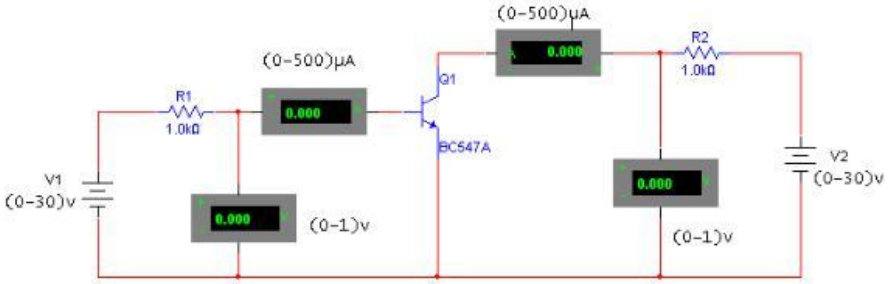
This is also called grounded emitter configuration. Base is the input terminal, collector is the out put terminal and emitter is the common terminal.

OPERATION:

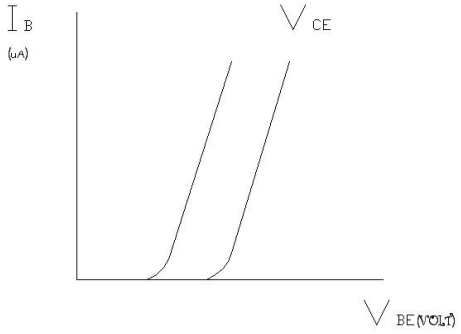
Input characteristics:

The collector to emitter voltage is kept constant at zero volt and base current increased from zero in equal steps by increasing V_{BE}. This procedure is repeated for higher fixed values of V_{CE} and curves of I_B Vs V_{BE} are drawn. When $V_{CE} = 0$, the emitter base junction is forward biased and the junction behaves as a

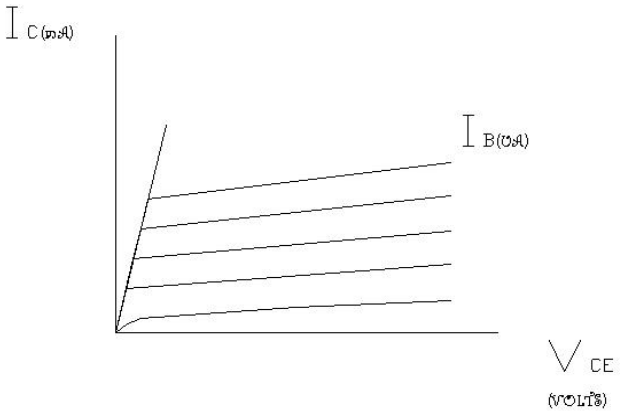
CIRCUIT DIAGRAM FOR COMMON EMITTER CONFIGURATION:



INPUT CHARACTERISTICS



OUTPUT CHARACTERISTICS



OUTPUT CHARACTERISTICS

I_B = µA		I_B = µA		I_B = µA	
V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)

MODEL CALCULATION:

forward biased diode. When V_{CE} increased, the width of the depletion region at the reverse biased collector base junction will increase. Hence the effective width of the base will decrease.

Output characteristics:

The base current I_B is kept constant at a suitable value by adjusting base emitter voltage V_{BE}. The magnitude of collector emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting V_{CE} . Now the curves of I_C versus V_{CE} are plotted for different constant values of I_B.

Saturation region:

Both junctions are forward biased and an increase in the base current does not cause a corresponding large change in I_C. The ratio of V_{CE} (sat) to I_C in this region is called saturation resistance.

Cut off region:

Both junctions are reverse biased. When the operating point for the transistor enters the cut off region, the transistor is OFF. The transistor is virtually an open circuit between collector and emitter.

Active region:

Emitter base junction is forward biased and the collector base junction is reverse biased. If the transistor is to be used as a linear amplifier, it should be operated in the active region.

PROCEDURE:

Input characteristics:

1. Keeping the voltage across collector to emitter (V_{CE}) as constant, tabulate the values of base current for various values of base emitter voltage (V_{BE}.).
2. Repeat the same procedure for various values of $V_{CE.}$

Output characteristics:

1. Keeping the base current as constant, tabulate the values of collector current (I_C) for various values of collector emitter voltage (V_{CE}).
2. Repeat the same procedure for various constant values of base current (I_B).

RESULT:

DISCUSSION QUESTIONS:

1. What are the types of breakdown occurs in transistors?

Avalanche multiplication or avalanche breakdown .Reach through

of punch through

2. Why do we prefer silicon for transistor?

Silicon is an indirect band semiconductor the life time of charge carriers is more and hence amplification is more.

3. What is meant by stabilization?

The maintenance of the operating point is fixed stable.

4. What is the need for biasing?

To maintain proper zero signal emitter base voltage.To maintain proper zero signal collector emitter voltage. To maintain proper zero signal collector current.

5. What is meant by operating point?

The zero signal values of I_C and V_{CC} are known as operating point. It is also called so because the variations of I_C and V_{CC} take place about this point when signal is applied. It is also called as Q point and it is the point was the transistor is silent.

6. What types of components are used for temperature stabilization?

Passive type of components are used

7. What are the types of biasing?

Fixed bias

Collector feedback bias

Self bias or emitter bias

8. Define stability factor?

Stability factor S defined as the rate of change of collector current IC w.r.t reverse saturation current Iα keeping β and V_{BE} constant.

$$S= \Delta I_C / \Delta I\alpha$$

9. What is Q point?

The quiescent operating point is given by the inter section of the bias curve and the dc load line.

10. What is bias? What is the need for biasing?

The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as transistor biasing.When a transistor is biased properly, it works efficiently and produces no distortion in the output signal and thus operating point can be maintained stable.

Ex.No:2 **FET CHARACTERISTICS**

Date:

AIM:

To draw the drain and transfer characteristics and determine the transconductance, drain resistance and amplification factor of the given FET.

APPARATUS REQUIRED:

Sl.No.	Apparatus	Range	Quantity
1.	RPS	(0-30)V	2
2.	Resistor	1KΩ	1
		1.5 KΩ	1
3.	Voltmeter	(0-10)V	1
		(0-30)V	1
4.	FET	BFW10	1
5.	Ammeter	(0-10)mA	1
6.	Bread board	-	As required
7.	Connecting wires		As required

FORMULA USED:

Drain Resistance R_d = $\Delta V_{DS} / \Delta I_{D,}$ V_{GS} as constant

Amplification factor $\mu = g_m r_d$

Transconductance $g_m = \Delta I_D / \Delta V_{GS}$, V_{DS} as constant

THEORY:

FET is a three terminal device which current is controlled an electrified. The operation of FET depends only on the majority carriers.

OPERATION:

When V_{GG} applied $V_{DD} = 0$

The P-type gate and N-type channel constitute PN junction is always reverse biased in FET operation. The reverse bias is applied by a battery voltage, V_{GG} connected between the gate and the source terminal. When PN junction is reverse biased, the electrons and holes diffuse across the junction and leave behind the positive ions on N side and negative ions on P side. The region containing immobile ions is known as **Depletion region.** Both regions are heavily doped, then the depletion region symmetrically on both sides.

When no V_{DD} is applied the depletion region is a symmetrical and the conductivity's zero, since there are no mobile carriers in the junction. As the reverse bias voltage across the junction is increased, thickness of the depletion region also increases.

When V_{DD} applied V_{GG} =0

When no voltage is applied to gate i.e V_{GG}=0 and V_{DD} is applied between source and drain. The electron will flow from source to drain through the channel.

When V_{DD} applied V_{GG} is applied

When voltage is applied between the drain and source with a battery V_{DD}, the electrons flow from source to drain through the narrow channel existing between the depletion regions.

TRANSFER CHARACTERISTICS:

The curves shows the relationship between drain current (I_D) and gate to source voltage (V_{GS}) for different values of drain source (V_{DS}) voltage. First adjust the drain to source voltage to some suitable value. Then increase the gate to source voltage in small suitable value at each step and record the corresponding values of drain current at each step. If V_{GS} continuously increasing, the channel width reduced when V_{GS} =V_P, the pinch off occurs thus I_D =0.

DRAIN CHARACTERISTICS:

It shows the relation between the drain to source voltage (V_{DS}) and drain current ($_{ID)}$.

Active Region:

In this region the for a small increase in drain to source voltage the drain current increases largely. Hence this is called active region.

Cut off region:

In this region the current never increases even if voltage increases.

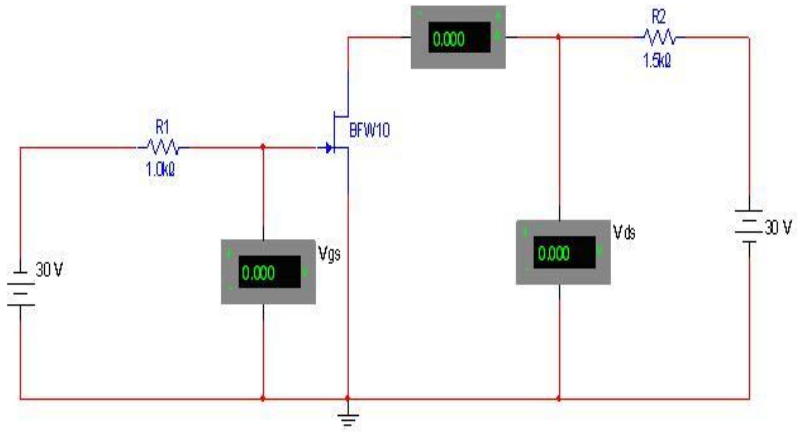
Hence it is called cutoff region.

Saturation region:

In this region after increasing from active region, the drain current remains constant over a range of drain to source voltage. After that current

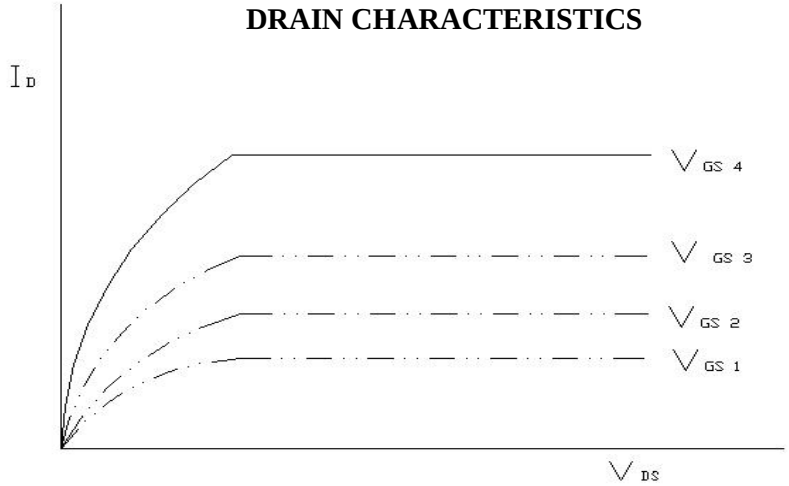
pinches off or shoots to a very high value. The drain to source voltage at which it occurs is called as pinch off Voltage.

CIRCUIT DIAGRAM FOR FET:

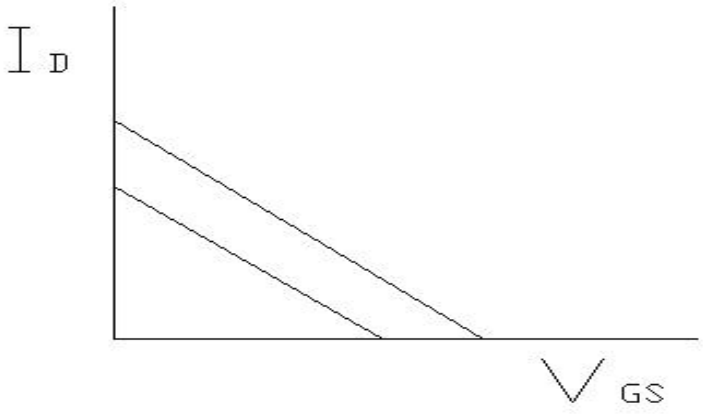


MODEL GRAPH FOR FET:

DRAIN CHARACTERISTICS



TRANSFER CHARACTERISTICS



TABULATION FOR FET:

DRAIN CHARACTERISTICS

V_{GS}= V		V_{GS} = V		V_{GS} = V	
V_{DS}(v)	I_D(mA)	V_{DS}(v)	I_D(mA)	V_{DS}(v)	I_D(mA)

TRANSFER CHARACTERISTICS

V_{DS} = V		V_{DS} = V		V_{DS} = V	
V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)

MODEL CALCULATION:

PROCEDURE:

1. The connections are given as shown in circuit diagram.
2. By varying RPS1 V_{GS} is kept constant.
3. Now V_{DS} is varied and corresponding variation in drain current I_D is tabulated.
4. This process is repeated for another value of V_{GS}(V_{GS} is set at -1 V and -2Volts)
5. Plot these values on graph with V_{GS} on x axis and I_D on Y axis. This gives the drain characteristics.
6. By varying RPS2, it is kept at constant value. Say V_{DS} = 2V.
7. Now for various values of VGS, drain current is taken(I_D).This is repeated for Another value of V_{DS}.
8. Plot these values on graph sheet with V_{GS} on X axis and I_D on Y axis. This gives us Transfer characteristics.
9. The various parameters are found as given in formula used.

RESULT:

DISCUSSION QUESTIONS:

1. What is a FET?

A field effect (FET) is a three terminal semiconductor device in which current conduction takes place by one type of carriers (either holes or electron) and is controlled by an electric field.

2. Why FET is called an unipolar device?

The operation of FET depends upon the flow of majority carriers only (either holes or electrons) the FET is said to be unipolar device.

3. Define pinch off voltage?

It is the voltage at which the channel is pinched off, i.e. all the free charge from the channel get removed.

4. Define drain resistance?

Drain resistance (r_d) is defined as the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in drain current (ΔI_d) at constant gate to source voltage (V_{gs}). $r_d = \Delta V_{ds} / \Delta I_d$ at constant gate to source voltage (V_{gs})

5. Write down the relationship between various FET parameters?

Amplification factor = drain resistance * Transconductance

$$\mu = r_d * g_m$$

6. Mention the application of FET?

Used as a low noise amplifier

Used as a buffer amplifier

Used as phase shift oscillator

7. Why the input impedance of FET is more than that of a BJT?

The input impedance of FET is more than that of a BJT because the input circuit of FET is reverse biased whereas the input circuit of BJT is forward biased.

8. What is meant by gate source threshold voltage of a FET?

The voltage at which the channel is completely cur off and the drain current becomes zero is called as gate source threshold voltage.

9. Why N channel FET's are preferred over P channel FET's?

In N channel FET the charge carriere are the electrons which have a mobility o9f about 1300 cm^2/ VS, whereas in P channel FET's the charge carriers are the holes which have a mobility of about 500 cm^2 /VS. the current in a semiconductor is directly proportional to mobility. Therefore the current in N channel FET is more than that of P channel FET.

Ex.No:3 **UJT CHARACTERISTICS**

Date:

AIM:

To determine the static characteristics of UJT.

APPARATUS REQUIRED:

S.No.	Apparatus	Range	Quantity
1.	RPS	(0-30)V	2
2.	Voltmeter	(0-10)V	2
3.	Ammeter	(0-100)mA	1
4.	Resistance	1KΩ	1
		1.5KΩ	1
5.	UJT	2N2646	1
6.	Connecting wires		As required
7.	Read Board		As required

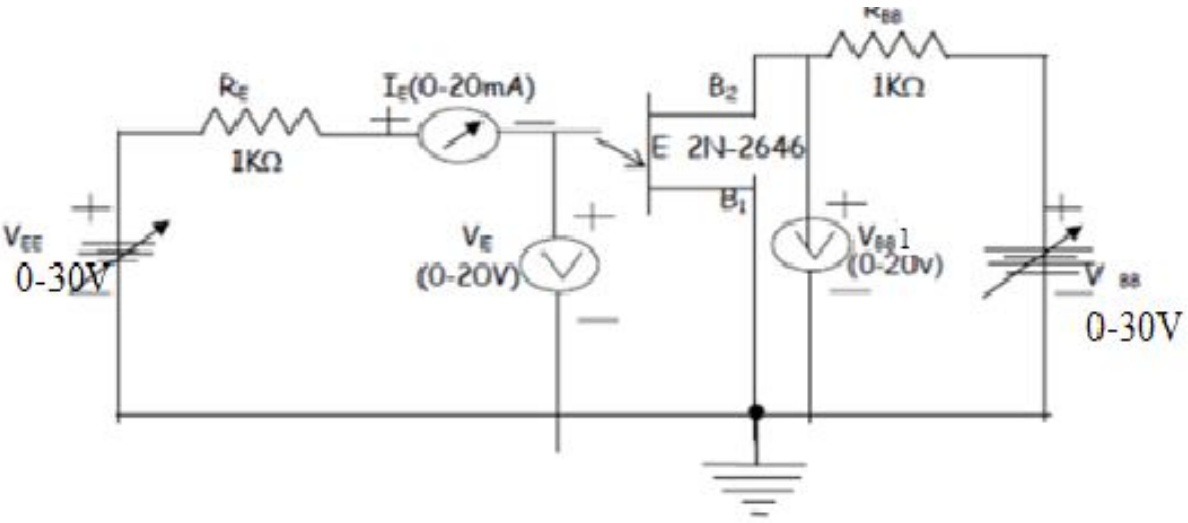
FORMULA USED:

1. Negative Resistance $= \Delta V_{BE} / \Delta I_E \ / \ V_{B1B2}$
2. Intrinsic Stand off ratio $= V_P - V_{BE} / V_{B1B2}$

THEORY:

The Uni Junction Transistor is a three terminal device. It has three terminals. Emitter, Base1 and base2. It consists of N type semiconductor bar into which P-Type semi conductor material is diffused. Contacts are then made into the device. The fig.1 shows the equivalent circuit of a n UJT.

CIRCUIT DIAGRAM FOR UJT:



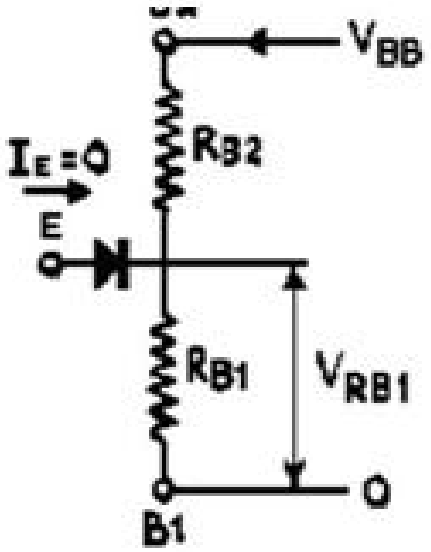
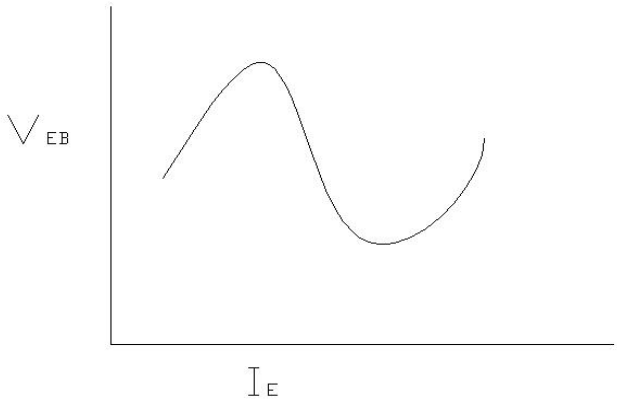


Fig.1.Equivalent circuit of UJT

UJT CHARACTERISTICS:



OPERATION

From the characteristics of UJT up to the peak point, the diode is reverse biased, and hence to the left of the peak point is known as cut off voltage. The voltage corresponding to this point is peak voltage. In the cut off region PN junction is reverse biased. The device does not conduct, only a small amount of current flows through the device. Once peak point is reached the device starts conducting. UJT has negative resistance characteristics. The device conducts up to one point which is called valley point. After the valley point the device passes to a saturation region. In this region the device voltage and current reach standard values.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. The voltage V_{B1B2} is kept as constant.
3. Varying the RPS1 the voltmeter readings of V_{EB1} and ammeter I_E readings are note down.
4. The above process is repeated for different values of V_{B1B2} readings.
5. At one point the needle deflects back and current starts increasing.
6. The current must not increase beyond 25mA.
7. The graph betweenV_{EB1} and I_E are plotted.

TABULATION FOR UJT:

V_{B2B1} =		V_{B2B1} =	
$V_{EB(V)}$	$I_{E(A)}$	$V_{EB(V)}$	$I_{E(A)}$

MODEL CALCULATION:

RESULT:

DISCUSSION QUESTIONS:

1. What does UJT stand for? Justify the name UJT.

UJT stands for uni junction transistor. The UJT is a three terminal semiconductor device having two doped regions. It has one emitter terminal and two base terminals. It has only one junction, moreover from the outlook; it resembles to a transistor hence the name uni junction transistor.

2. What is "interbase resistance" of UJT?

The resistance between the two bases of UJT is called interbase resistance. Its typical value ranges from 5kΩ to 10kΩ with emitter open.

Interbase resistance, $R_{bb} = R_{b1}+R_{b2}$

Where

R_{b1}= resistance of silicon bar between B_1 and emitter function

R_{b2} = resistance of silicon bar between B_2 and emitter function

3. What is meant by negative resistance region of UJT?

In a UJT the emitter voltage reaches the peak point voltage (Vp), emitter current starts flowing. After the peak point any effort to increase in emitter voltage (Ve) further leads to sudden increase in the emitter current with corresponding decrease in Ve, exhibition negative resistance. This takes place until the valley point is reached. The region between the peak point and valley point is called "negative resistance region".

4. How does UJT differ from a FET?

The gate junction of FET is reversed biased whereas in UJT the emitter junction is forward biased. BJT can amplify signals, whereas UJT has no ability to amplify signals.

5. What are the difference between UJT and BJT?

UJT	**BJT**
It has only one PN junction	It has two PN junction
Three terminals are labeled as emitter(E), base(B1)& base2(B2)	Three terminals are labeled as emitter(E),base(B)& collector(C)
It has no ability to amplify signals	It can amplify signals

6. Mention the application of UJT?

Used in timing circuits.

Used in switching circuits.

Used in phase control circuits

Used in trigger device for SCR and TRIAC Used for pulse generation

7. What sis source follower?

CD configuration of UJT is called as source follower because the output is taken from the source terminal of JFET. Since the output voltage closely follows the input voltage hence it is named as source follower.

Ex.No:4 SCR CHARACTERISTICS

Date:

AIM:

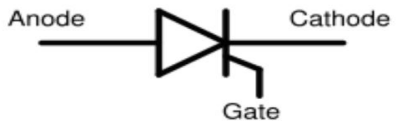
To obtain the forward and reverse characteristics of SCR and measure the holding and latching current.

APPARATUS REQUIRED:

Apparatus	Range	Type	Quantity
SCR	-	TYN616	1
RPS	(0-30V)		2
Voltmeter	(0-10V)	MC	1
Ammeter	(0-50mA)	MC	1
Resistor	10KΩ /1A 1KΩ		1 1

THEORY:

An SCR is a three terminal device. The three terminals are anode, cathode, and gate. When the anode is more positive with respect to the cathode, junctions j1,j3 are forward biased and the junctions j2 is reverse biased. Only a small leakage current



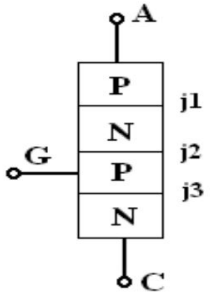


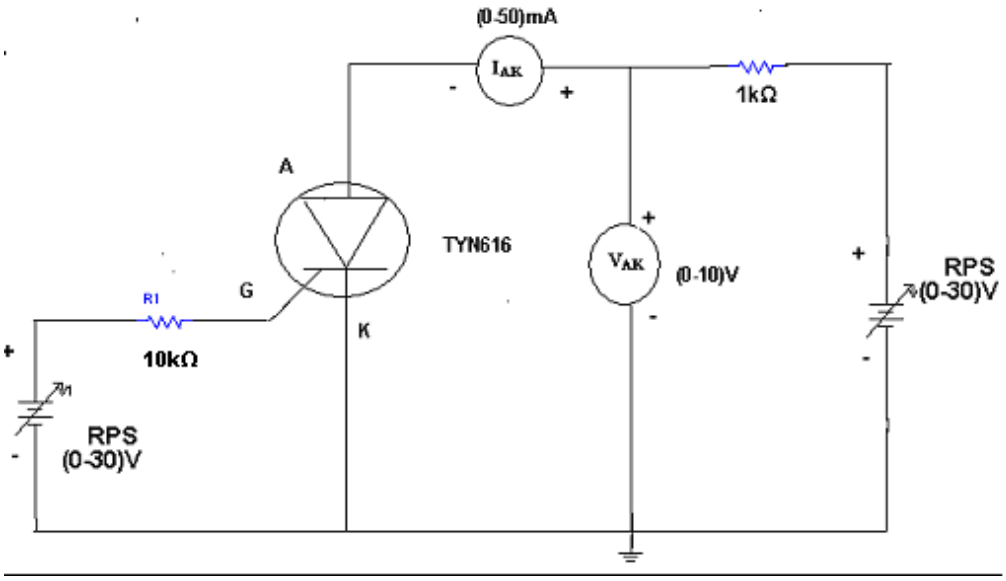
Fig.1. Schematic Symbol **Fig.2. Block Construction**

Flows through the device. The device is said to be in the **forward blocking state or off state**. when the anode to cathode voltage is increased to break over value, the junction j2 breaks down and device starts conducting (ON state) the anode current must be more than the value known as latching current in order to maintain the device in the ON state. Once SCR starts conducting, it behaves like a conducting diode and gate has no control over the device. The device can be turned off only by bringing the device in below a value known as holding current. The forward voltage drop across the device in the ON state is around one volt. When the cathode voltage is made positive with respect to the anode voltage junction j2 is forward biased and the junction j1 and j3 are reversed biased. The device will be in the reverse blocking state and only small leakage current flows through the device. The device can be turned on at forward voltage less than break over voltage by applying suitable gate current.

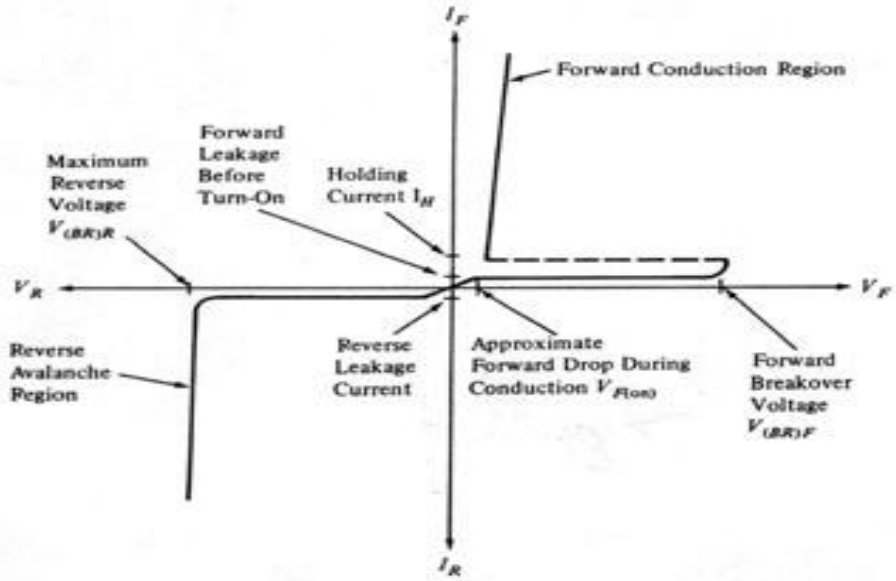
PROCEDURE:

1. The connections are made as per the circuit diagram
2. RPS is adjusted to the required gate current flows through the device.
3. The V_{AK} is increased in steps by varying the RPS and each step, the corresponding anode current noted down.
4. Reading corresponding to Break over point, latching current, holding current and also noted down.
5. To determine latching current:
6. The forward voltage is increased to break over value, gradually. The device gets tureen ON. At this condition, the gate current is removed. If the anode current is less than the latching current, the SCR will go into OFF state immediately. The circuit resistance is repeated until the device remains in ON stat even after removing the gate current. This current is latching current.
7. To determine Holding current:
8. The gate current is removed after bringing the device into the ON state. The circuit resistance is increased in steps. The minimum value of anode current at which the SCR remains in the ON state is the holding current.

Circuit Diagram:



MODEL GRAPH FOR SCR:



V–I characteristics of the SCR with gate open.

TABULATION FOR SCR:

I_G = mA		I_G = mA		I_G = mA	
V_{AK}(V)	I_A(mA)	V_{AK}(V)	I_A(mA)	V_{AK}(V)	I_A(mA)

MODEL CALCULATION:

RESULT:

DISCUSSION QUESTIONS:

1. Define break over voltage of SCR?

Break over voltage is defined as the minimum forward voltage at which the SCR starts conducting heavily.

2. List the advantages of SCR?

SCR can handle and control large currents. Switching speed is very high.It has no moving parts, therefore it gives noiseless operation. Operating efficiency is high.

3. List the applications of SCR?

Used as speed controlled in DC and AC motors.

Used as a inverter

Used as an converter

Used in battery chargers

Used for phase control and heater control

Used in light dimming control circuits

4. What is meant by latching?

The ability of SCR to remain conducting even when the gate signal is removed is called latching.

5. Define forward current rating of a SCR?

Forward current rating oaf a SCR is the maximum anode current that it can handle without destruction.

6. List the important ratings of SCR?

Forward break over voltage

Holding current

Gate trigger current

Average forward current

Reverse breakdown voltage

7. Define latch current and holding current?

Latch current: the maximum anode current that an SCR is capable passing without destruction.

Holding current: the minimum value of anode current required to keep the SCR is a position.

8. Define reverse break down voltage (V_{BR})?

The reverse voltage (anode – negative and cathode- positive) above which the reverse breakdown occurs, breaking J_1 and J_3 junctions. When the SCR is reverse biased, the thickness of the J_2 depletion layer during the forward bias condition is greater than the total thickness of the two depletion layers at J_1 and J_3. Therefore the forward breakdown voltage V_{BO} is greater than the reverse break over voltage V_{BR}.

9. Define forward break over voltage?

Forward break over voltage is the voltage above which the SCR enters the conduction region (ON state). The forward breakdown voltage is dependent on the gate bias.

10. What are the losses o occurs in a thyristor during working conditions?

1. Forward conduction loss.
2. Loss due of leakage current during forward and reverse blocking
3. Switching losses at turn-on and turn-off
4. Gate triggering loss.

Ex No:5 **POWER SUPPLY**
Date:

Objective

- To study the function and operation of regulated power supply.

Equipment required

- Multimeter
- Dual DC variable regulated Power supply (0-30) Volts

Theory

A **power supply** is a device that supplies electric power to an electrical load. The term is most commonly applied to electric power converters that convert one form of electrical energy to another, though it may also refer to devices that convert another form of energy (mechanical, chemical, solar) to electrical energy. A regulated power supply is one that controls the output voltage or current to a specific value; the controlled value is held nearly constant despite variations in either load current or the voltage supplied by the power supply's energy source.

A power supply may be implemented as a discrete, stand-alone device or as an integral device that is hardwired to its load. Examples of the latter case include the low voltage DC power supplies that are part of desktop computers and consumer electronics devices.

Commonly specified power supply attributes include:

- The amount of voltage and current it can supply to its load.
- How stable its output voltage or current is under varying line and load conditions.

POWER SUPPLIES TYPES

- Battery
- DC power supply
- AC power supply
- Linear regulated power supply
- Switched mode power supply
- Programmable power supply
- Uninterruptible power supply
- High voltage power supply
- Voltage multipliers

DC POWER SUPPLY

SPECIFICATION

1. Adjustable 0~30V/0~2A
2. The design is limit the voltage overload
   The power supply input **220V, 230V, 240V AC**
3. Output voltage: 0-30V DC
4. Work temperature: -10^{o}C-40^{o}C

MAIN FUNCTION

1. Output constant current adjustable.
2. Output constant voltage adjustable.
3. LCD voltage and current display.
4. Constant voltage and current operation in individual.
5. Over current protection.

Adjustable power supply

RESULT:

Thus the Function and operation of Regulated Power supply was studied.

Ex No. 6(a) Frequency Response of Common Emitter Amplifiers With Self

Date: Bias, Fixed Bias and Collector to Base Feedback Bias

Aim:

To study the frequency response of Common Emitter Amplifier and calculate its self bias, Fixed bias and collector to base feedback bias

APPARATUS REQUIRED:

Apparatus	Range	Type	Quantity
Transistor	-	BC107	1
RPS	(0-30V)	Dual	1
Resistor	3MΩ,5.1KΩ	-	1,1
Capacitor	1μF	-	1
Function Generator	(0-10)MHz	single	1
Connecting wires	-	-	-

Design

Choose $\beta = 250$, $V_{CC} = 12V$, $I_C = 1$ mA

By applying KVL to output side,

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CC} = I_C R_C - V_{CE}$

Assume equal drops across R_C and V_{CE}

$V_{RC} = V_{CE} = 6V$, $I_C R_C = 6V$

$R_C = 6V/10^{-3} = 6K\Omega$

Choosing a standard value for R_C as 5.1Ω

By applying KVL to the input side,

$V_{CC} - I_B R_B - V_{BE} = 0$

$I_B = I_C/\beta = 1mA/250 = 4\mu A$

$RB = (V_{CC} - V_{BE}) / I_B$

$= (12 - 0.7)/4x10^{-6}$

$= 2.825M\ \Omega$

$\approx 3M\ \Omega$

Design of input capacitor

$F = 1/2\pi h_{ie}C$

Take $F = 100Hz$ and $h_{ie} = 1.6\ K\Omega$

$C1 = 1/ (2\pi \times 1.6\ K\Omega \times 100) = 0.9\mu F \approx 1\mu F$

Calculation

Bandwidth = $f_H - f_L$

Procedure:

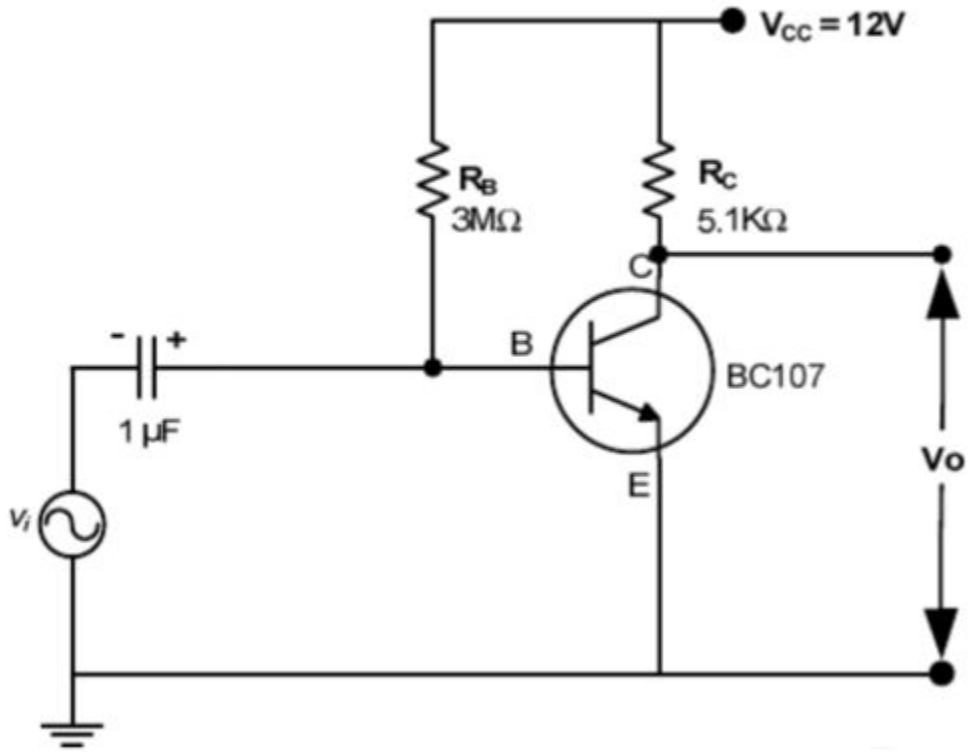
1) Connect the circuit as per the circuit diagram
2) Set Vin = 50mV in the signal generator. Keeping input voltage constant, vary the frequency from 1Hz to 1MHzin regular steps.
3) Note down the corresponding output voltage.
4) Plot the graph: Gain in dB Vs Frequency in Hz.
5) Calculate the Bandwidth from the Frequency response graph

To plot the Frequency Response

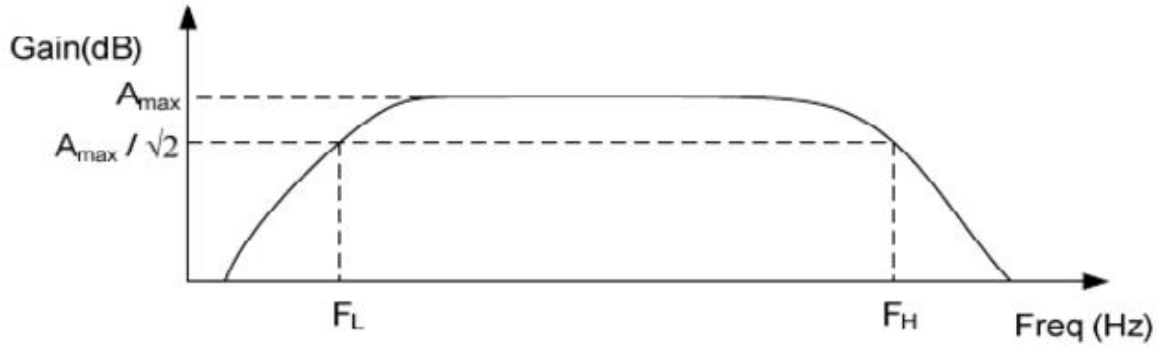
1) The frequency response curve is plotted on a semi-log scale.
2) The mid frequency voltage gain is divided by $\sqrt{2}$ and these points are marked in the frequency response curve.
3) The high frequency point is called the upper 3dB point.
4) The lower frequency point is called the lower 3dB point.
5) The difference between the upper 3dB point and the lower 3dB point in the frequency scale gives the bandwidth of the amplifier.
6) From the plotted graph the bandwidth is obtained. (i.e) Bandwidth = $f_H - f_L$

Circuit Diagram

CE Amplifier with Fixed Bias



Model Graph



TABULATION:

Frequency(Hz)	Vo(V)	Gain=Vo/Vs	Gain=20log(Vo/Vs)dB

MODEL CALCULATION:

Result

Thus a BJT Common Emitter Amplifiewith fixed bias is designed and implemented and the frequency response curve is plotted.

The bandwidth is found to be _____

Ex No.6(b) Frequency Response of Common Collector Amplifiers With Self Bias, Fixed Bias and Collector To Base Feedback Bias

Date:

Aim: To design and construct common Base amplifier using voltage divider(self-biad)

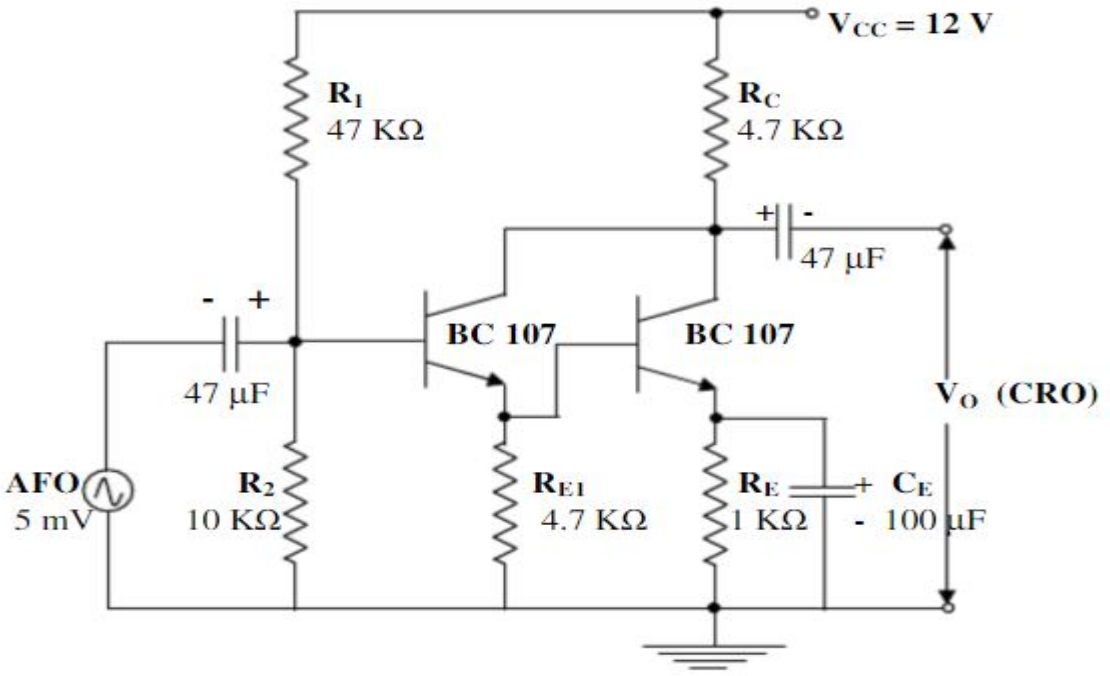
Apparatus Required:

Apparatus	Range	Type	quantity
RPS	(0-30V)	-	1
Transistor		BC107	1
AFO	(0-10)MHz	single	1
CRO	(0-20)MHz	Dual	1
Resistor	1KΩ,10KΩ,4.7KΩ, 47KΩ	-	1,1,2,1
Capacitor	47µF,100 µF	-	2,1

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set V_S = 5 mV using AFO.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph gain Vs frequency.
5. Calculate bandwidth from the graph.

Circuit diagram:

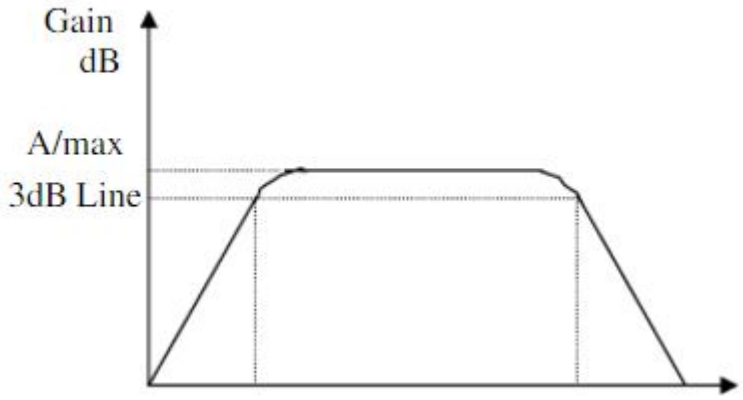


TABULATION:

Frequency(Hz)	Vo(V)	Gain=Vo/Vs	Gain=20log(Vo/Vs)dB

MODEL CALCULATION:

Model graph (frequency response)



RESULT:

Thus a Common Collector amplifier was designed and implemented and frequency response curve plotted.

Ex no.7 SOURCE FOLLOWER WITH BOOTSTRAPPED GATE RESISTANCE
Date:

AIM:

To construct a source follower with bootstrapped gate resistance amplifier and plot its frequency response characteristics.

APPARATUS REQUIRED:

S.No.	Name	Range	Quantity
1.	Transistor	BC107	2
2.	Resistor	1kΩ,11 kΩ,1M kΩ	1,1,1
3.	Regulated power supply	(0-30)V	1
4.	Signal Generator	(0-3)MHz	1
5.	CRO	30 MHz	1
6.	Bread Board		1
7.	Capacitor	0.01μF	2

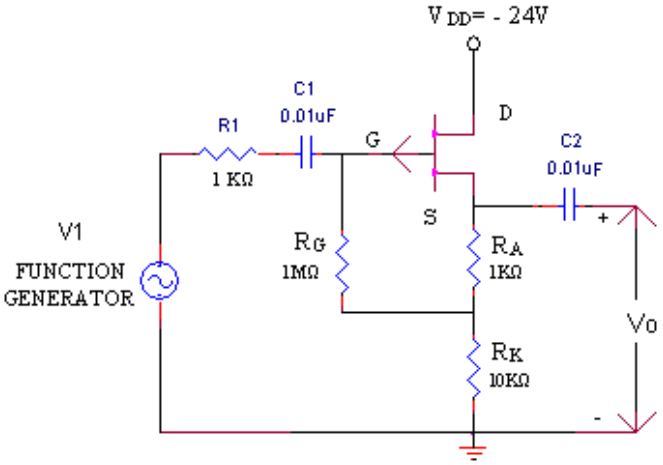
THEORY:

Source follower is similar to the emitter follower(the output source voltage follow the gate input voltage),the circuit has a voltage gain of less than unity, no phase reversal, high input impedance, low output impedance. Here the Bootstrapping is used to increase the input resistance by connecting a resistance in between gate and source terminals. The resister R_A is required to develop the necessary bias for the gate.

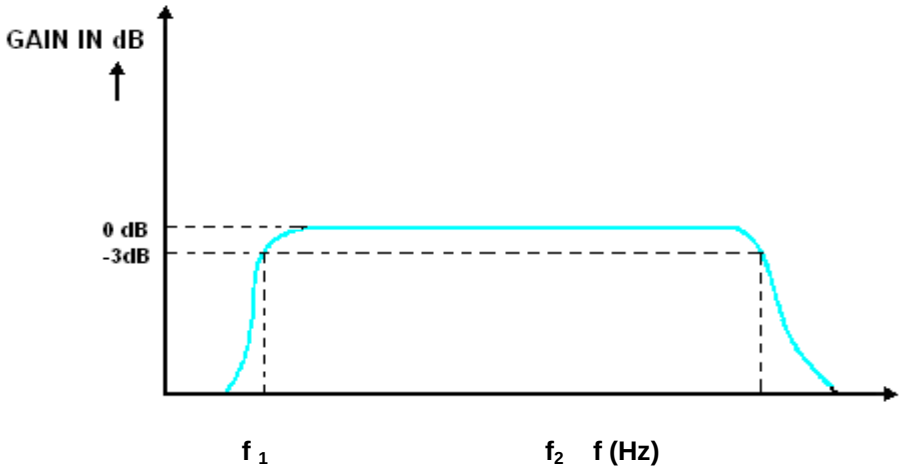
PROCEDURE:

1. Connections are made as per the circuit diagram.
2. The waveforms at the input and output are observed for cascode operations by varying the input frequency.
3. The biasing resistances needed to locate the Q-point are determined.
4. Set the input voltage as 1V and by varying the frequency, note the output voltage.
5. Calculate gain=20 log (V_o / $V_{in.}$)
6. A graph is plotted between frequency and gain.

CIRCUIT DIAGRAM



MODEL GRAPH



TABULATION:
Keep the input voltage constant (V_{in}) =

Frequency (in Hz)	**Output Voltage (in volts)**	**Gain = 20 log (V_o / V_{in}) (in dB)**

MODEL CALCULATION:

RESULT:

Thus, the Source follower with Bootstrapped gate resistance was constructed and the gain was determined.

Ex no.8(a) **CLASS - A POWER AMPLIFIER**
Date:

AIM:

To construct a Class A power amplifier and observe the waveform and to compute maximum output power and efficiency.

APPARATUS REQUIRED:

S.No.	Name	Range	Quantity
1.	Transistor	CL100, BC558	1,1
2.	Resistor	47kΩ,33Ω,220Ω,	2,1
3.	Capacitor	47 µF	2
4.	Signal Generator	(0-3)MHz	1
5.	CRO	30MHz	1
6.	Regulated power supply	(0-30)V	1
7.	Bread Board		1

FORMULA

Maximum power transfer $=P_o,max=V_o^2/R_L$
Effeciency,$\eta = P_{o,max}/P_c$

THEORY:

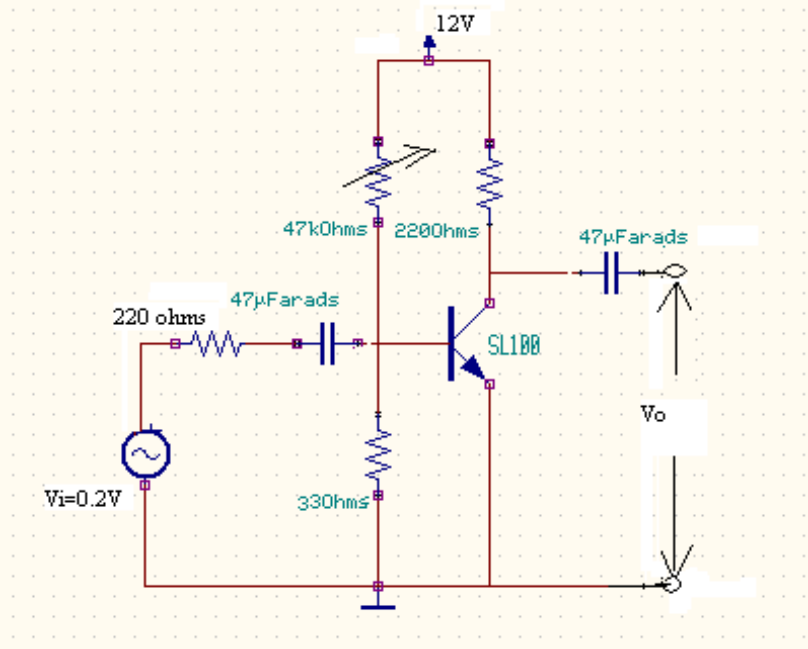
The power amplifier is said to be Class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input signal cycle.

For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally.The collector current flows for 360^0 (full cycle) of the input signal. i e the angle of the collector current flow is 360^0.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mv, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 10 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) vs Frequency(Hz).

CIRCUIT DIAGRAM



TABULATION:

Keep the input voltage constant, Vin =

Frequency (in Hz)	Output Voltage (in volts)	Gain= 20 log(Vo/Vin) (in dB)

MODEL CALCULATION:

RESULT:

Thus the Class A power amplifier was constructed. The following parameters were calculated:

a) Maximum output power=

` b) Efficiency=

Ex no. 8(b) **CLASS B COMPLEMENTARY SYMMETRY POWER AMPLIFIER**
Date:

AIM:

To construct a Class B complementary symmetry power amplifier and observe the waveforms with and without cross-over distortion and to compute maximum output power and efficiency.

APPARATUS REQUIRED:

S.No.	Name	Range	Quantity
1.	Transistor	CL100, BC558	1,1
2.	Resistor	4.7kΩ,15kΩ	2,1
3.	Capacitor	100µF	2
4.	Diode	IN4007	2
5.	Signal Generator	(0-3)MHz	1
6.	CRO	30MHz	1
7.	Regulated power supply	(0-30)V	1
8.	Bread Board		1

CIRCUIT DIAGRAM

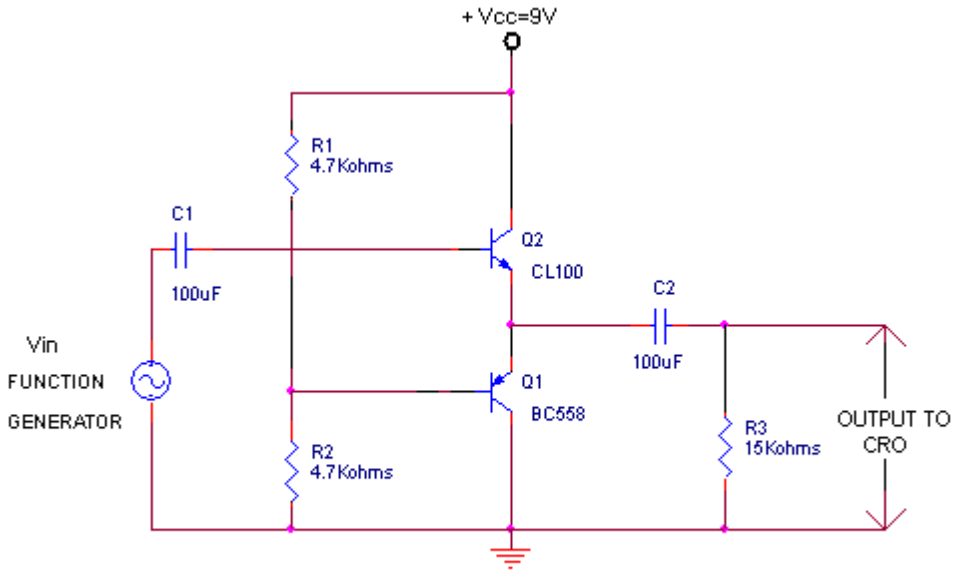


FIG.6.1

FORMULA:

Input power, $P_{in}=2V_{cc}I_m/\Pi$

Output power, $P_{out}=V_mI_m/2$

Power Gain or efficiency, $\eta=л/4(V_m/V_{cc})$ 100

THEORY:

A power amplifier is said to be Class B amplifier if the Q-point and the input signal are selected such that the output signal is obtained only for one half cycle for a full input cycle. The Q-point is selected on the X-axis. Hence, the transistor remains in the active region only for the positive half of the input signal.

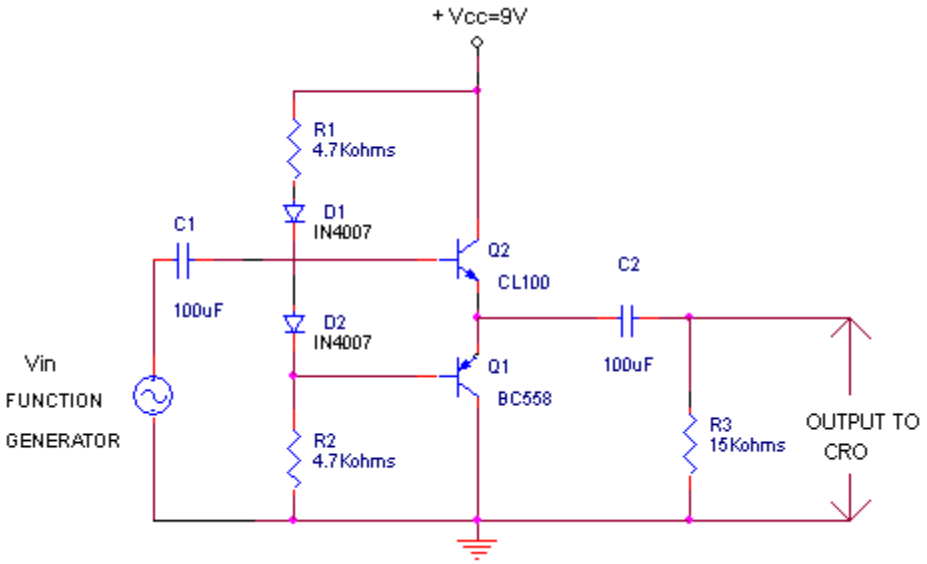
There are two types of Class B power amplifiers: Push Pull amplifier and complementary symmetry amplifier. In the complementary symmetry amplifier, one n-p-n and another p-n-p transistor is used. The matched pair of transistor are used in the common collector configuration. In the positive half cycle of the input signal, the n-p-n transistor is driven into active region and starts conducting and in negative half cycle, the p-n-p transistor is driven into conduction. However there is a period between the crossing of the half cycles of the input signals, for which none of the transistor is active and output, is zero.

PROCEDURE:

1. Connections are given as per the circuit diagram without diodes.
2. Observe the waveforms and note the amplitude and time period of the input signal and distorted waveforms.
3. Connections are made with diodes.
4. Observe the waveforms and note the amplitude and time period of the input signal and output signal.
5. Draw the waveforms for the readings.
6. Calculate the maximum output power and efficiency.

Hence the nature of the output signal gets distorted and no longer remains the same as the input. This distortion is called cross-over distortion. Due to this distortion, each transistor conducts for less than half cycle rather than the complete half cycle. To overcome this distortion, we add 2 diodes to provide a fixed bias and eliminate cross-over distortion.

CIRCUIT DIAGRAM



OBSERVATION

OUTPUT SIGNAL

AMPLITUDE :

TIME PERIOD :

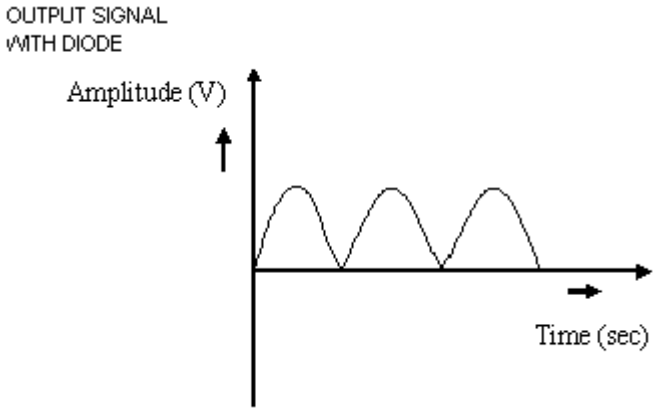
CALCULATION

POWER, P_{IN} = $2V_{CC}\ I_m/л$

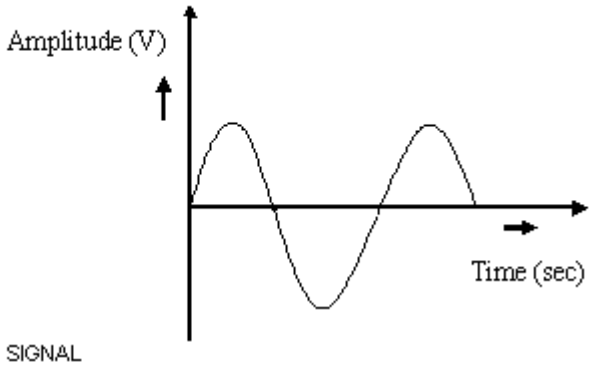
OUTPUT POWER, P_{OUT} = $V_m I_m/2$

EFFICIENCY, η = $(л/4)(V_m/ V_{CC}) \times 100$

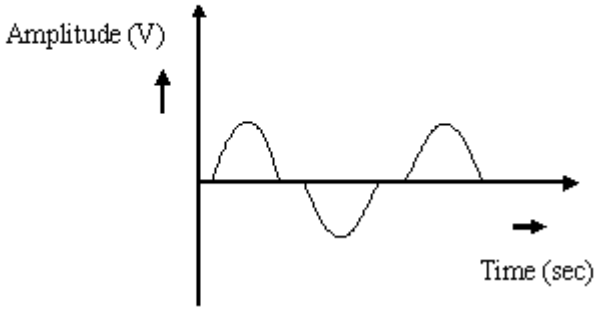
MODEL GRAPH



INPUT SIGNAL



OUTPUT SIGNAL WITHOUT DIODE



RESULT:

Thus the Class B complementary symmetry power amplifier was constructed to observe cross-over distortion and the circuit was modified to avoid the distortion. The following parameters were calculated:

a)Maximum output power=

b)Efficiency=

Ex No.9 **DIFFERENTIAL AMPLIFIER, CMRR MEASUREMENT**

Date:

Aim: To construct a differential amplifier using BJT and to determine the dc collector current of individual transistors and also to calculate the CMRR.

APPARATUS REQUIRED:

S.No.	Name	Range	Quantity
1.	Transistor	BC107	2
2.	Resistor	4.7kΩ, 10kΩ	2,1
3.	Regulated power supply	(0-30)V	1
4.	Function Generator	(0-3) MHz	2
5.	CRO	30 MHz	1
6.	Bread Board		1

THEORY:

The differential amplifier is a basic stage of an integrated operational amplifier. It is used to amplify the difference between 2 signals. It has excellent stability, high versatility and immunity to noise. In a practical differential amplifier, the output depends not only upon the difference of the 2 signals but also depends upon the common mode signal.

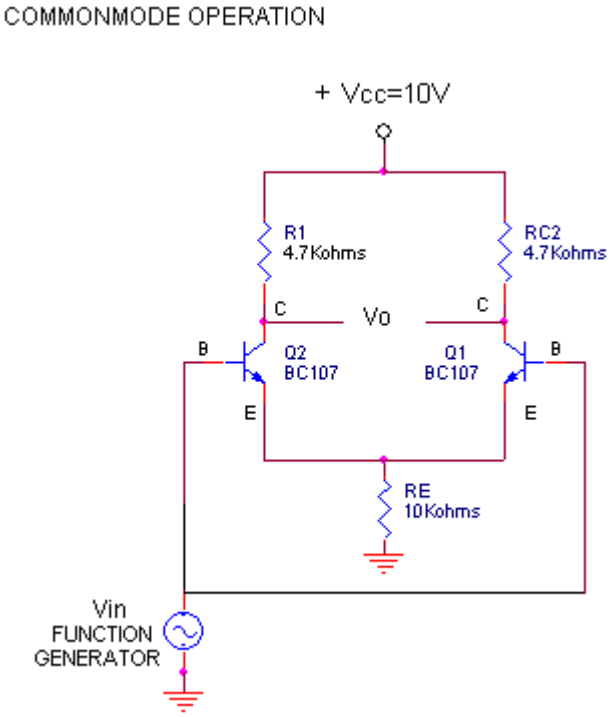
Transistor Q1 and Q2 have matched characteristics. The values of R_{C1} and R_{C2} are equal. R_{e1} and R_{e2} are also equal and this differential amplifier is called emitter coupled differential amplifier. The output is taken between the two output terminals.

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. To determine the common mode gain, we set input signal with voltage V_{in}=2V and determine V_o at the collector terminals. Calculate common mode gain, $A_c=V_o/V_{in}$.
3. To determine the differential mode gain, we set input signals with voltages V_1 and V_2. Compute $V_{in}=V_1-V_2$ and find V_o at the collector terminals. Calculate differential mode gain, $A_d=V_o/V_{in}$.

4. Calculate the CMRR=A_d/A_c.
5. Measure the dc collector current for the individual transistors.

CIRCUIT DIAGRAM



OBSERVATION

$$\mathbf{V_{IN} = V_O = A_C = V_O / V_{IN}}$$

FORMULA:

Common mode Gain $(A_c) = V_O / V_{IN}$

Differential mode Gain $(A_d) = V_0 / V_{IN}$

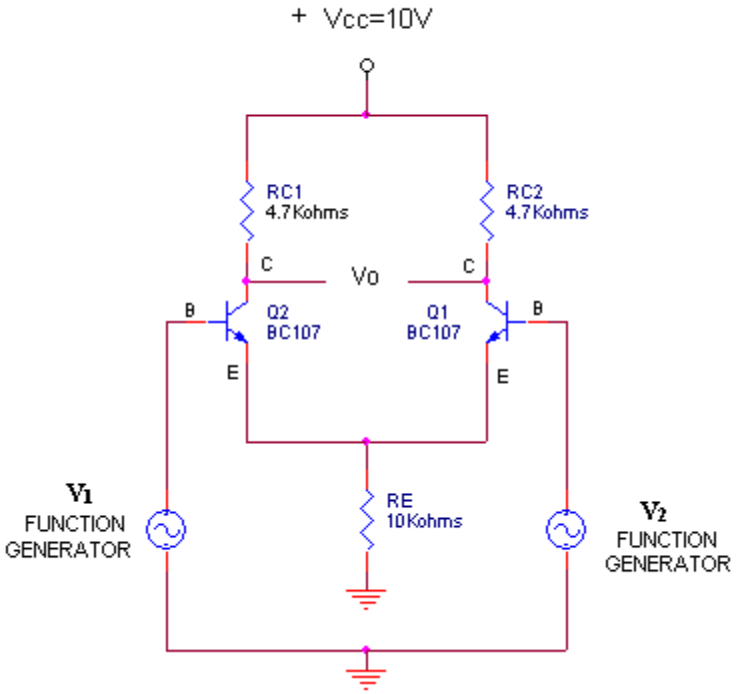
Where $V_{IN} = V_1 - V_2$

Common Mode Rejection Ratio (CMRR) = A_d/A_c

Where, A_d is the differential mode gain

A_c is the common mode gain.

DIFFERENTIOL MODE OPERATION



OBSERVATION

$$\mathbf{V_{IN} = V_1 - V_2}$$

$$\mathbf{V_0 =}$$

$$\mathbf{A_d = V_0 / V_{IN}}$$

For the differential mode operation the input is taken from two different sources and the common mode operation the applied signals are taken from the same source

Common Mode Rejection Ratio (CMRR) is an important parameter of the differential amplifier. CMRR is defined as the ratio of the differential mode gain, A_d to the common mode gain, A_c.

$$CMRR = A_d / A_c$$

In ideal cases, the value of CMRR is very high.

RESULT:

Thus, the Differential amplifier was constructed and dc collector current for the individual transistors is determined. The CMRR is calculated as…….

Ex No.10 Spice Simulation of Common Emitter and Common Source Amplifiers

Date:

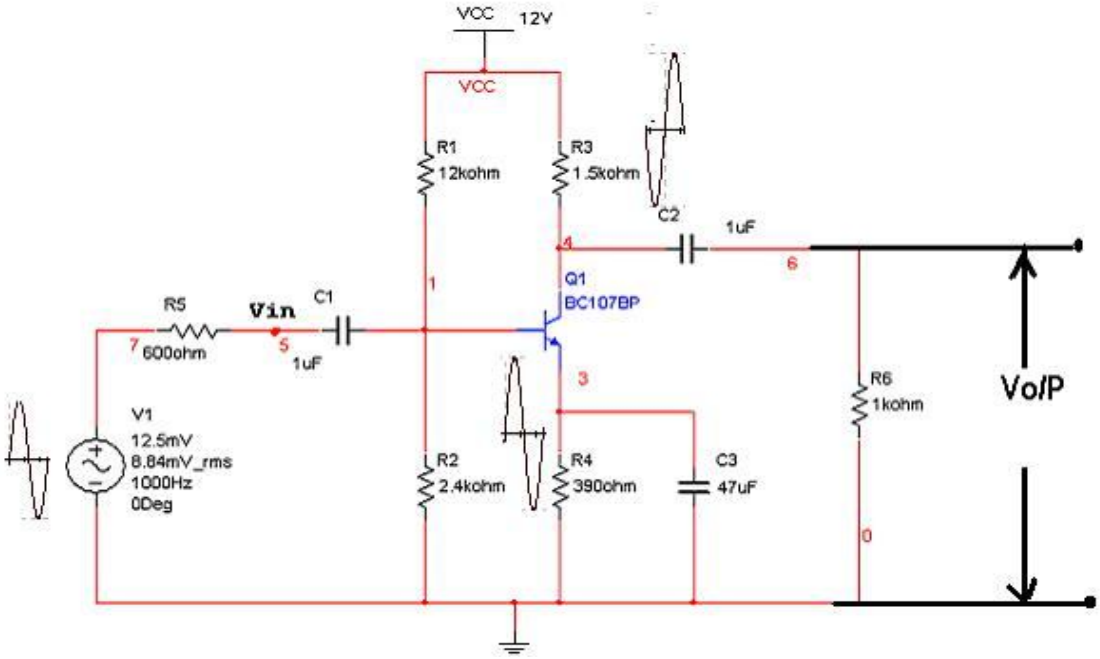
AIM :

To design and simulate the frequency response of common emitter amplifier for a gain of 50.

APPARATUS REQUIRED:

PC with SPICE software

CIRCUIT DIAGRAM :



THEORY:

The CE amplifier provides high gain and wide frequency response. The emitter lead is common to both the input and output circuits are grounded. The emitter base junction is at forward biased .The collector current is controlled by the base current rather than the emitter current. The input signal is applied to the base terminal of the transistor and amplified output taken across collector terminal. A very small change in base current produces a much larger change in collector

current. When the positive is fed to input circuit it opposes forward bias of the circuit which cause the collector current to decrease, it decreases the more negative. Thus when input cycle varies through a negative half cycle, increases the forward bias of the circuit, which causes the collector current increases .Thus the output signal in CE is out of phase with the input signal.

PROCEDURE

1. Select different components and place them in the grid.
2. For calculating the voltage gain the input voltage of 25mv (p-p) amplitude and 1KHz frequency is applied, then the circuit is simulated and output voltage is noted.
3. The voltage gain is calculated by using the expression

$$Av = Vo/Vi$$

4. For plotting frequency response, the input voltage is kept constant at 25mv(p-p) and frequency is varied.
5. Note down the output voltage for each frequency.
6. All readings are tabulated and Av in db is calculated using the formula

$$20 \text{ Log } Vo/Vi.$$

7. A graph is drawn by taking frequency on X-axis and gain in dB on Y-axis on a Semi log graph sheet.

SPICE FILE :

```
VIN 1 4 SIN(0 1.5V
2KHZ) VB 4 0 2.3V
RL 3 0 15K
V1 2 0 15V
Q1 2 1 3 MOD1
.MODEL MOD1 NPN
.TRAN 0.02MS 0.78MS
.PROBE
.END
```

$$r'_e = \frac{25mV}{I_E} = \frac{25}{3.3} = 7.575\Omega$$

$$r_L = \frac{R_C \times R_L}{R_C + R_L} = \frac{1500 \times 1000}{1500 + 1000} = 600\Omega$$

$$A_V = \frac{r_L}{r'_e} = \frac{600}{7.575} = 79.20$$

$$Z_{in(base)} = \beta r'_e = 40 \times 7.575 = 303\Omega$$

$$Z_{in} = Z_{in(base)} \parallel R_1 \parallel R_2 = 303 \parallel 12000 \parallel 2400 = 263\Omega$$

$$V_b = \frac{Z_{in}}{R_G + Z_{in}} \times 25mV = \frac{263}{600 + 263} = 7.61mV$$

$$V_{out} = A_V \times V_b = 79.20 \times 7.61mV = 0.603V$$

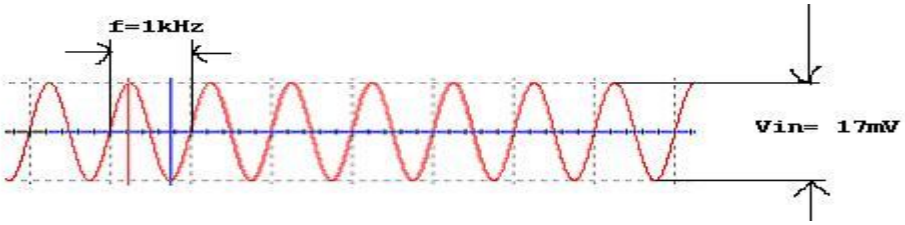
PRACTICAL CALCULATIONS :

$$V_{in} =$$

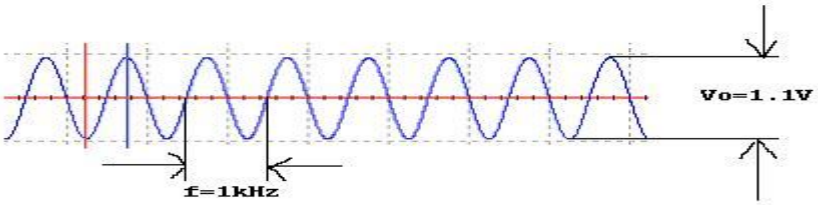
$$V_{out} =$$

$$A_V = \frac{V_{out}}{V_{in}} =$$

INPUT WAVE FORM :



OUT PUT WAVE FORM :



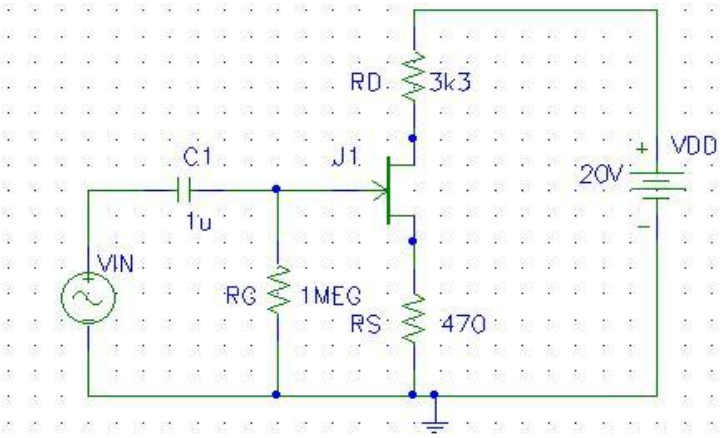
AIM:

To find the DC response of CS amplifier.

APPARATUS REQUIRED:

PC with SPICE software

CIRCUIT DIAGRAM:



THEORY:

In electronics, a **common-source** amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit. The analogous bipolar junction transistor circuit is the common- emitter amplifier.

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier. (See classification of amplifiers). As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance

according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics. The CS–CG combination is called a cascode amplifier.

PROCEDURE:

1.Measure the DC operating point of each transistor and compare your results with the calculated values.

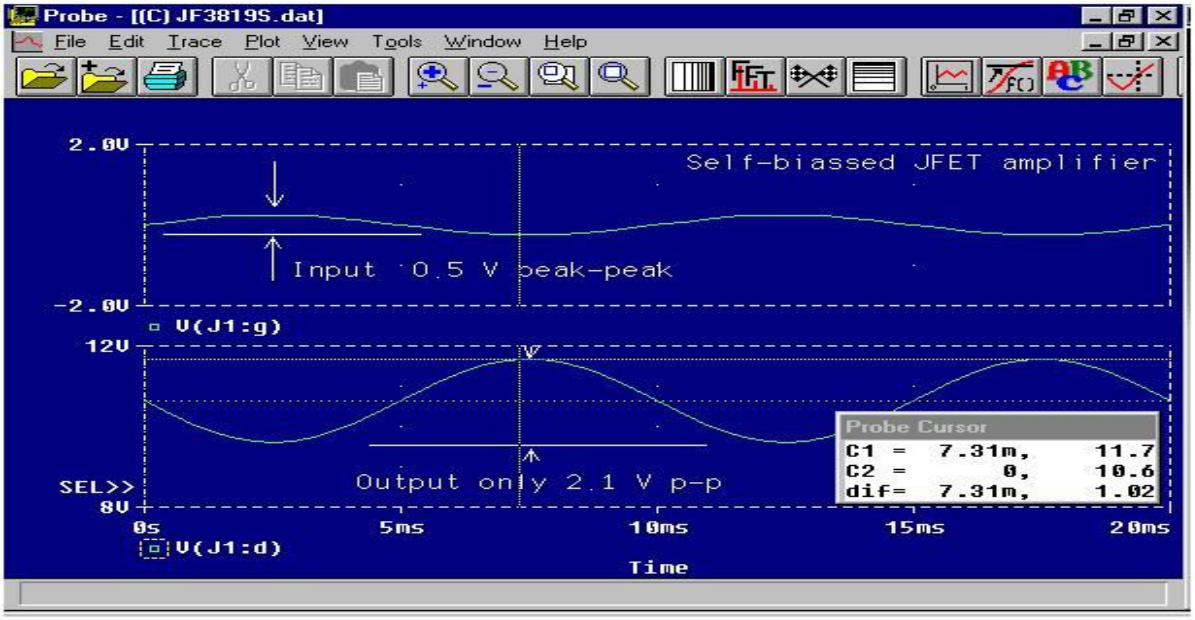
2.At a frequency of 5 KHz, measure the voltage gain, the input and the output resistance and compare your results withthe theoretical values. Calculate the power gain from both experimental and theoretical values.

3.Find the maximum peak-to-peak output voltage swing (i.e. the maximum swing without distortion).

4.Measure the frequency response of the circuit and comment on the change observed in comparison with a single stage common-emitter amplifier.

5.Simulate the circuit using Pspice. Compare the Pspice results with those obtained in the previous parts.

OUTPUT WAVEFORM:



RESULT:

Thus the simulation of common emitter and common source amplifier using PSPICE was simulated successfully.