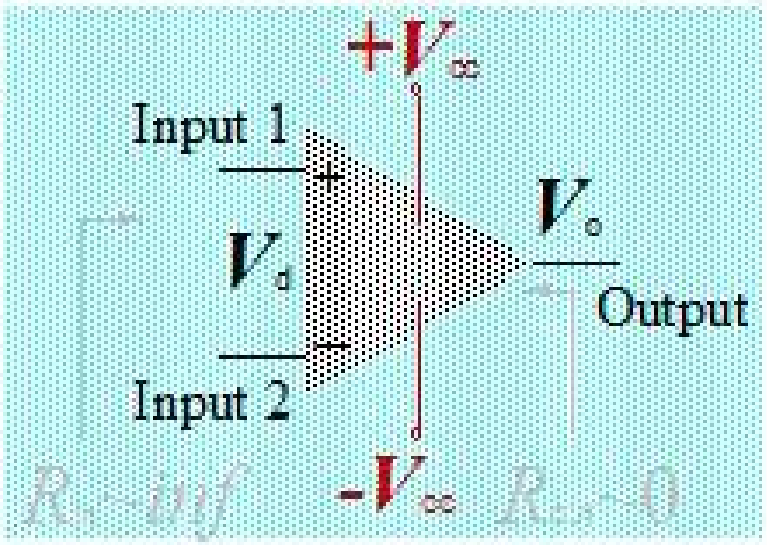
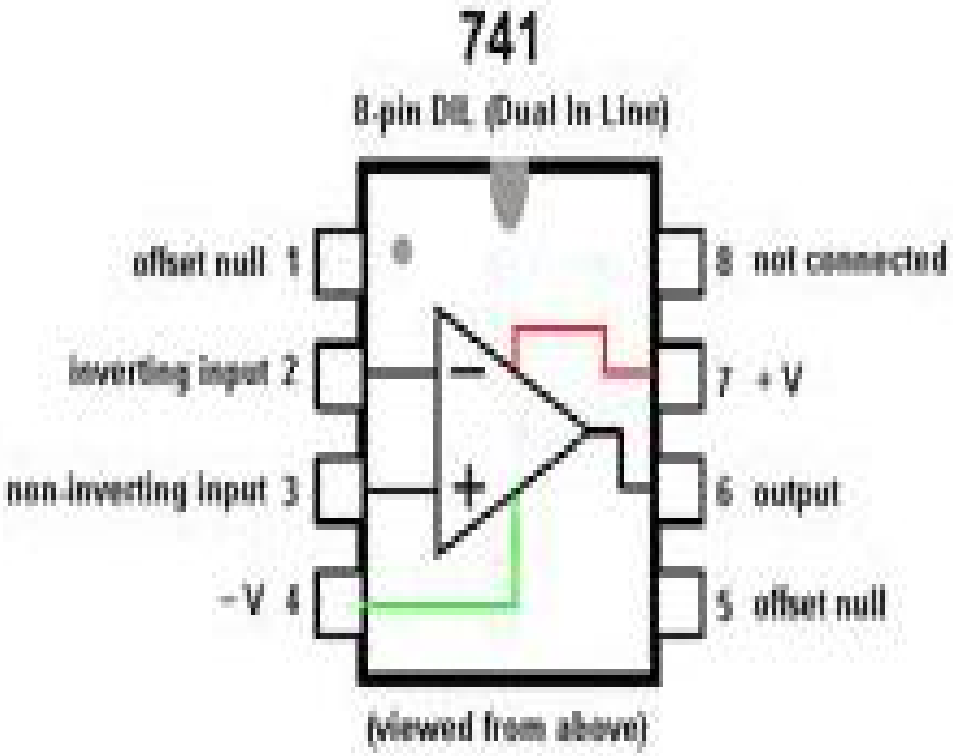
UNIT – I
Circuit Configuration for Linear ICs

Operational Amplifier (Op-Amp)

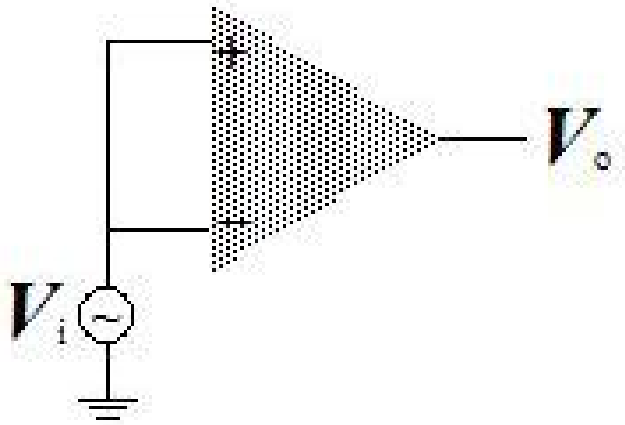
- Very high differential gain
- High input impedance
- Low output impedance
- Used in oscillator, filter and instrumentation
- Accumulate a very high gain by multiple stages




741
8-pin DIL (Dual In Line)
offset null 1
inverting input 2
non-inverting input 3
-V 4
8 not connected
7 +V
6 output
5 offset null
(viewed from above)

Common-Mode Operation

- Same voltage source is applied at both terminals
- Ideally, two input are equally amplified
- Output voltage is ideally zero due to differential voltage is zero
- Practically, a small output signal can still be measured

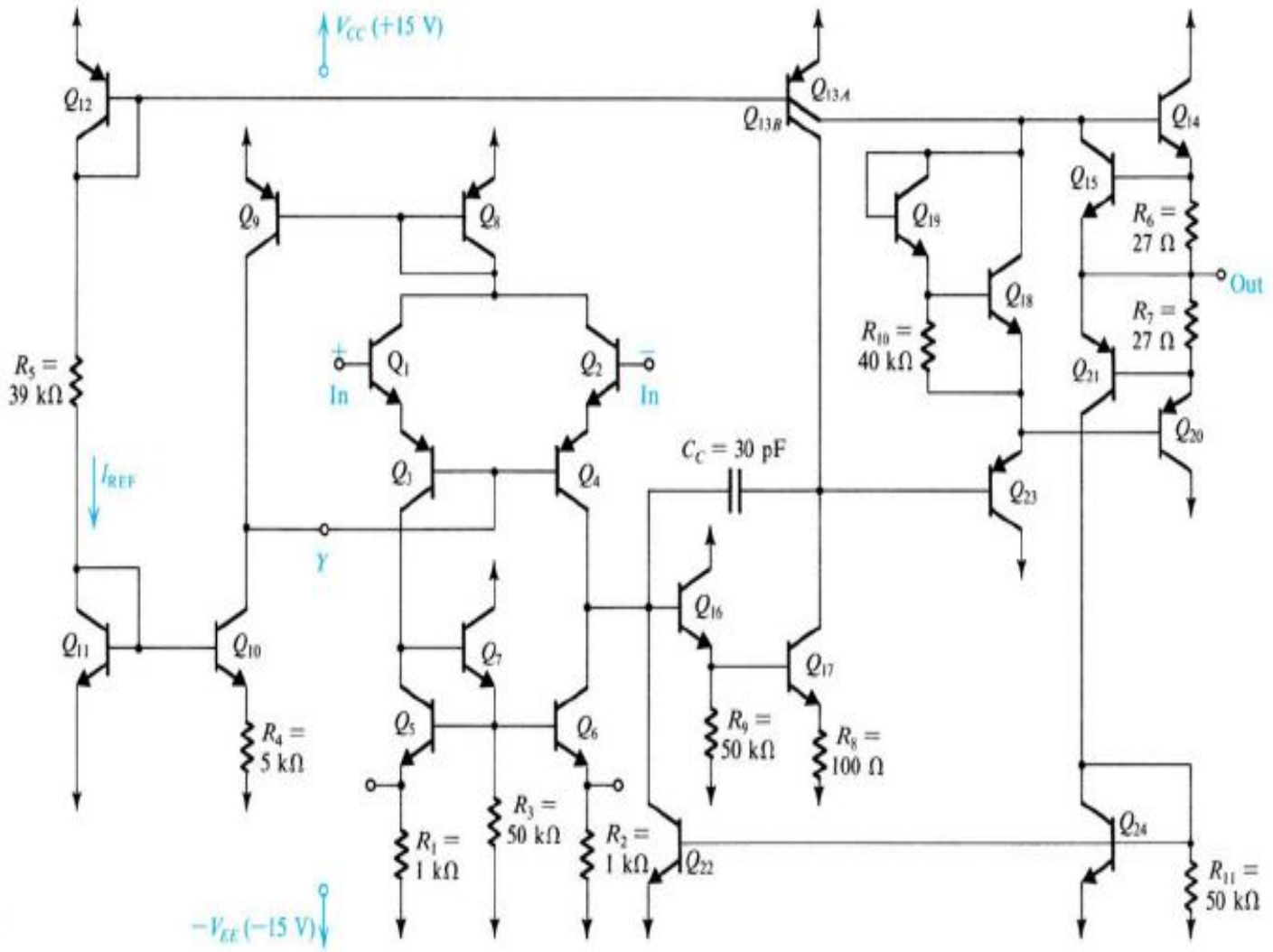


Characteristics of Ideal Op-Amp

- For an ideal Op-Amp, $V_1 = V_2 = 0$ and hence $I_1 = i_2 = 0$
- Open loop voltage gain $A_{OL} = \infty$
- Input Impedance $R_i = \infty$
- Output Impedance $R_o = 0$
- Bandwidth BW $= \infty$

Stages and Internal circuit of general Op-Amp (IC 741)

- General Stages
  - Input Stage
  - Intermediate Stage
  - Buffer and Level Shifting Stage
  - Output Stage


V_{CC} (+15 V)
Q_{12}
Q_{13A}
Q_{13B}
Q_{14}
Q_{15}
Q_{19}
R_6 = 27 Ω
Out
Q_{18}
R_7 = 27 Ω
R_{10} = 40 kΩ
Q_{21}
Q_{20}
Q_9
Q_8
R_5 = 39 kΩ
Q_1
Q_2
In
In
C_C = 30 pF
Q_3
Q_4
Q_{23}
I_{REF}
Y
Q_{16}
Q_{11}
Q_{10}
Q_7
Q_{17}
R_4 = 5 kΩ
Q_5
Q_6
R_9 = 50 kΩ
R_8 = 100 Ω
R_3 = 50 kΩ
R_1 = 1 kΩ
R_2 = 1 kΩ
Q_{22}
Q_{24}
R_{11} = 50 kΩ
$-V_{EE}$ (−15 V)

The Input Stage

- The input stage consists of transistors *Q1* through *Q7*.
- *Q1*-*Q4* is the differential version of CC and CB configuration.
- High input resistance.
- Current source (*Q5*-*Q7*) is the active load of input stage. It not only provides a high-resistance load but also converts the signal from differential to single-ended form with no loss in gain or common-mode rejection.

The Intermediate Stage

- The intermediate stage is composed of Q_{16}, Q_{17} and Q_{13B}.
- Common-collector configuration for Q_{16} gives this stage a high input resistance as well as reduces the load effect on the input stage.
- Common-emitter configuration for Q_{17} provides high voltage gain because of the active load Q_{13B}.
- Capacitor Cc introduces the miller compensation to insure that the op amp has a very high unit-gain frequency.

Level Shifting Stage

- All stages coupled to each other, hence voltage level of previous stage applied to next stages.
- So stage by stage d.c level increases , such high voltage drives the transistors into saturation
- Hence before output stage, it is necessary to bring such high voltage to zero volt.
- Level shifter brigs the d.c level down to ground potential when no signal is applied
- The buffer is an emitter follower whose input impedance is very high.

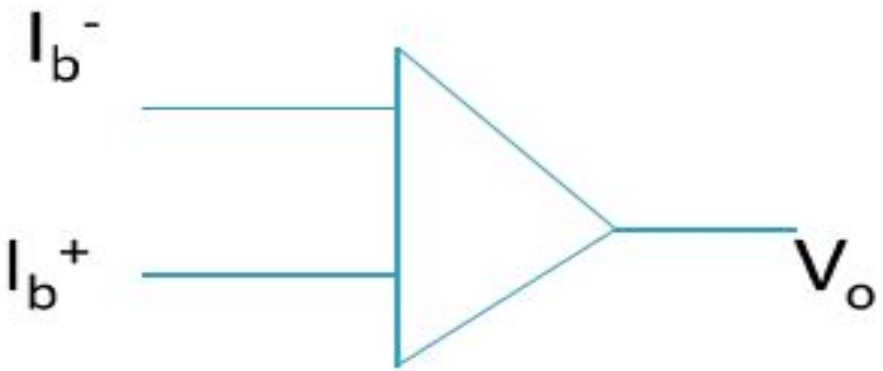
The Output Stage

- The output stage is the efficient circuit called class AB output stage.
- Voltage source composed of Q_{18} and Q_{19} supplies the DC voltage for Q_{14} and Q_{20} in order to reduce the cross-over distortion.
- Q_{23} is the CC configuration to reduce the load effect on intermediate stage.
- Short-circuit protection circuitry
  - Forward protection is implemented by R_6 and Q_{15}.
  - Reverse protection is implemented by R_7, Q_{21}, current source(Q_{24}, Q_{22}) and intermediate stage.

DC Characteristics

- Input Bias Current (I_b)
- Input Offset Current(I_{os})
- Input Offset Voltage (V_{ios})
- Thermal Drift

Input Bias Current



Bias Current $I_B = \frac{I_b^+ + I_b^-}{2}$

Input Offset Current

- Input Offset current will work if both bias currents are equal.
- If they are not equal, the difference between them is know as Input Offset current

$$I_{os} = I_b^+ - I_b^-$$

Input Offset Voltage

- Due to unavoidable imbalances inside the op-amp, the output voltage will not be zero with zero input voltage. This voltage is called as input offset voltage.

Considering this voltage V_{ios},

Output Voltage $V_o = (1 + \frac{R_f}{R_1})V_{ios}$

Thermal Drift

- Bias current, Offset current and Offset voltages change with temperature. This change is called as drift.
- Offset current drift is expressed in nA/^{0}C
- Offset voltage drift is expressed in mV/^{0}C
- To avoid this drift careful printed circuit board layout must be used and forced air cooling may be used to stabilize the ambient temperature.

AC Characteristics (Slew Rate – SR)

- The maximum rate of change of output voltage caused by step input voltage , specified in V/μs
- **Cause of SR**:

There is a **capacitor** within an op-amp which prevent the output voltage from responding immediately to a fast change in input. This capacitor caused the SR

- For example, if $V_o = V_m \sin \omega t$

Then the rate of change of output is,

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t$$

The maximum rate of change occurs when $\cos \omega t = 1$

Therefore SR = $(dv_o/dt)\max = \omega V_m$

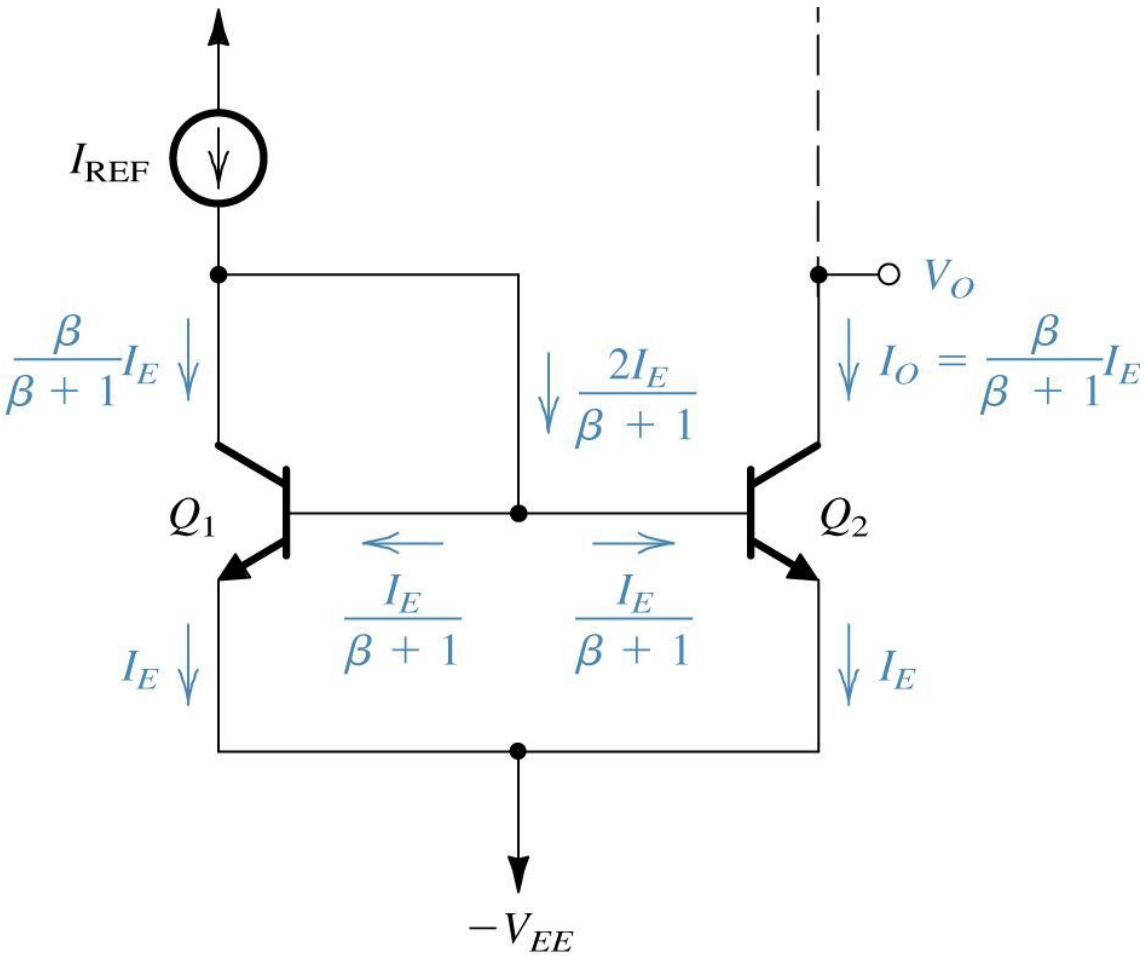
Or SR = $2\pi f V_m$ V/s

Or SR = $\frac{2\pi f V_m}{10^6}$ V/μs

- Current Mirror Circuit:

  A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading.

Current Mirror



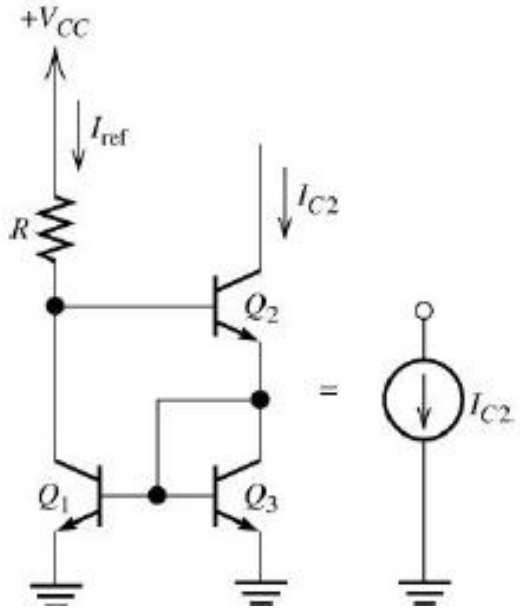
The Wilson current source

An improved circuit, called Wilson current source, with higher output impedance that the previous current mirror.

For the Wilson current source, the following

$$I_{ref} = \frac{V_{CC} - V_{BE2} - V_{BE3}}{R}$$

$$I_{C2} \approx \frac{A_3}{A_1} I_{ref}$$



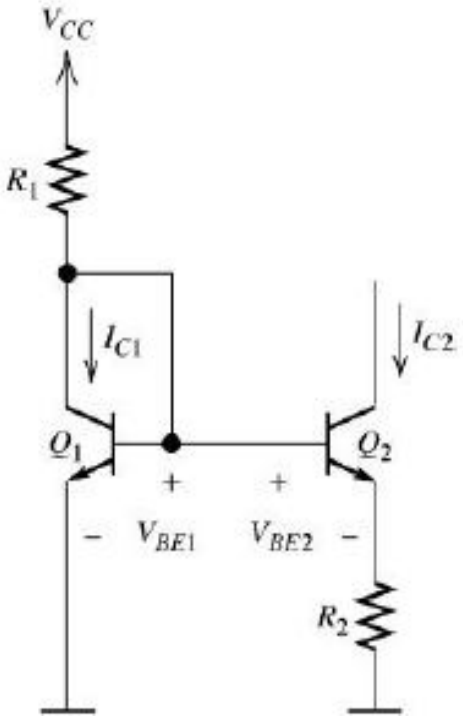
The Widlar current source

When the desired current is small, the Widlar current source may be a better alternative, as shown in the Figure.

For Widlar current source,

$$R_2 \approx \frac{V_T}{I_{C2}} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$I_{C1} \approx I_{ref} = \frac{V_{CC} - V_{BE1}}{R_1}$$



Voltage Reference Circuits

- Used to provide a constant d.c voltage, which acts as a reference for other circuits
- It is independent of changes in the parameters like temperature, input line voltage and load current
- Accuracy and stability with temperature are the basic characteristics of any voltage reference circuit
- Temperature coefficient TC = $\Delta Vo/\Delta T$ in $mV/^0C$

Performance parameters of Voltage reference circuits

- **Line regulation** (Input/Supply regulation)

$$\text{Line Regulation} = \frac{\Delta v_o}{\Delta v_i}$$

- **Load regulation**

$$\text{Load Regulation} = \frac{\Delta v_o}{\Delta I_L}$$

- **Long term stability**

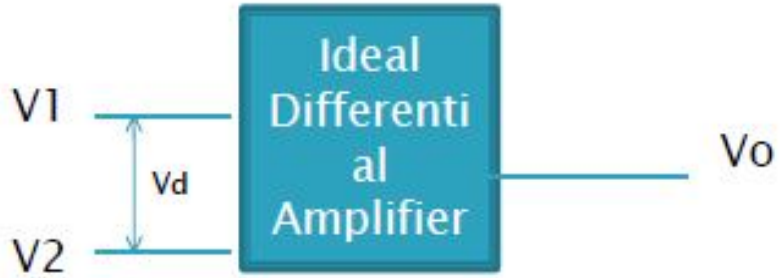
The ability of circuit to maintain the output voltage constant with respect to time

- **Ripple Rejection Ratio (RRR)**

$$\text{RRR} = 20 \log \frac{v_{ri}}{v_{ro}}$$

Differential Amplifier

- Amplifies the difference between two input voltages. ($V_d = V_1 - V_2$)

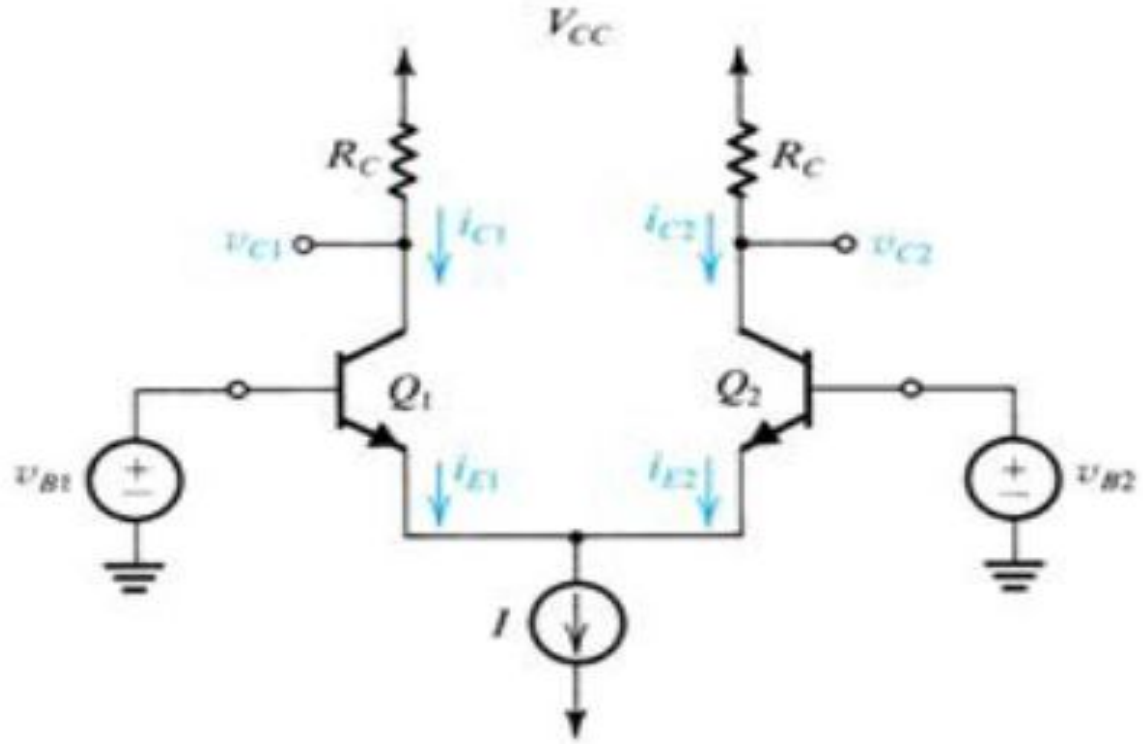


- V_o ά (V_1–V_2)
- $V_o = A_d(V_1–V_2)$ where A_d = Differential Gain

  $V_o = A_dV_d$, hence $A_d = V_o/V_d$

  $A_d = 20 \log A_d$ (dB)

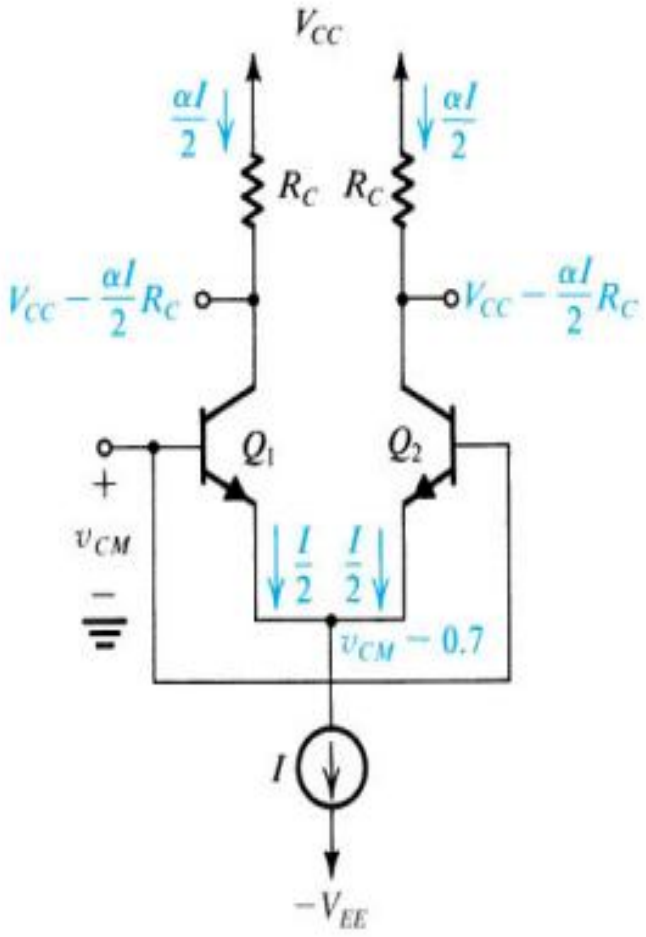
BJT Differential Amplifier



The basic BJT differential-pair configuration.

Difference Mode Operation

- Q1 positive going, Q2 negative going signal
- Hence there will be negative going output at the collector of Q1 and positive going output at the collector of Q2
- So the difference between two voltages Vo is the twice as large as the signal voltage.



- **Common Mode Operation**
- The differential pair with a common-mode input signal V_{CM}.
- Two transistors are matched.
- Current is divided equally between two transistors.
- The difference in voltage between the two collector is zero.

Configurations of Differential Amplifier

- Dual input , balanced output
- Dual input, unbalanced output
- Single input, balanced output
- Single input, unbalanced output

Note:

- If output is taken between two collectors – balanced output
- If output is taken between one collector with respect to ground then it is unbalanced output

D.C Analysis of Differential Amplifier

Applying KVL to base-emitter loop,

$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0$ ------(1)

But, $I_C = \beta I_B$ and $I_C \approx I_E$

Therefore, $I_B = I_E/\beta$ -------(2)

(2) In (1) we get,

$[-I_E R_S/\beta] - V_{BE} - 2I_E R_E + V_{EE} = 0$

$I_E[(-R_S/\beta) - 2R_E] + V_{EE} - V_{BE} = 0$ ---------(3)

Therefore

$$IE = \frac{V_{EE} - V_{BE}}{\left(\frac{R_s}{\beta}\right) - 2R_E}$$ ----------(4)

In practical,

$R_s / 2R_E$, hence $I_E = [V_{EE} - V_{BE}]/2R_E$ ----------(5)

- The collector voltage of Q1

$$V_c = V_{cc} - I_c R_c \qquad \text{----(5)}$$

And $V_{CE} = V_c - V_E = (V_{CC} - I_C R_C) - (-V_{BE})$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \qquad \text{----(6)}$$

For the differential amplifier,

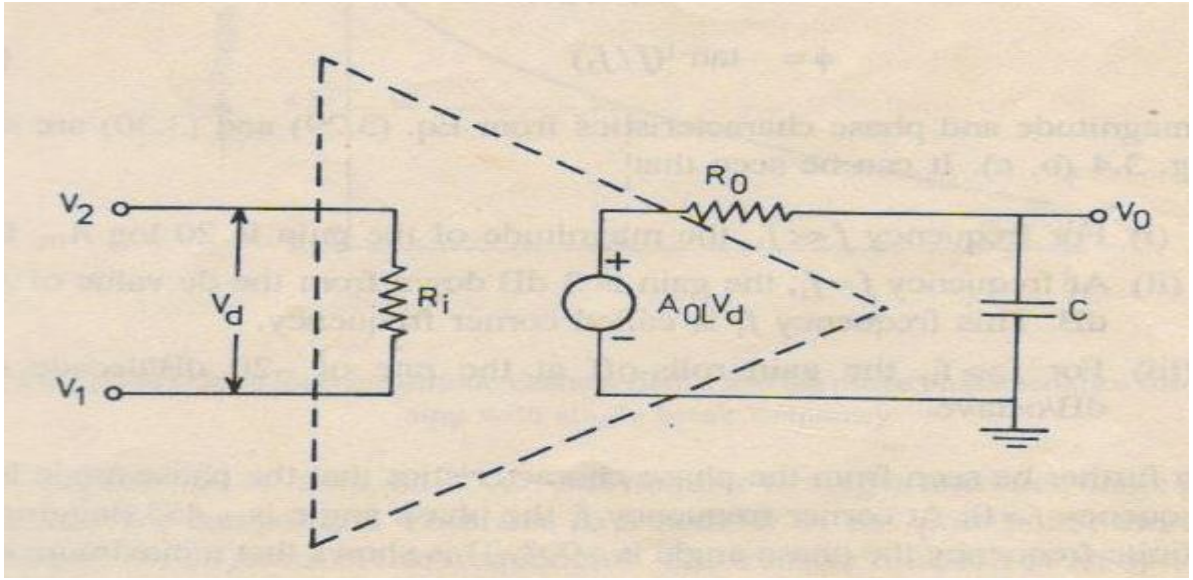
The operating point values

$$V_{CEQ} \approx V_{CE}$$

And $$I_{CQ} \approx I_E$$

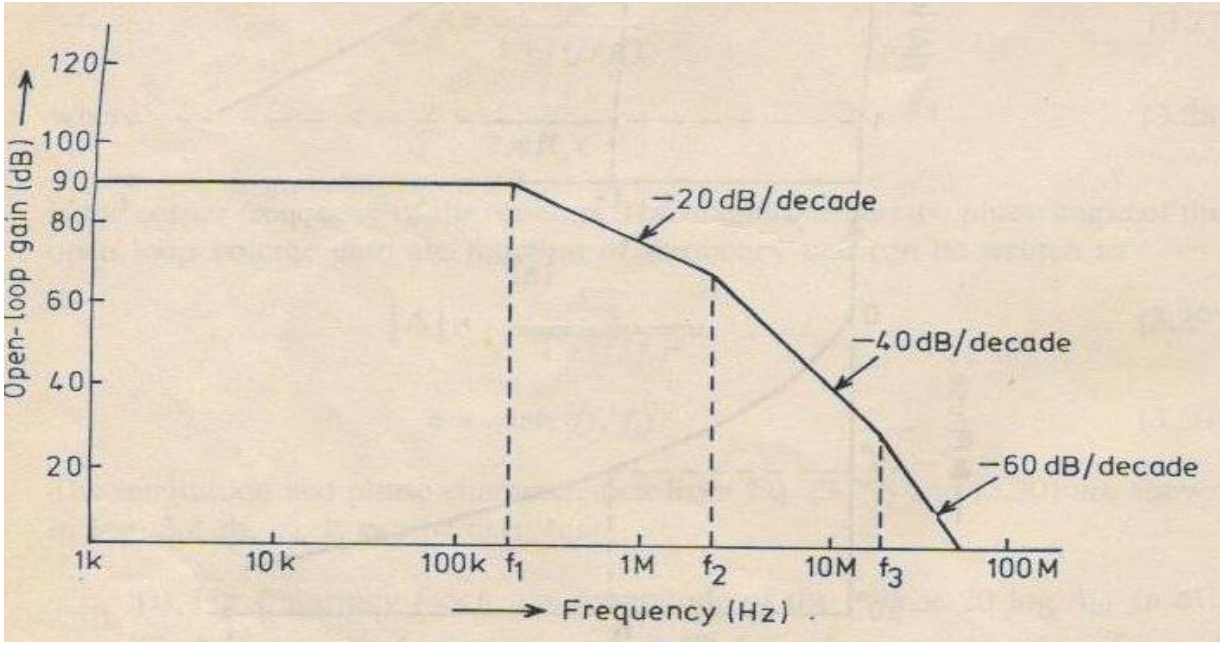
Frequency Response

High Frequency Model Of OP AMP



AC characteristics

- **Frequency Response**



Need for frequency compensation in practical op-amps

- Frequency compensation is needed when large bandwidth and lower closed loop gain is desired.
- Compensating networks are used to control the phase shift and hence to improve the stability

Frequency compensation methods

- Dominant- pole compensation

- Pole- zero compensation

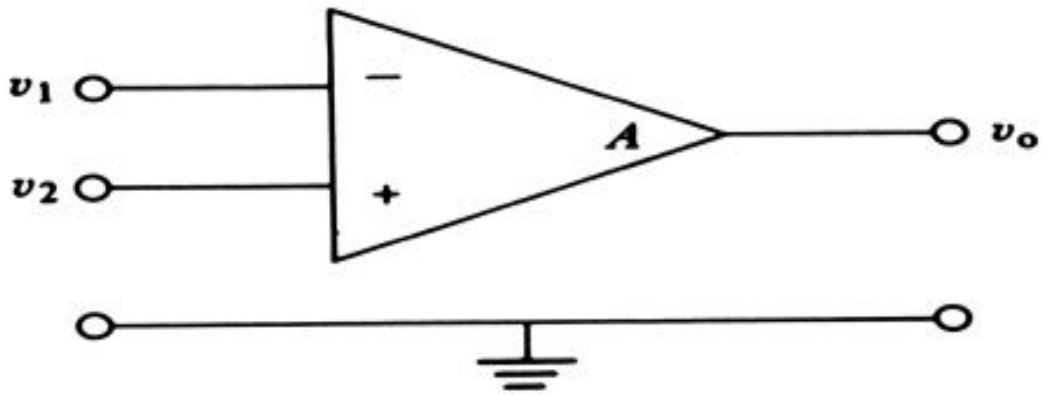
Stability of Opamp

- To evaluate the stability potential for a particular amplifier type, "gain vs frequency" and "phase vs frequency" is needed.
- If the phase response exhibits -180^{o} at a frequency where the gain is above unity, the negative feedback will become positive feedback and the amplifier will actually sustain an oscillation.
- Even if the phase lag is less than -180^{o} and there is no sustained oscillation, there will be overshoot and the possibility of oscillation bursts triggered by external noise sources, If the phase response is not "sufficiently less" than -180^{o} for all frequencies where the gain is above unity.
- The "sufficiently less" term is more properly called phase margin. If the phase response is -135^{o}, then the phase margin is 45^{o} (the amount "less than" -180^{o}).
- Actually, the phase margin of interest to evaluate stability potential must also include the phase response of the feedback circuit. When this combined phase margin is 45^{o} or more, the amplifier is quite stable. The 45^{o} number is a "rule of thumb" value and greater phase margin will yield even better stabilitv and less overshoot.

UNIT II

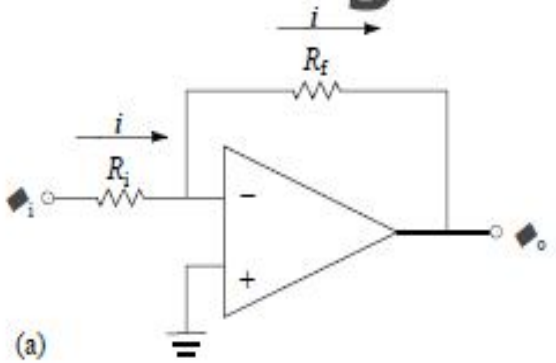
APPLICATIONS OF OPERATIONAL AMPLIFIER

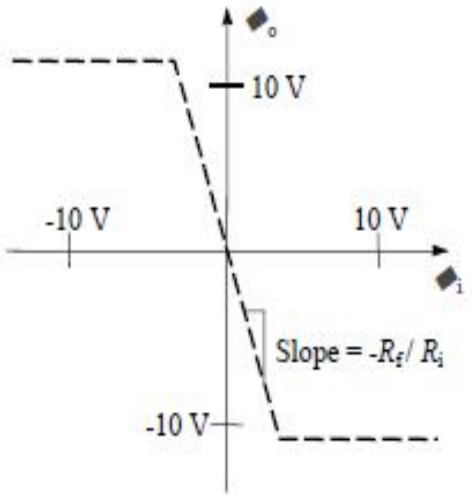
Two Basic Rules



- Rule 1
  - When the op-amp output is in its linear range, the two input terminals are at the same voltage.
- Rule 2
  - No current flows into or out of either input terminal of the op amp.

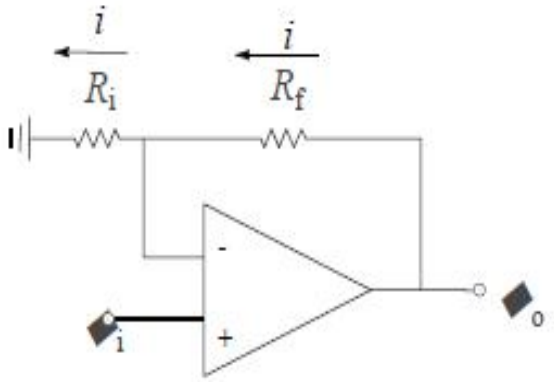
Inverting Amplifier

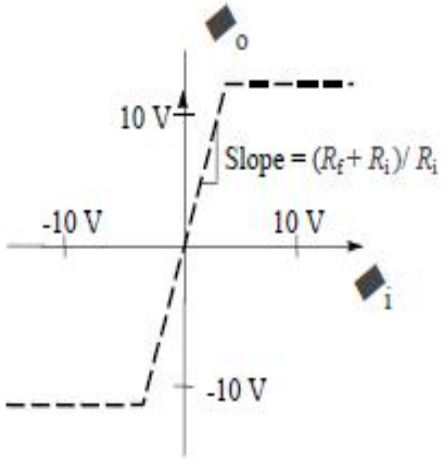




$$v_o = -\frac{R_f}{R_i} v_i \qquad G = \frac{v_o}{v_i} = -\frac{R_f}{R_i}$$

Noninverting Amplifier

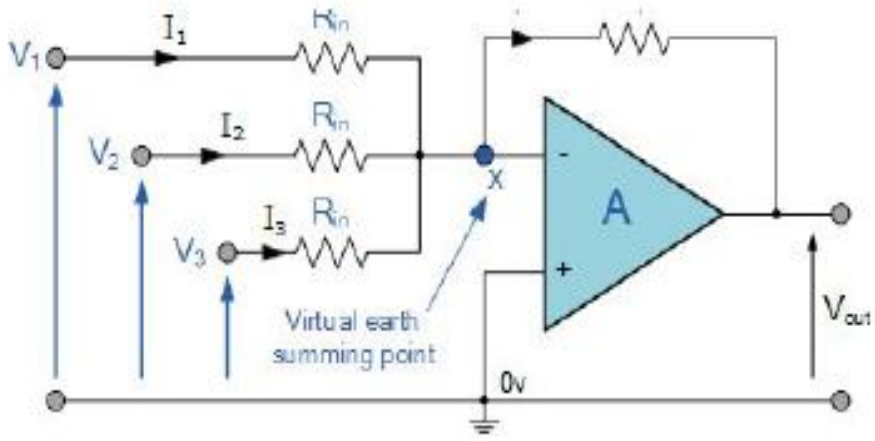




$$v_o = \frac{R_f + R_i}{R_i} v_i$$

$$G = \frac{R_f + R_i}{R_i} = \left(1 + \frac{R_f}{R_i}\right)$$

Summing Amplifier



Summing Amplifier

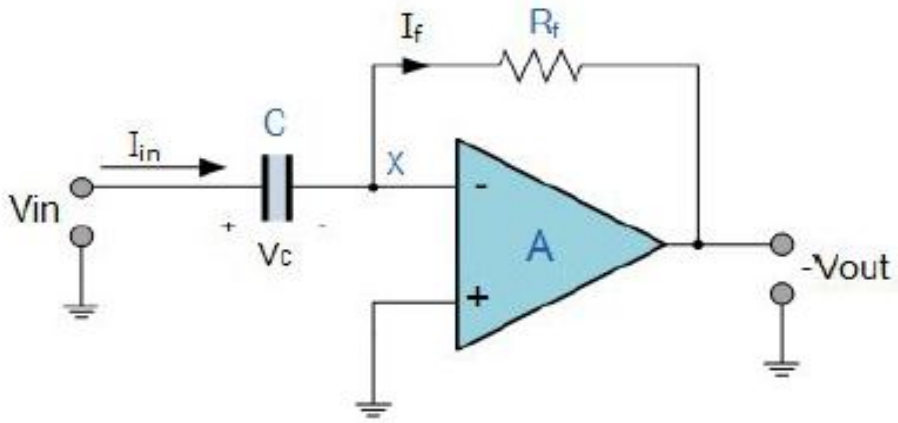
$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

Inverting Equation: $Vout = -\frac{Rf}{Rin} \times Vin$

then, $-Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$

$$-Vout = \frac{R_F}{R_{IN}}\left(V1 + V2 + V3 \ldots . etc\right)$$

Op-amp Differentiator



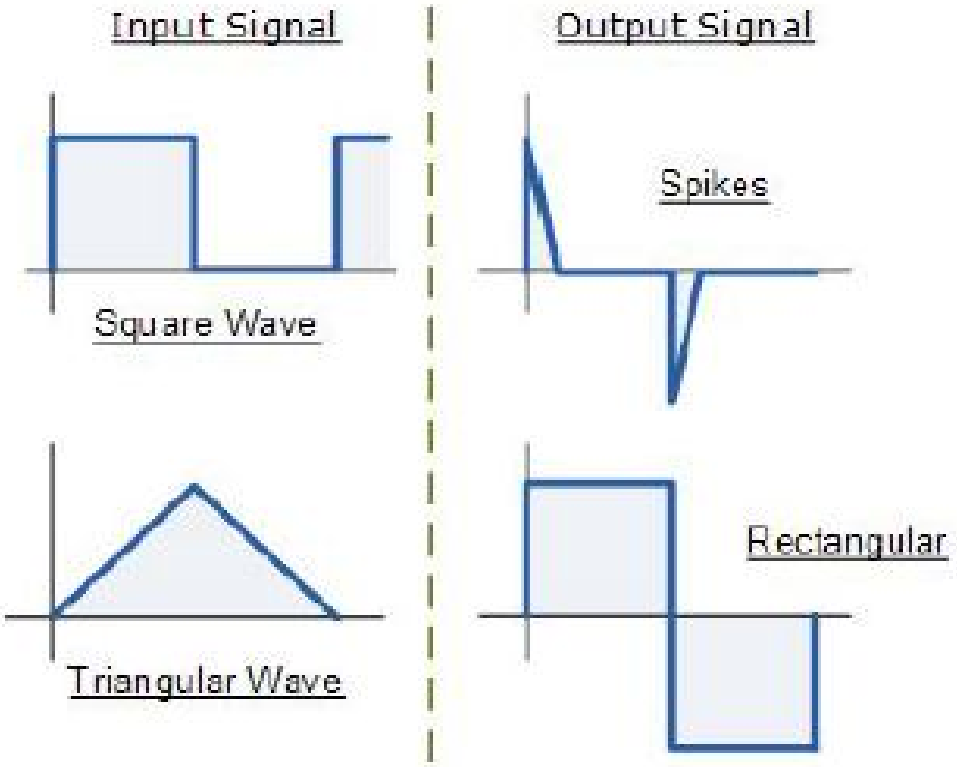
Applying KCL at inverting node of opamp, we get

$$(0-V_{out})/R + I_c = 0$$

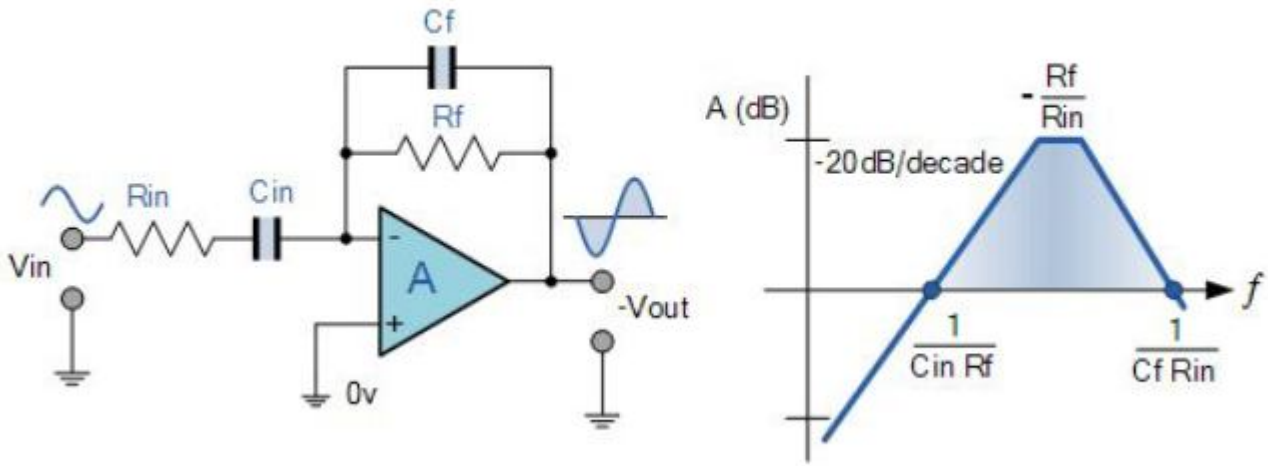
$$I_c = V_{out}/R$$

where $I_c = C*d(0-V_{in})/dt$. Hence we get $V_{out} = -R*C*dV_{in}/dt$.

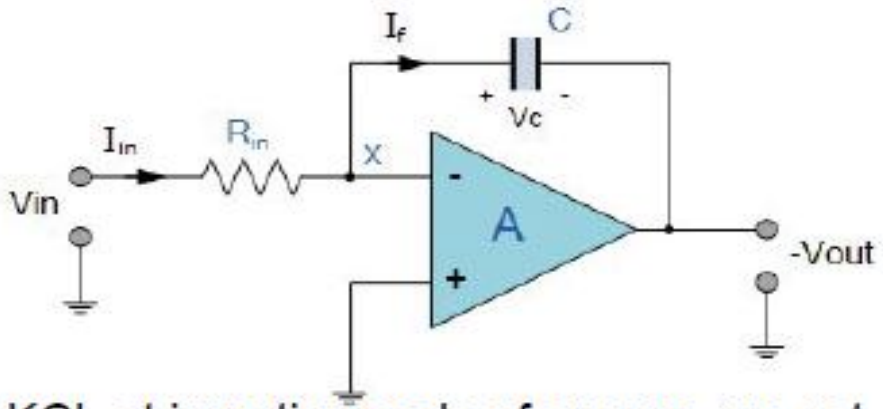
Op-amp Differentiator



Improved Opamp Differentiator



Opamp Integrator



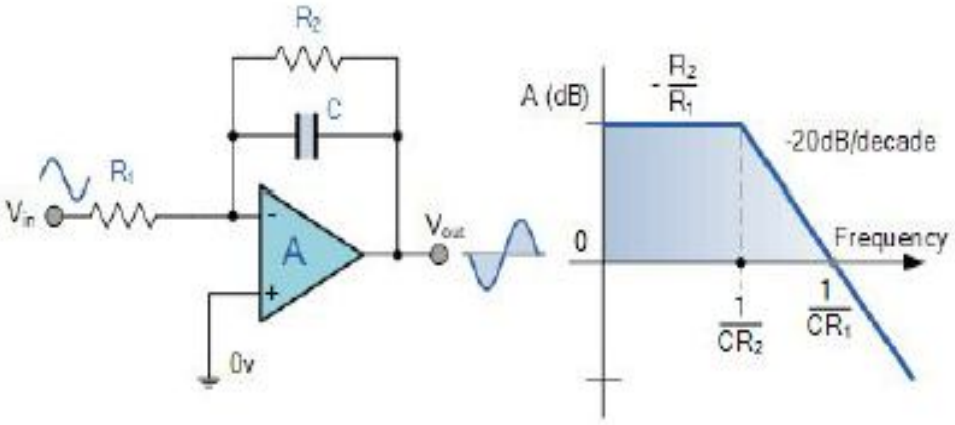
Applying KCL at inverting node of opamp, we get

$(0-V_{out})/R + I_c = 0$

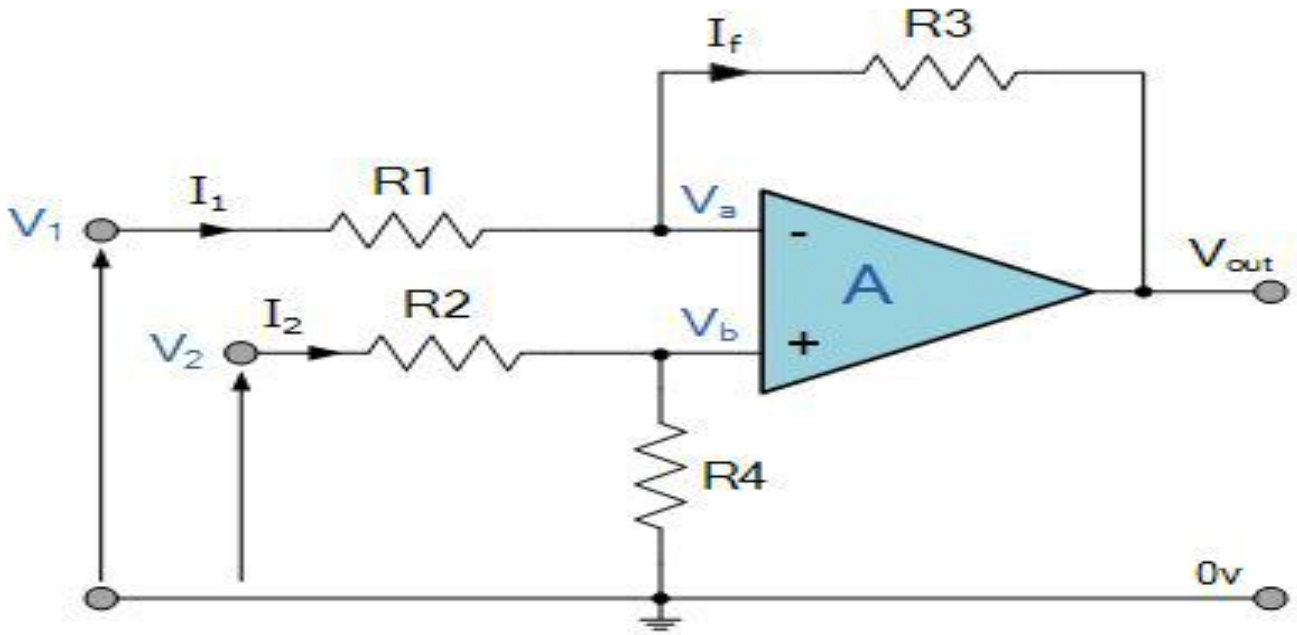
$Ic = Vout/R = 1/\int V_{in} * dt$

$$V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$$

Practical Integrator



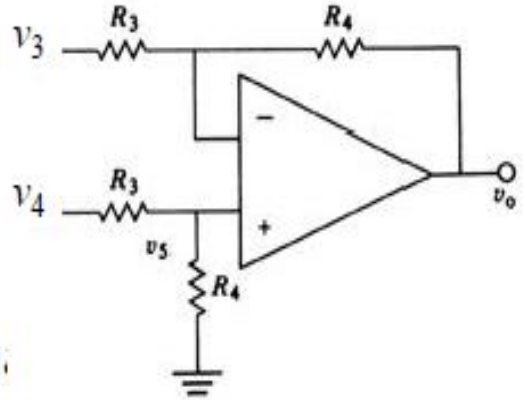
Differential Amplifier



Differential Amplifiers

- Differential Gain G_d

$$G_d = \frac{v_o}{v_4 - v_3} = \frac{R_4}{R_3}$$



- Common Mode Gain G_c
  - For ideal op amp if the inputs are equ
    then the output = 0, and the G_c = 0.
  - No differential amplifier perfectly rejects the common-mode voltage.

$$v_o = \frac{R_4}{R_3}(v_4 - v_3)$$

- Common-mode rejection ratio *CMMR*
  - Typical values range from 100 to 10,000

$$CMRR = \frac{G_d}{G_c}$$

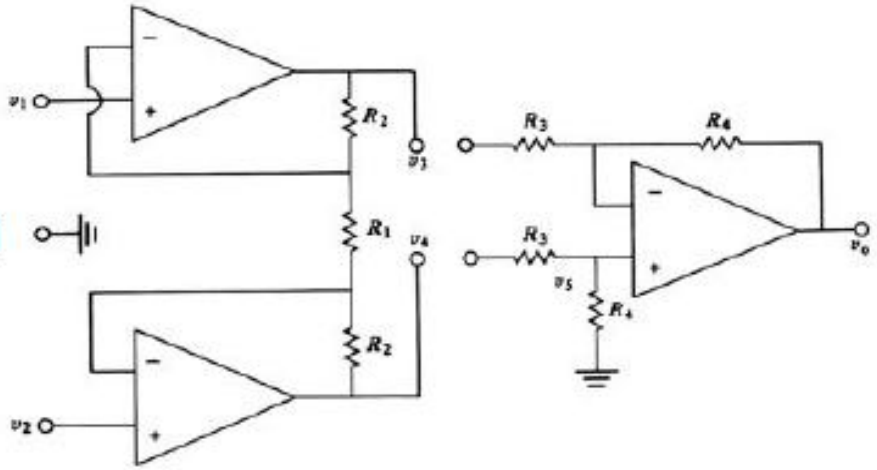
Instrumentation Amplifier

- In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

Features of Instrumentation Amplifier:

1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature co- efficient
4. low dc offset
5. low output impedance

Instrumentation Amplifiers



Differential Mode Gain

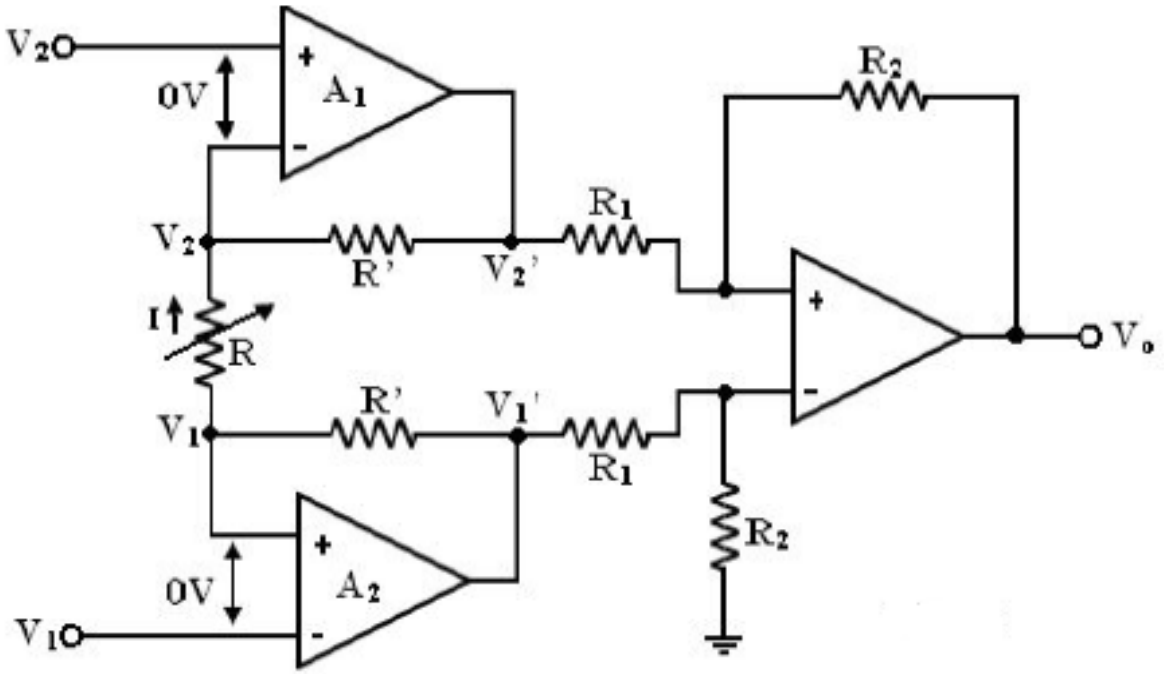
$$v_3 - v_4 = i(R_2 + R_1 + R_2)$$

$$v_1 - v_2 = iR_1$$

$$G_d = \frac{v_3 - v_4}{v_1 - v_2} = \frac{2R_2 + R_1}{R_1}$$

Advantages: High input impedance, High CMRR, Variable gain

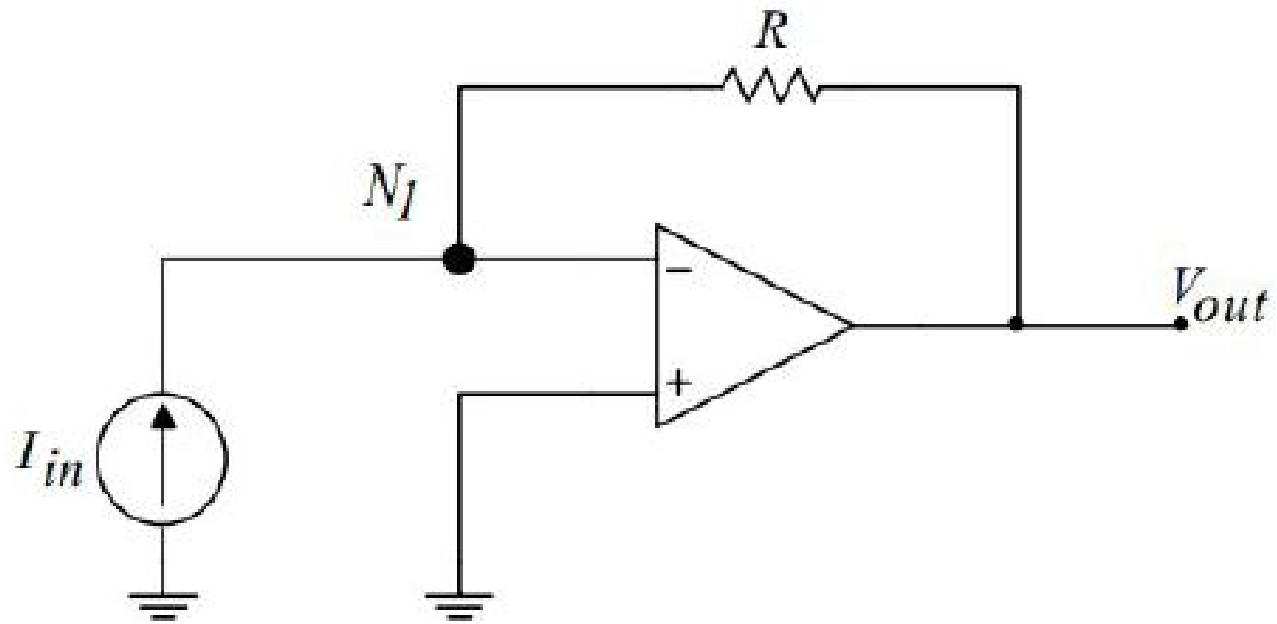
Instrumentation Amplifier



Applications of Instrumentation Amplifier

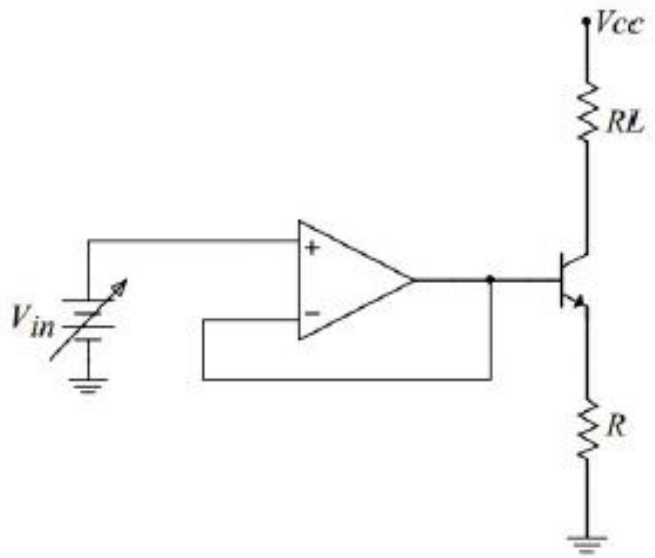
- *Audio applications involving weak audio signal or noisy environment*
- *Medical instruments*
- *High frequency signal amplification in cable RF*
- *Current/voltage monitoring*
- *Data acquisition*

Current to Voltage Converter (Transresistance Amplifier)



$$I_1 + \left(\frac{V_{out} - 0}{R} \right) = 0 \Rightarrow \boxed{V_{out} = -RI_1}$$

Voltage to Current Converter (Transconductance Amplifier)

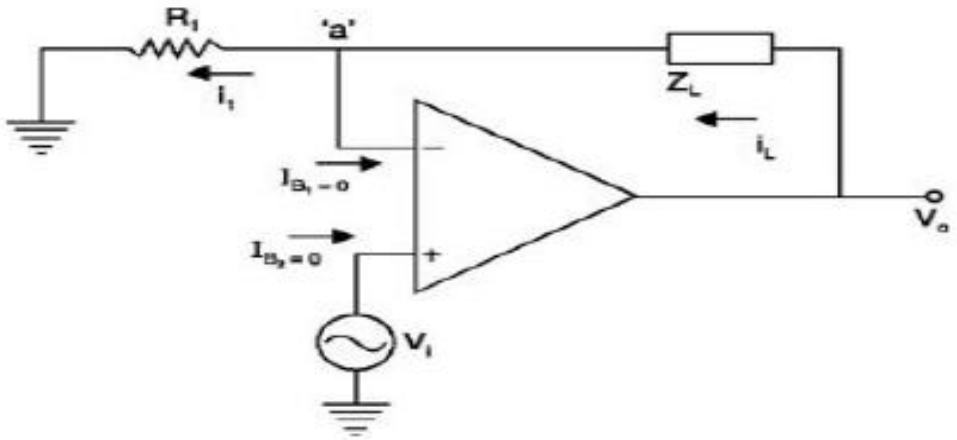


$$I_{out} = SV_{in}$$

Where S is the sensitivity or gain of the V-I converter.

$$I_L = V_{in}/R_L$$

Transconductance amplifier with floating Load



$$V_a = V_i$$

$$I_{B1} = I_{B2} = 0$$

$$i_L + I_{B1} = i_1$$

$$i_L = i_1$$

$$i_1 = \frac{V_a - 0}{R_1}$$

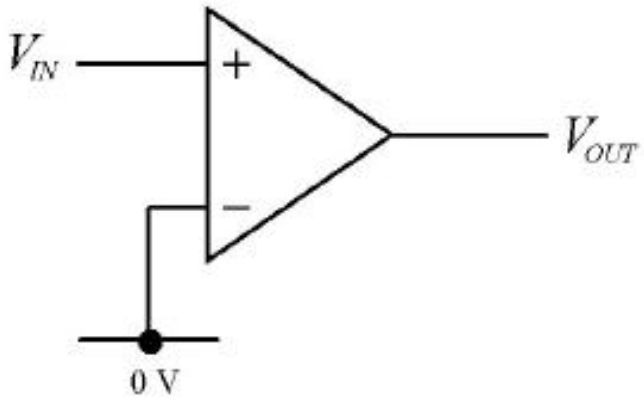
$$i_1 = \frac{V_a}{R_1}$$

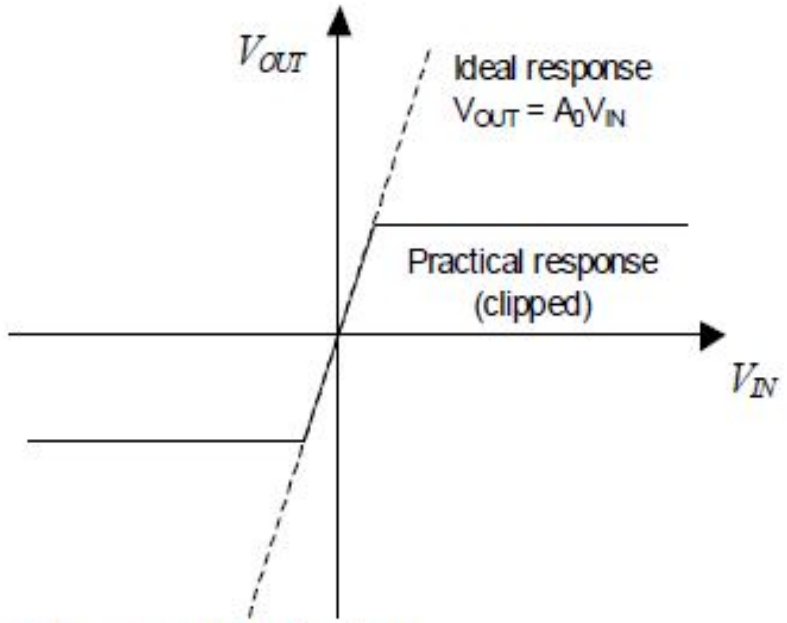
$$i_L = \frac{V_i}{R_1}$$

Non-Linear Op-Amp Applications

- Applications using saturation
  - Comparators
  - Comparator with hysteresis (Schmitt trigger)
  - Oscillators
- Applications using active feedback components
  - Log, antilog, squaring etc. amplifiers
  - Precision rectifier

Comparators



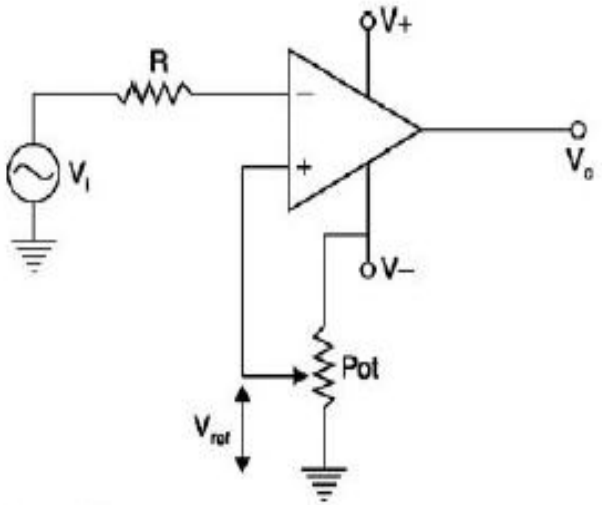


If A_0 is large, practical response can be approximated as :

$V_{IN} > 0 \Rightarrow V_+ > V_- \Rightarrow V_{OUT} = +V_{SAT}$

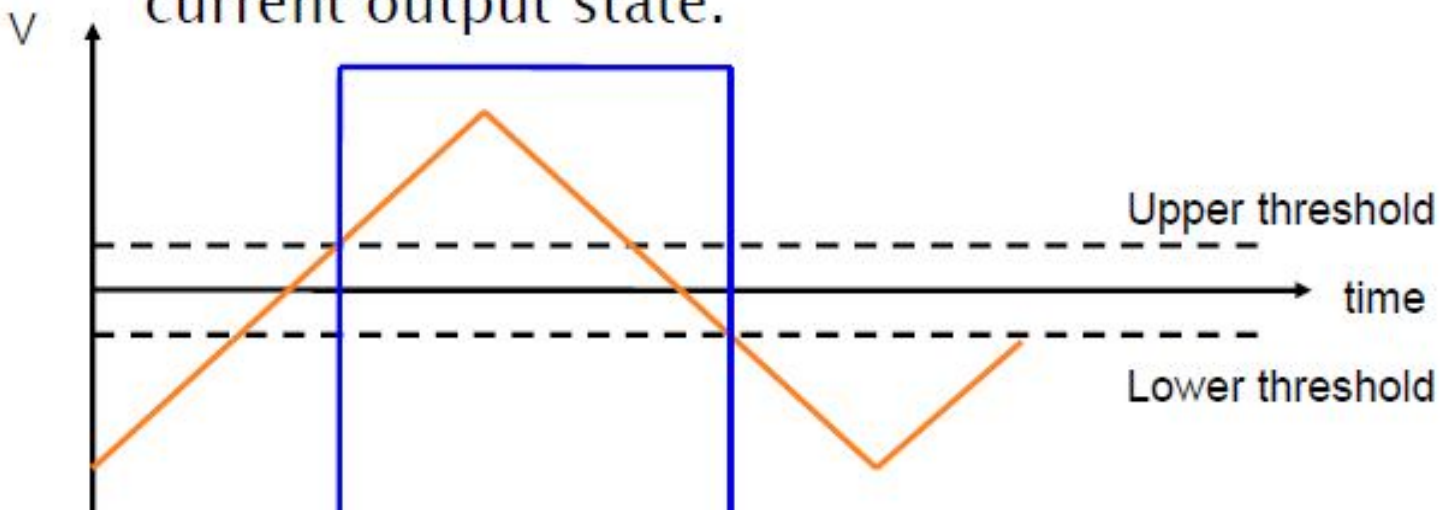
$V_{IN} < 0 \Rightarrow V_+ < V_- \Rightarrow V_{OUT} = -V_{SAT}$

INVERTING COMPARATOR

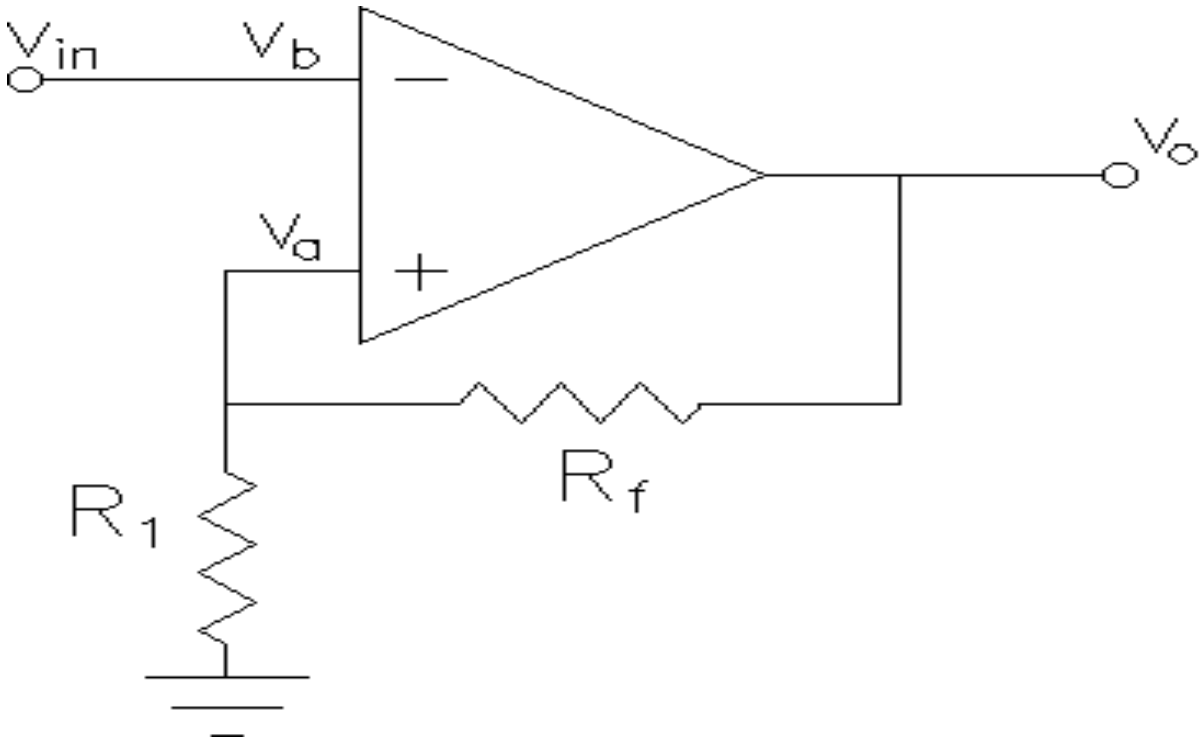


Hysteresis

- A comparator with hysteresis has a 'safety margin'.
- One of two thresholds is used depending on the current output state.



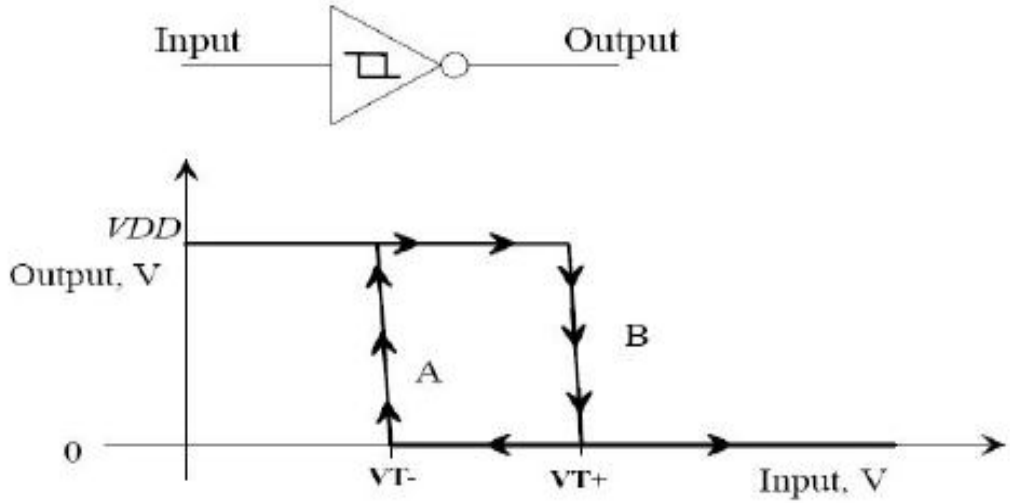
Schmitt trigger



Schmitt trigger

- Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform

Hysterisis

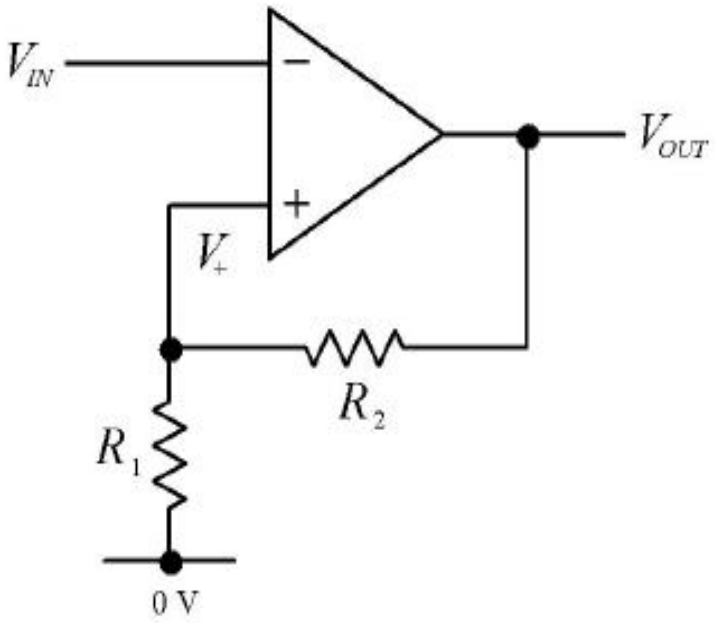


Transfer characteristics of a Schmitt trigger

Hysteresis = $V_{upper\ threshold} - V_{lower\ threshold}$

$= \beta * V_{cc} - (-\beta * V_{cc}) = 2 * \beta * V_{cc} = 2 * V_{cc} * R_2/(R_2+R_1)$

Schmitt Trigger Analysis



Switching occurs when:

$$V_{IN} = V_- = V_+ = V_{OUT}\frac{R_1}{R_1 + R_2}$$

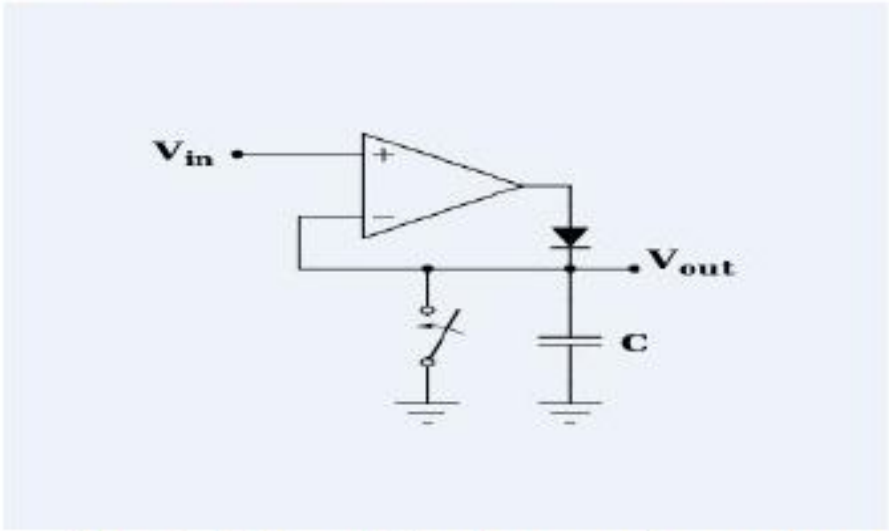
But,

$$V_{OUT} = \pm V_{SAT}$$

$$\therefore V_{THRESH} = \pm V_{SAT}\frac{R_1}{R_1 + R_2}$$

Peak Detector

Peak detector detects and holds the most positive value of attained by the input signal prior to the time when the switch is closed.

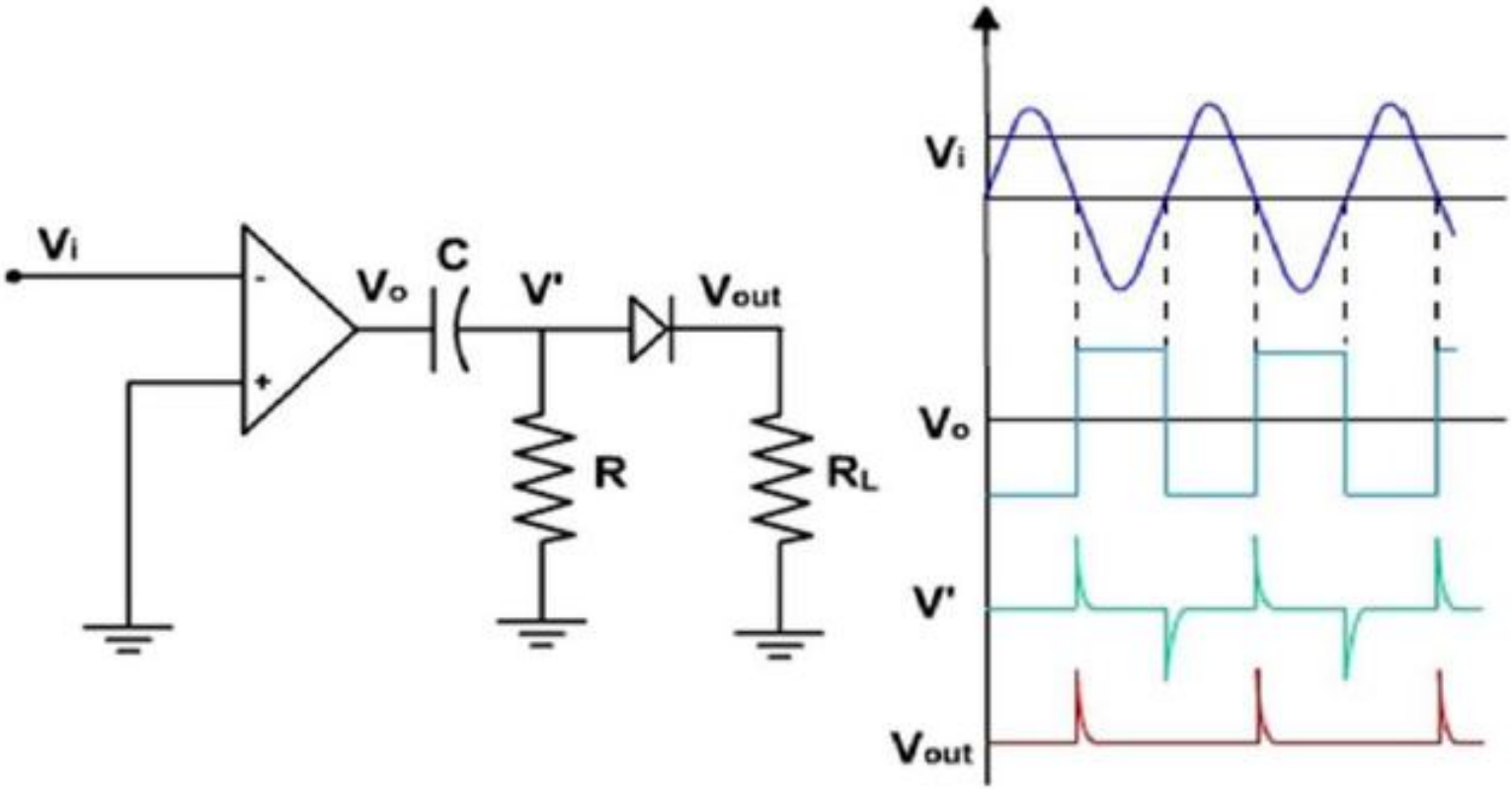


$V_{out} < V_{in}$; D ON and C charges to peak value of input,
$V_{out} < V_{in}$; D OFF and C holds the peak value of input

- a)$V_{out} < V_{in}$ the op amp output V' is positive so that the diode conducts and the capacitor charges to the input value at that instant as it forms a voltage follower circuit.
- b) When $V_{out} > V_{in}$, op amp output V' is negative and the diode becomes reverse biased.
- Thus the capacitor charges to the most positive value of input.

Op amp zero crossing detector

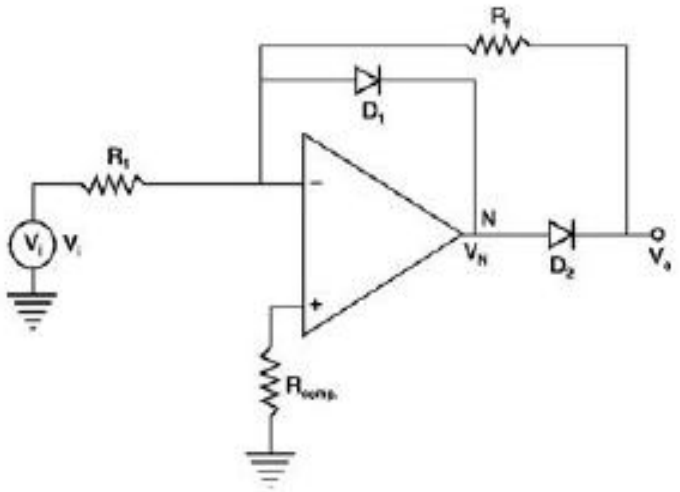
- In opamp zero crossing detectors the output responds almost discontinuously every time the input passes through zero. It consists of a comparator circuit followed by differentiator and diode arrangement.

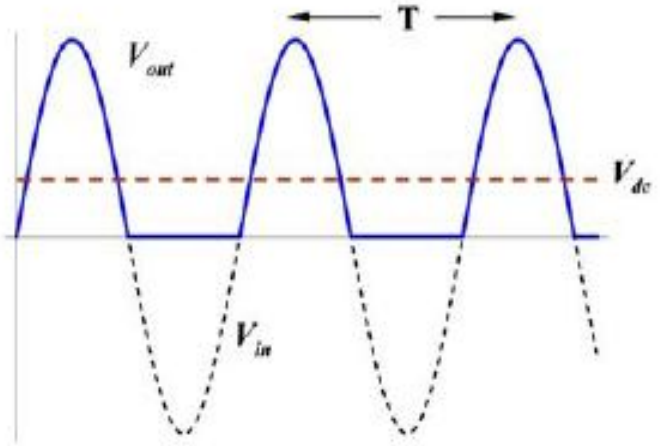


$V_{in}>0, V_o=+V_{cc}$, V' = R*C*dVo/dt positive spike, D ON and C charges through R and R_L to $+V_{cc}$;

$V_{in}>0, V_o=-V_{cc}$, V' = R*C*dVo/dt negative spike, D OFF and C discharges through R to $+V_{cc}$

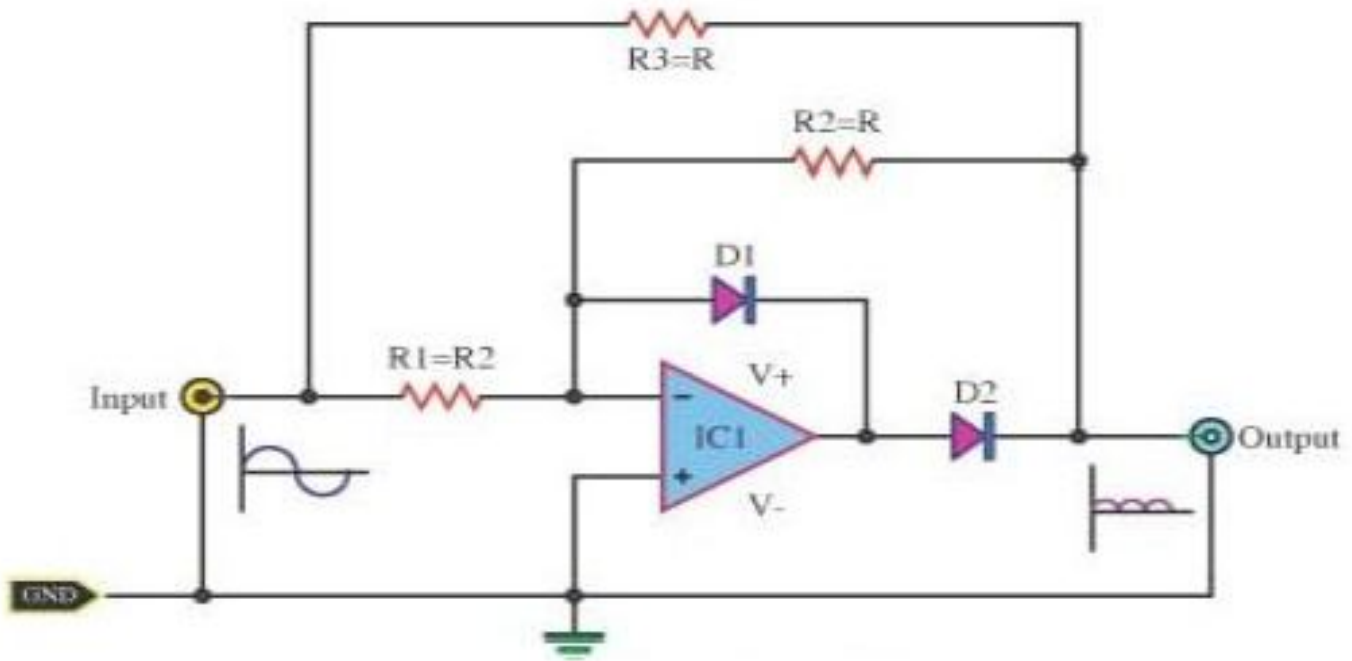
Opamp Half wave rectifier



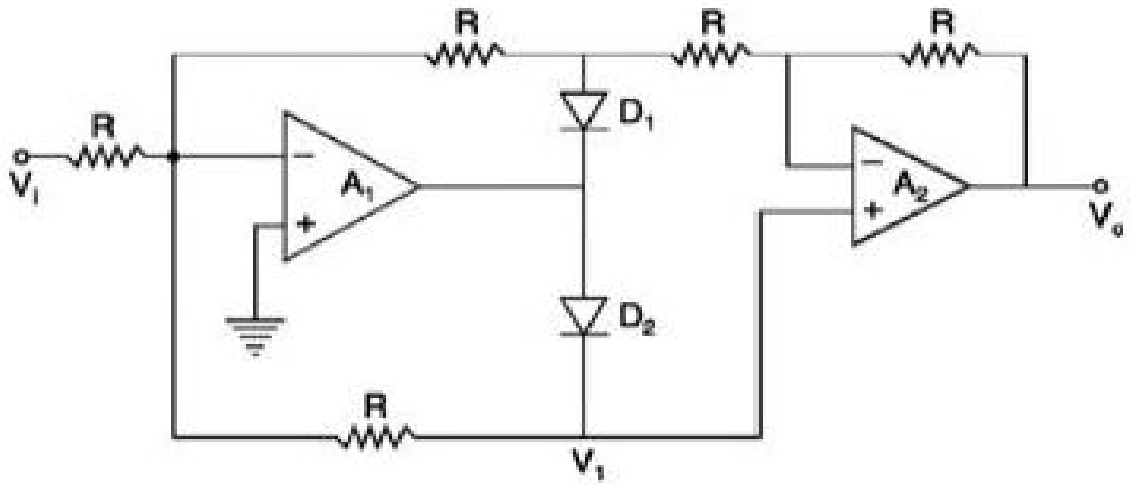


Vi > 0 v ; D1, D2 ON ;Vo = 0
Vi < 0 v ; D1, D2 OFF ;Vo = −(Rf/R1)*Vi

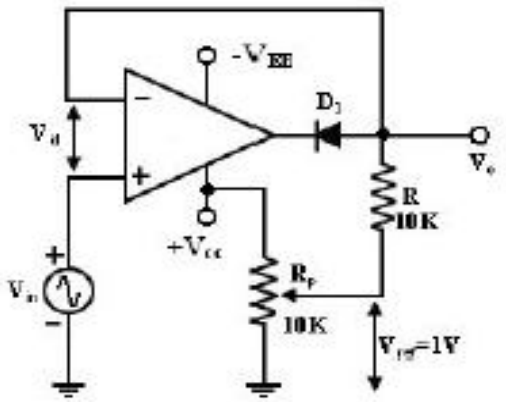
Full wave rectifier with an op amp

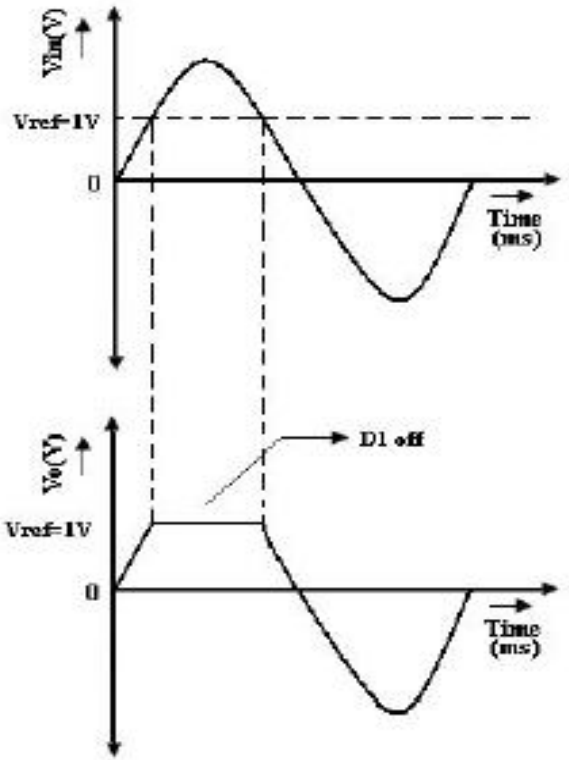


Full wave rectifier with two op-amps

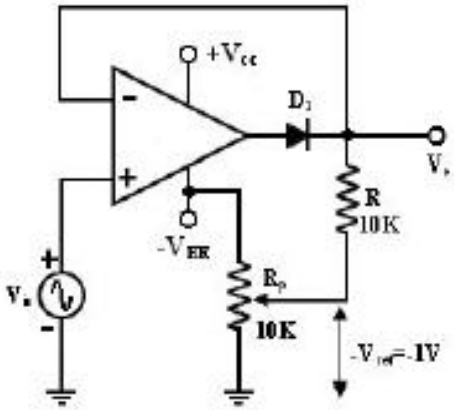


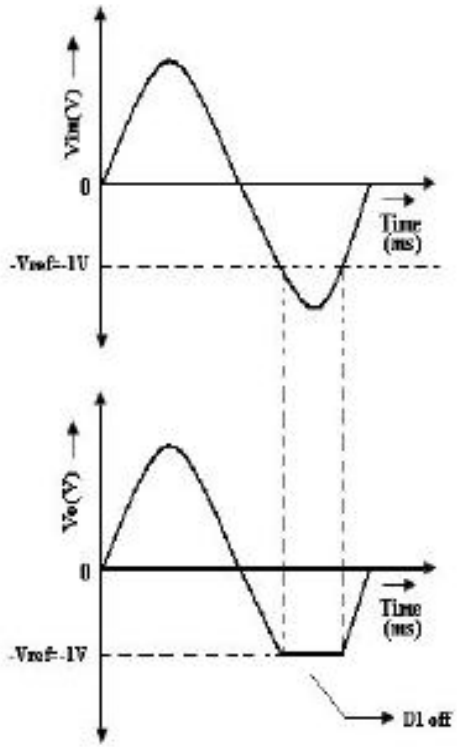
Positive and Negative Clipper:

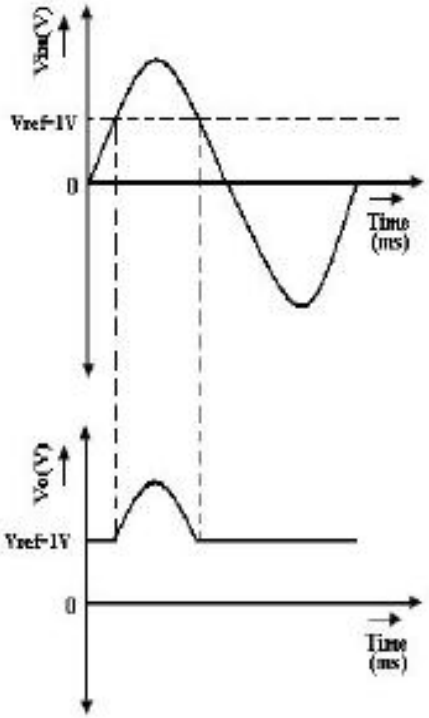




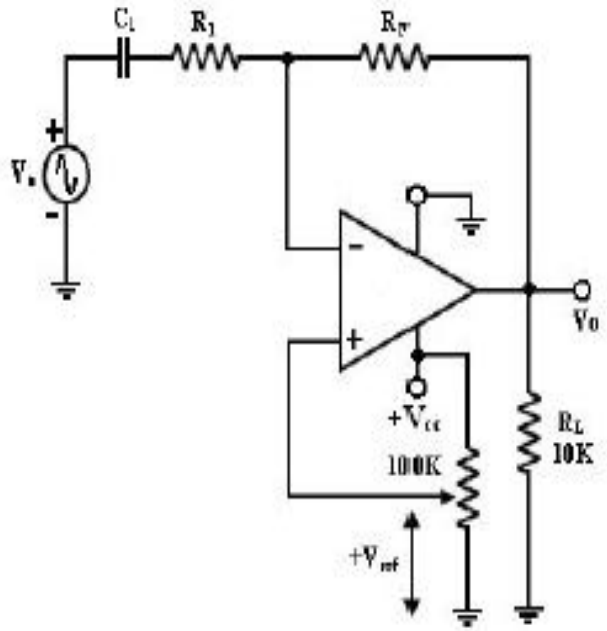
Negative Clipper:

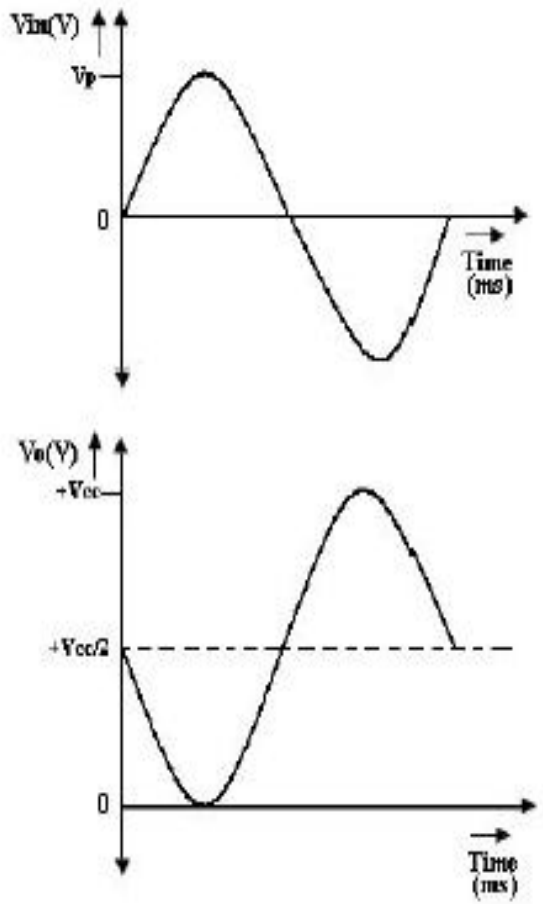






Positive and Negative Clampers:

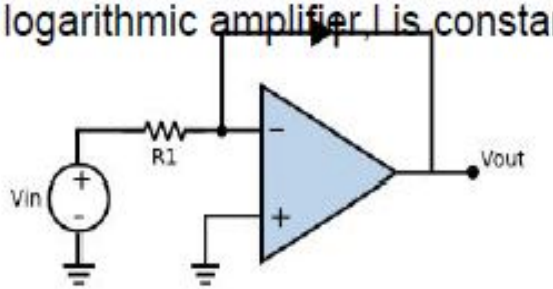




Logarithmic Amplifier

- Logarithmic amplifier gives the output proportional to the logarithm of input signal.

- If V_i is the input signal applied to a differentiator then output is $V_o = K*\ln(V_i)+I$
- where K is gain of logarithmic amplifier I is constant.



- The current equation of diode
- $I_d = I_{do}*(\exp (V/V_t)-1)$ ----------(1)
- where I_{do} is reverse saturation current,
- V is voltage applied across diode;
- V_t is the voltage equivalent of temperature
- $(0-V_{in})/R_1 + I_d = 0$
- $I_d = V_{in}/R_1$ --------(2)
- (1)=(2)

$I_{do}*(\exp (V/V_t)-1) = V_{in}/R_1$.

Assuming $\exp (V/V_t) >> 1$ i.e. $V>>V_t$ and

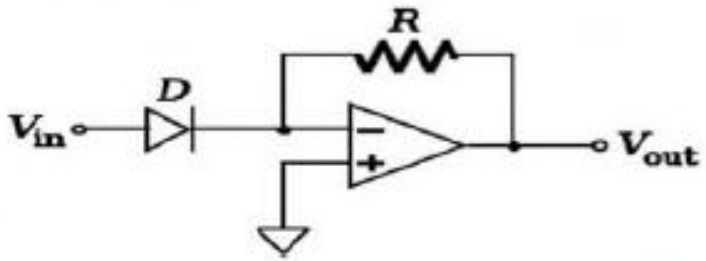
$V = -V_o$, $I_{do}*\exp (-V_o / V_t) = V_{in}/R_1$.

Applying Antilog on both sides we get

$V_o = -V_t * \ln (V_{in}/(R_1*I_{do}))$.

Anti log amplifier

- Anti log amplifier is one which provides output proportional to the anti log i.e. exponential to the input voltage.
- If V_i is the input signal applied to a Anti log amplifier then the output is $V_o=K^*\exp(a^*V_i)$ where K is proportionality constant, a is constant.



The current equation of diode is given as $I_d = I_{do}^*(\exp (V/V_t)-1)$

I_{do} is reverse saturation current,

V is voltage applied across diode;

V_t is the voltage equivalent of temperature

Applying KCL at inverting node of opamp

$$I_d = (0-V_o)/R = I_o^*(\exp (V_{in}/V_t)) \text{ (assumed } V_{in}/V_t >> 1)$$

$$V_o = -I_o^*R^*(\exp (V_{in}/V_t)).$$

Filter

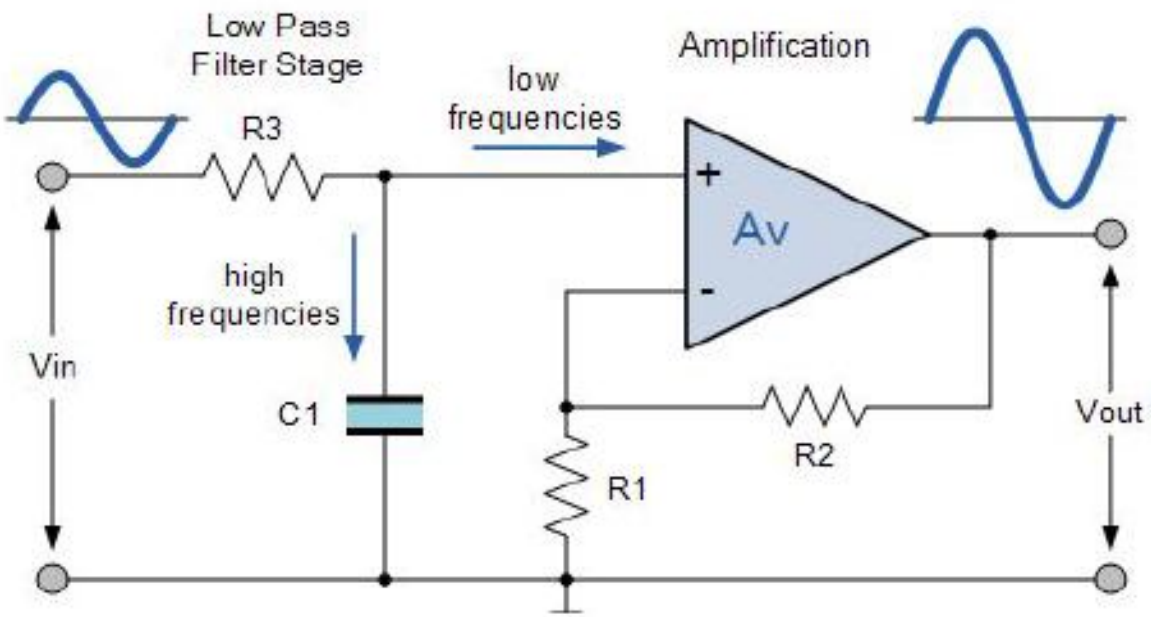
- Filter is a frequency selective circuit that passes signal of specified Band of frequencies and
- attenuates the signals of frequencies outside the band
- **Type of Filter**
- 1. Passive filters
- 2. Active filters

- **Passive filters**
- Passive filters works well for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive.
- For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q,resulting in high power dissipation
- **Active filters**
- Active filters used op- amp as the active element and resistors and capacitors as passive elements.
- By enclosing a capacitor in the feed back loop , inductor less active filters can be obtained

- Active filters use op-amp(s) and RC components.
- Advantages over passive filters:
  - op-amp(s) provide gain and overcome circuit losses
  - increase input impedance to minimize circuit loading
  - higher output power
  - sharp cutoff characteristics **some commonly used active filters**

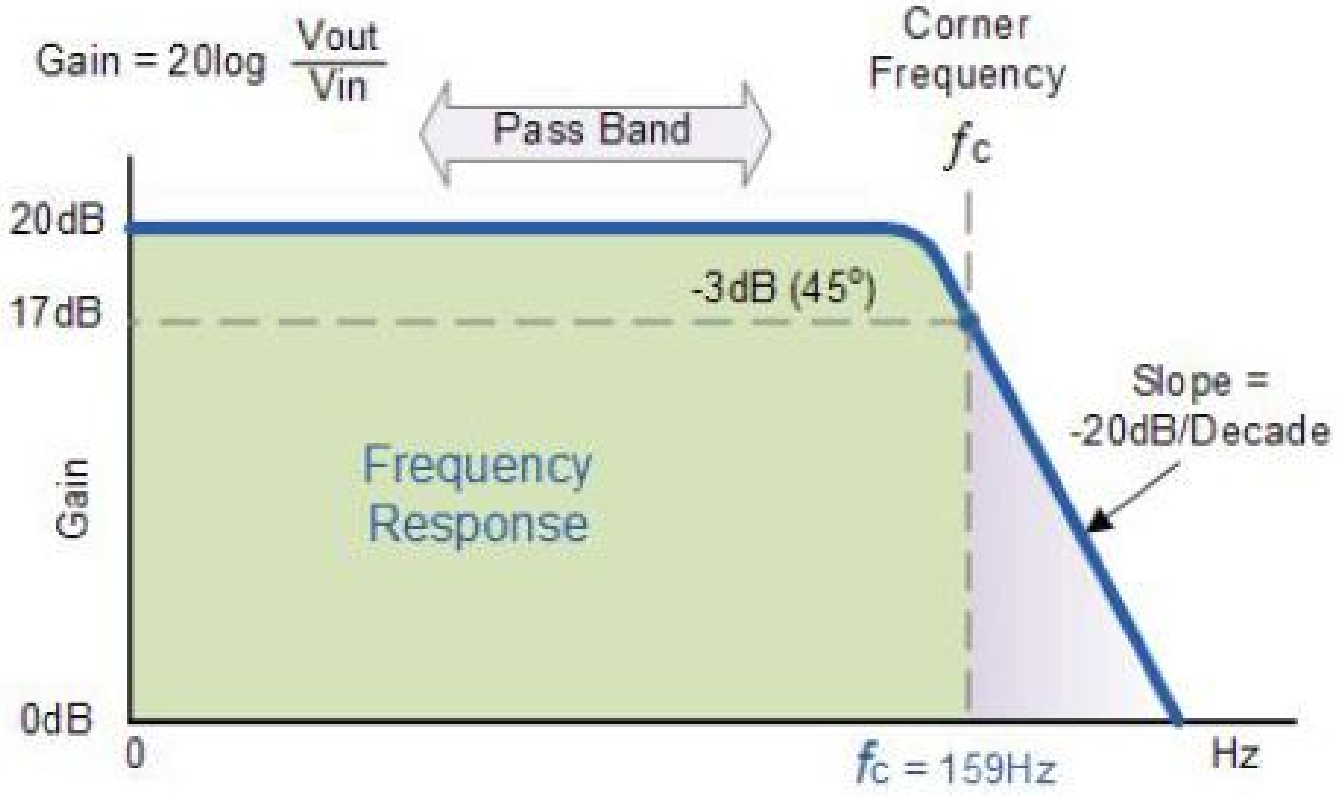
1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter

I order Active LPF

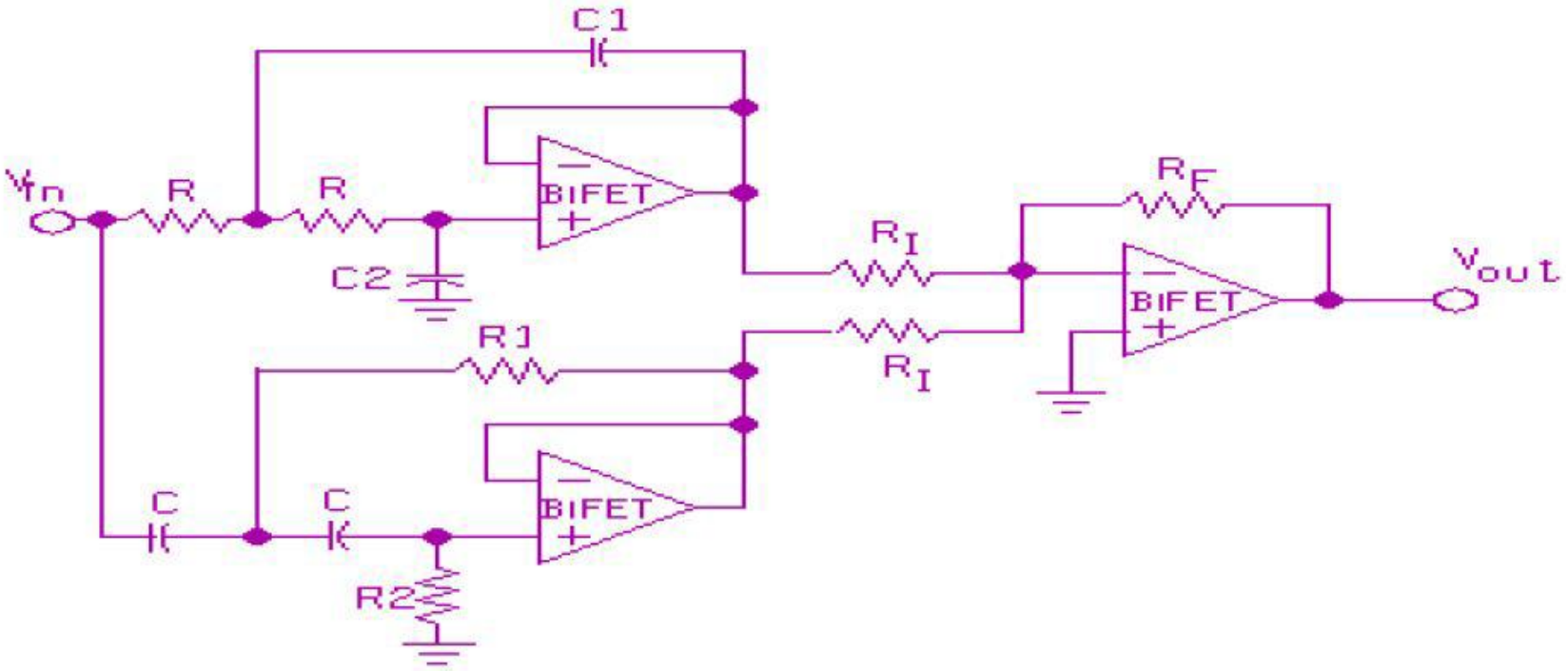


Gain of a first-order low pass filter

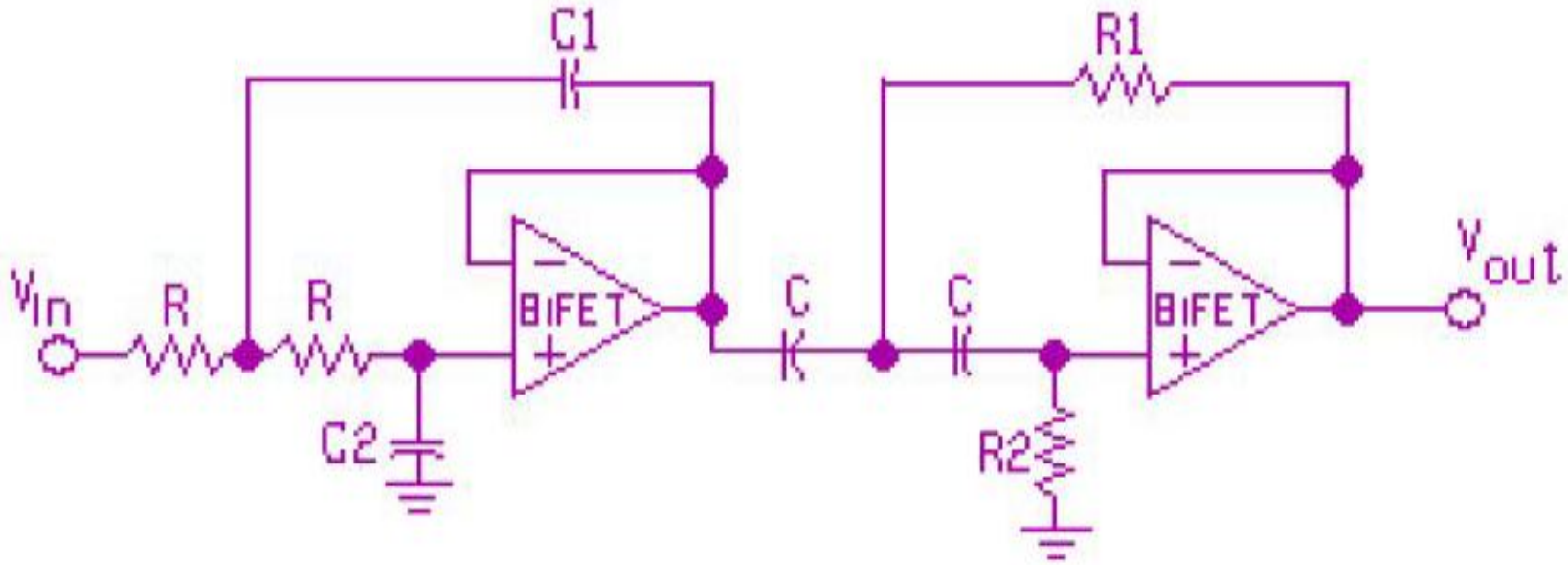
$$Voltage\ Gain,\ (Av) = \frac{Vout}{Vin} = \frac{A_F}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$


Gain = 20log Vout/Vin
Pass Band
Corner Frequency
fc
20dB
17dB
-3dB (45°)
Slope = -20dB/Decade
Gain
Frequency Response
0dB
0
fc = 159Hz
Hz

Wide BPF



A *broadband* BPF can be obtained by combining a LPF and a HPF



Multivibrators

- Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi- stable depending on the type of multivibrator

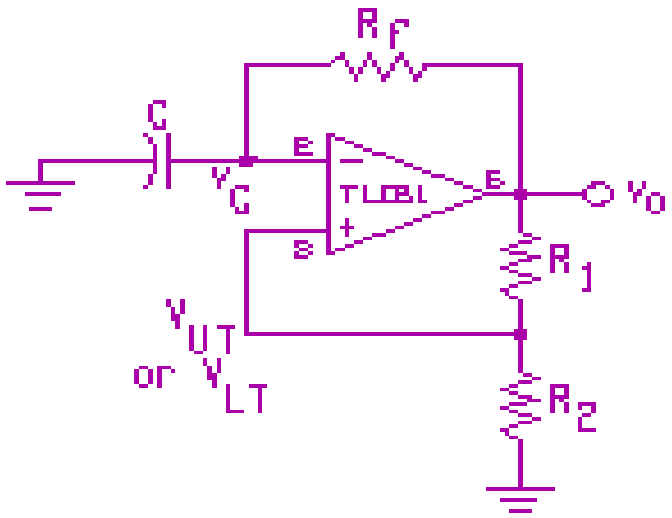
Monostable Multivibrator

- Monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state. Application of a trigger causes a change to the quasi-stable state.An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state

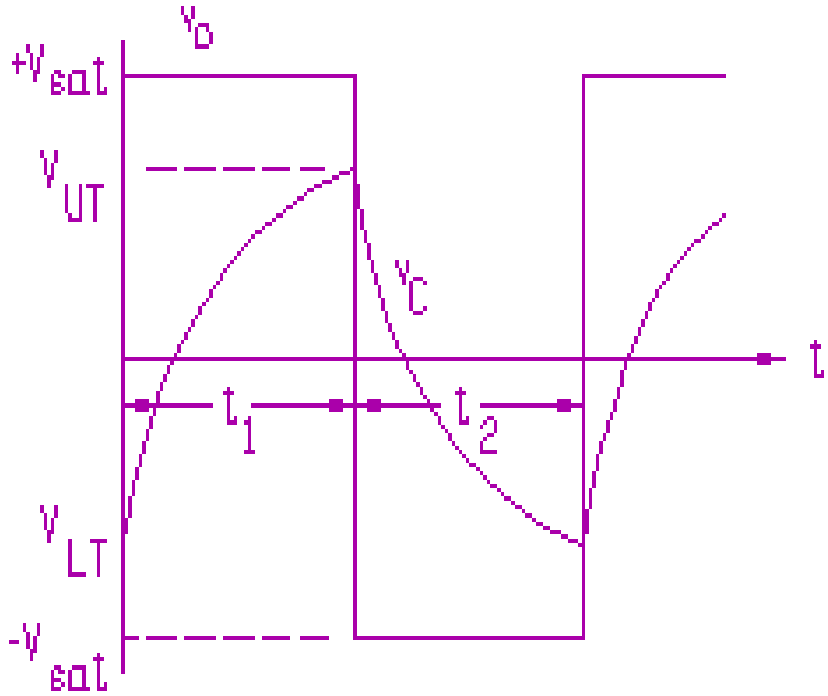
Astable Multivibrator

Astable multivibrator is a free running oscillator having two quasi- stable states. Thus, there is oscillations between these two states and no external signal are required to produce the change in state

Astable Multivibrator or Relaxation Oscillator



Circuit



Output waveform

Equations for Astable Multivibrator

$$V_{UT} = \frac{+V_{sat} R_2}{R_1 + R_2}; \quad V_{LT} = \frac{-V_{sat} R_2}{R_1 + R_2}$$

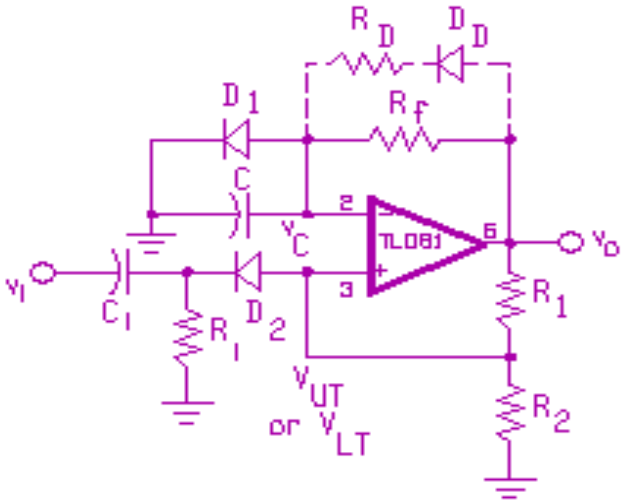
Assuming
$|+V_{sat}| = |-V_{sat}|$

$$T = t_1 + t_2 = 2\tau \ln\left(\frac{R_1 + 2R_2}{R_1}\right)$$

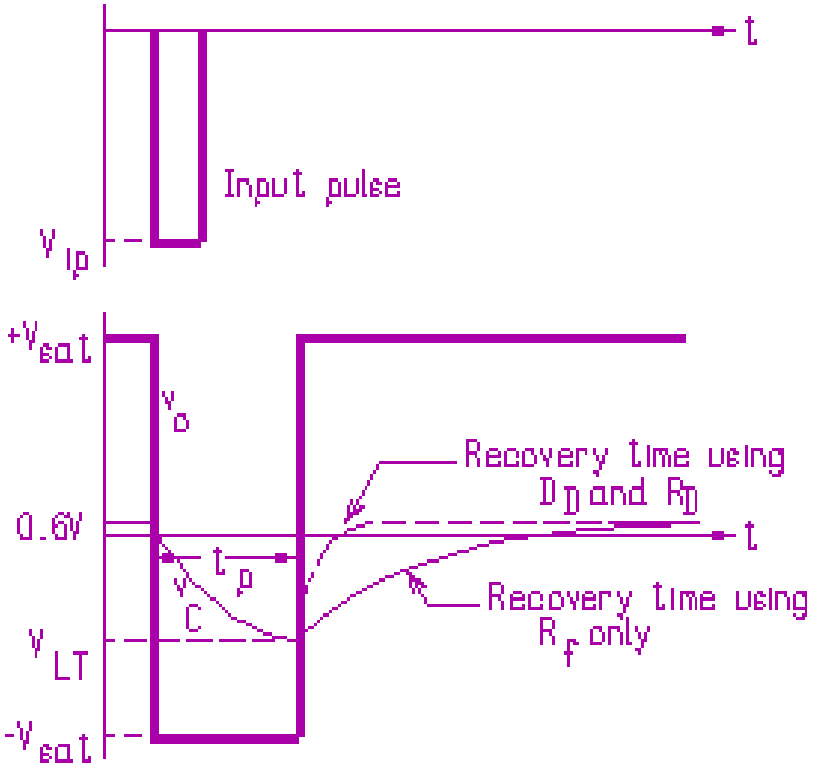
If R_2 is chosen to be $0.86R_1$, then $T = 2R_fC$ and

$$f = \frac{1}{2R_f C}$$

Monostable (One-Shot) Multivibrator



Circuit



Waveforms

Notes on Monostable Multivibrator

- Stable state: $v_o = +V_{sat}$, $V_C = 0.6$ V
- Transition to timing state: apply a -ve input pulse such that $|V_{ip}| > |V_{UT}|$; $v_o = -V_{sat}$.
- Timing state: C charges negatively from 0.6 V through R_f. Width of timing pulse is:
  - If we pick $R_2 = R_1/5$, then $t_p = R_fC/5$.
  - Recovery state: $v_o = +V_{sat}$; circuit is not ready for retriggering until $V_C = 0.6$ V. To speed up the recovery time, R_D (= $0.1R_f$) & C_D can be added.

Wien Bridge Oscillator

- The Wien bridge oscillator is essentially a feedback amplifier in which the Wien bridge serves as the phase-shift network. The Wien bridge is an ac bridge, the balance of which is achieved at one particular frequency.

- The basic Wien bridge oscillator is shown in Fig. 1-2. as can be seen. the Wien bridge oscillator consists of a Wien bridge and an operational amplifier represented by the triangular symbol. Operational amplifiers are integrated circuit amplifiers and have high-voltage gain, high input impedance, and low output impedance. The condition for balance for an ac bridge is

Cont'd

- The basic Wien bridge oscillator is shown in Fig. 1-2. as can be seen. the Wien bridge oscillator consists of a Wien bridge and an operational amplifier represented by the triangular symbol. Operational amplifiers are integrated circuit amplifiers and have high-voltage gain, high input impedance, and low output impedance. The condition for balance for an ac bridge is

$Z_1 Z_4 = Z_2 Z_3$ **1-2)**

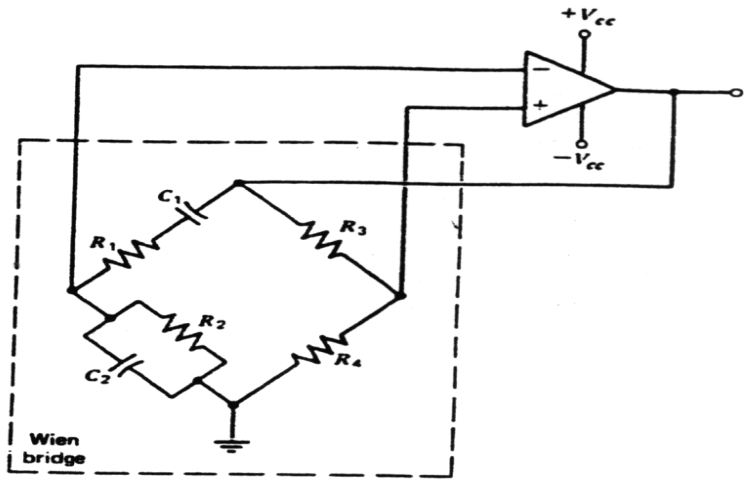


Fig. 1-2 Wien bridge oscillator.

Cont'd

Where

$$Z_1 = R_1 - j/\omega C_1$$

$$Z_2 = \frac{R_2(-j/\omega C_2)}{R_2 - j/\omega C_2} = \frac{-jR_2}{-j + R_2\omega C_2}$$

$Z_3 = R_3$
$Z_4 = R_4$

Substituting the appropriate expressions into Eq. 1-2 yields

$$\left(R_1 - \frac{j}{\omega C_1}\right)R_4 = \left(\frac{-jR_2}{-j + R_2\omega C_2}\right)R_3 \qquad (1\text{-}3)$$

Cont'd

- if the bridge is balanced both the magnitude and phase angle of the impedances must be equal. These conditions are best satisfied by equating real terms and imaginary terms. Separating and equating the real terms in Eq. 1-3 yields.

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \qquad (1\text{-}4)$$

Separating and equating imaginary terms in Eq. 1-3 yields

$$\omega C_1 R_2 = \frac{1}{\omega C_2 R_1} \qquad (1\text{-}5)$$

Cont'd

- Where $\omega = 2\pi f$. Substituting for to in Eq. 1-5, we can obtain an expression for frequency which is

$$f = \frac{1}{2\pi \left(C_1 R_1 C_2 R_2\right)^{1/2}} \qquad (1\text{-}6)$$

- If $C_1 = C_2 = C$ and $R_1 = R_2 = R$ then Eq. 1-4 simplifies yield

$$\frac{R_3}{R_4} = 2 \qquad (1\text{-}7)$$

Cont'd

- and from Eq. 1-6 we obtain

$$f = \frac{1}{2\pi RC} \qquad (1\text{-}8)$$

Where

f = frequency of oscillation of the circuit in Hertz

C = capacitance in farads

R = resistance in ohms

Phase Shift Oscillator

- The second audio-oscillator circuit of interest is the phase-shift oscillator.
- The phase-shift network for the phase-shift oscillator, is an RC network made up of equal-value capacitors and resistors connected in cascade. Each of the three *RC* stages shown provides a 60^{o} phase shift. with the total phase shift equal to the required 180^{o}.

Cont'd

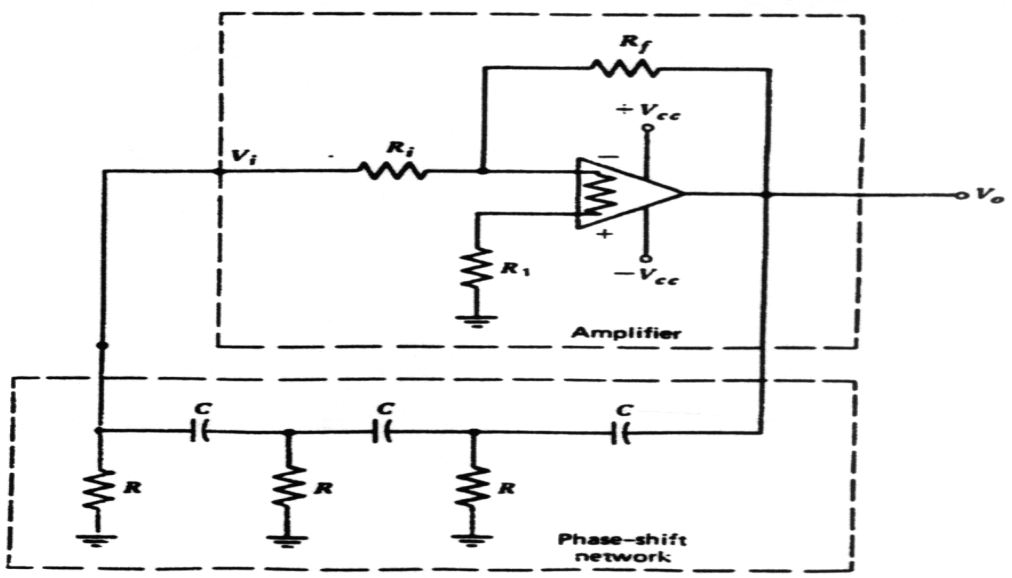


Fig.1-4 Basic phase-shift oscillator circuit.

Cont'd

- The phase-shift oscillator is analyzed by ignoring any minimal loading of the phase-shift network by the amplifier. By applying classical network analysis techniques, we can develop an expression for the feedback factor in terms of the phase-shift network components.
- The result is given in equation 1.9 as

$$\beta = \frac{V_i}{V_o} = \frac{1}{1 - \frac{5}{(\omega RC)^2} + j\left[\frac{1}{(\omega RC)_3} - \frac{6}{\omega RC}\right]}$$

Cont'd

- If the phase shift of the feedback network satisfies the 180^o phase-shift requirements, the imaginary components of Eq. 1-9 must be equal to zero or

$$\frac{1}{(\omega RC)^3} - \frac{6}{\omega RC} = 0$$

Cont'd

- The frequency of oscillation for the circuit can be determined by substituting $2\pi f$ for ω in Eq. 1-10 and solving for the frequency. The result is

$$f = \frac{1}{2\sqrt{6\pi RC}} \quad (1\text{-}11)$$

Cont'd

- We can express Eq. 1-11 as

$$2\pi f = \frac{1}{\sqrt{6RC}} \qquad (1\text{-}12)$$

or

$$\omega = \frac{1}{\sqrt{6RC}} \qquad (1\text{-}13)$$

substituting for in Eq. 10-9, we obtain

$$\beta = \frac{V_i}{V_2} = \frac{1}{1 - 5/(1/6) + j(6\sqrt{6} - 6\sqrt{6}} \qquad (1\text{-}14)$$

Cont'd

- or

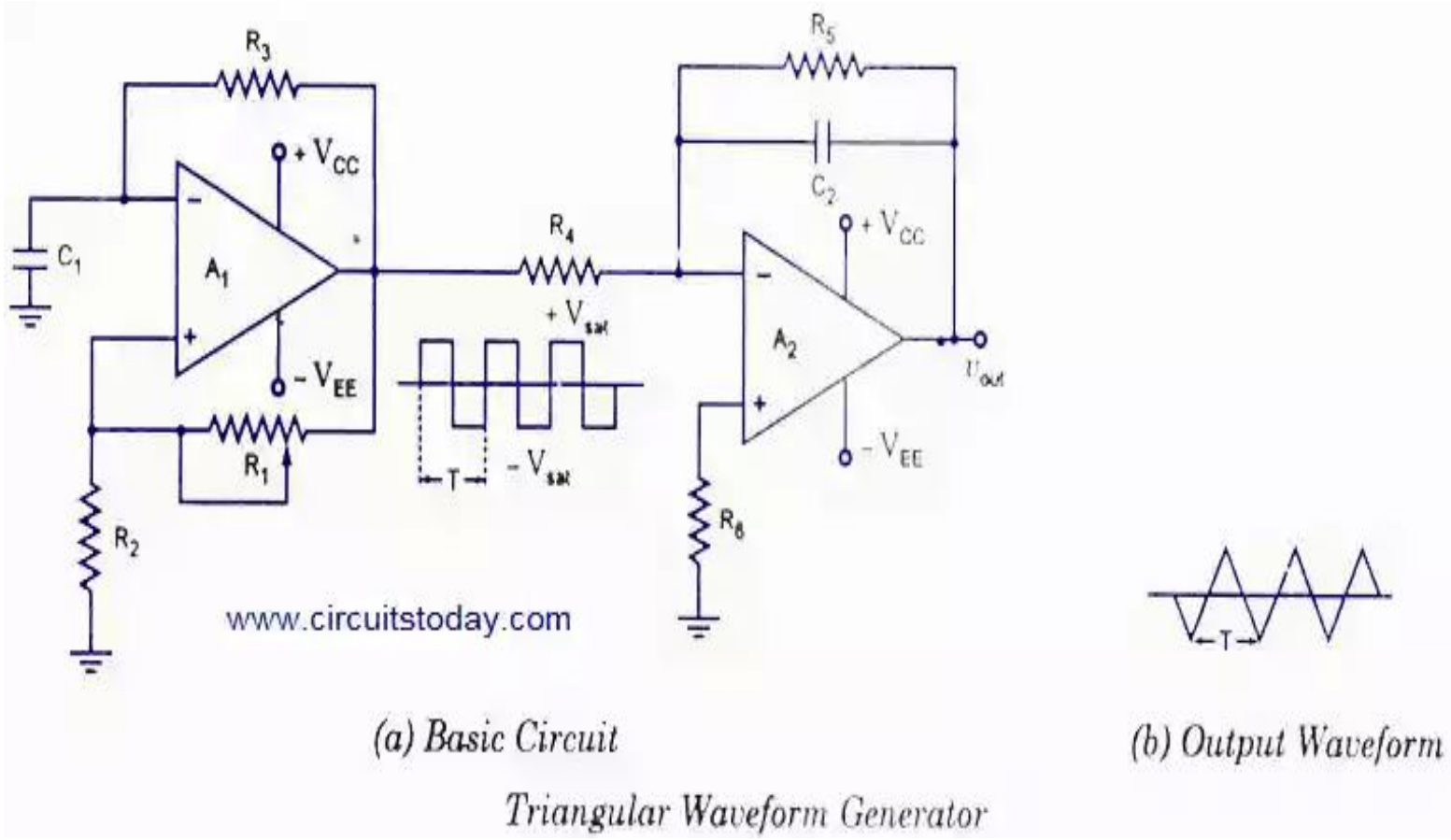
$$\beta = \frac{V_i}{V_o} = \frac{1}{1 - 5\ x\ 6} = \frac{1}{29} \quad (1\text{-}15)$$

Rewriting Eq. 1-15, we see that

$$V_o = -29V_i$$

which means that the gain of the amplifier must be at least 29 if the circuit is to sustain oscillation.

TRIANGULAR WAVE GENERATOR



(a) Basic Circuit

(b) Output Waveform

Triangular Waveform Generator

TRIANGULAR WAVE GENERATOR:-

- Triangular wave generator can be form by connecting an integrator to the square wave generator.
- This circuit requires dual op-amp,two capacitor and five resistors. For fix R1,R2,C be frequency of triangular wave depends on R
- As value of R is increase or decrease the frequency of triangular wave is increase or decrease.
- All though the amplitude of square wave form is constant the amplitude of triangular wave will increase or decrease with its frequency.
- The output of A1 is square wave which is given as an input to A2 as A2 act as an integrator. Its output is triangular wave form.

Analog Multiplier and PLL

UNIT–III

Introduction

- Nonlinear operations on continuous-valued analog signals are often required in instrumentation, communication, and control-system design.
- These operations include
  - rectification,
  - modulation,
  - demodulation,
  - frequency translation,
  - multiplication, and
  - division.
- In this chapter we analyze the most commonly used techniques for performing multiplication and division within a monolithic integrated circuit

Introduction

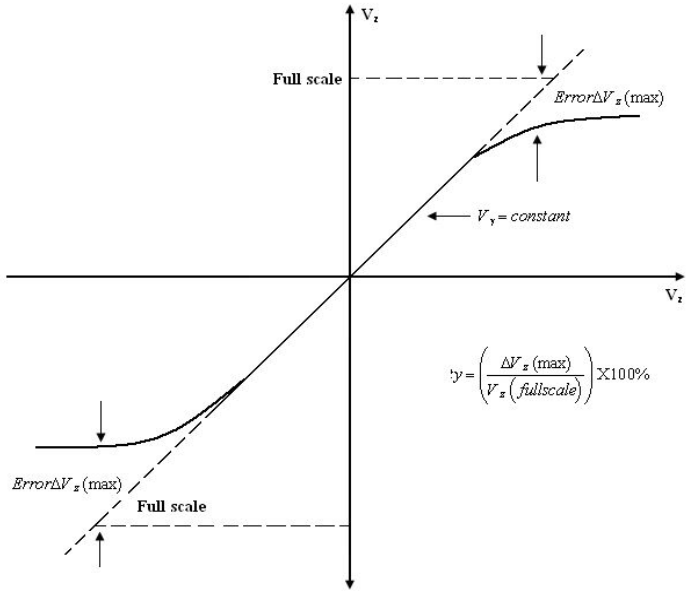
- In analog-signal processing the need often arises for a circuit that takes two analog inputs and produces an output proportional to their product.
- Such circuits are termed *analog multipliers*.
- In the following sections we examine several analog multipliers that depend on the exponential transfer function of bipolar transistors .

MULTIPLIERS

- A multiple produces an output V0 , which is proportional to the product of two inputs Vx and Vy.
  That is, V0 = K Vx Vy
- where K is the scaling factor that is usually maintained as (1/10) V-1
- There are various methods available for performing analog multiplication. Four of such techniques, namely,
- 1. Logarithmic summing technique
  2. Pulse height/width modulation Technique
  3. Variable trans conductance Technique
  4. Multiplication using Gilbert cell and
  5. Multiplication using variable trans conductance technique.

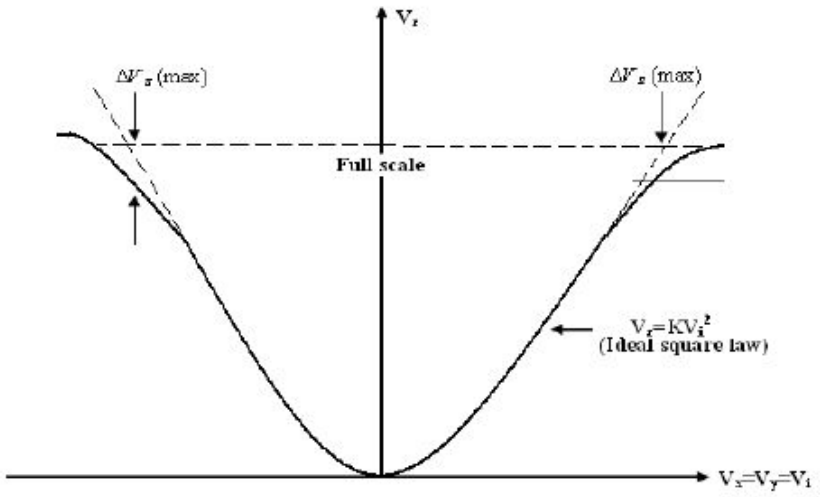
Terminologies associated voltage of the multiplier characteristics

- **Accuracy**:
  This specifies the derivation of the actual output from the ideal output, for any combination of X and Y inputs falling within the permissible operating range of the multiplier.
- **Linearity**:
  This defines the accuracy of the multiplier. It represents the maximum percentage derivation from the ideal straight line output. An error surface is formed by plotting the output for different combinations of X and Y inputs. The Linearity Error can be defined as the maximum absolute derivation of the error surface. This linearity error imposes a lower limit on the multiplier accuracy.



..CONTD

- **Squaring Mode Accuracy:**
  The Square – law curve is obtained with both the X and Y inputs connected together and applied with the same input signal. The maximum derivation of the output voltage from an ideal square – law curve expresses the squaring mode accuracy.



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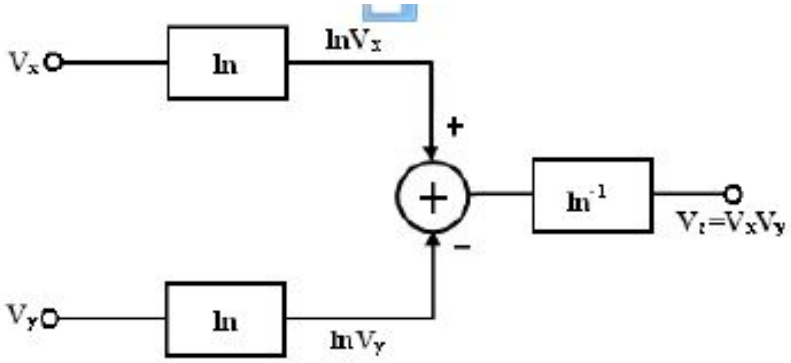
Bandwidth:
The Bandwidth indicates the operating capability of an analog multiplier at higher frequency values. Small signal 3 dB bandwidth defines the frequency f0 at which the output reduces by 3dB from its low frequency value for a constant input voltage. This is identified individually for the X and Y input channels normally.
The transconductance bandwidth represents the frequency at which the transconductance of the multiplier drops by 3dB of its low frequency value. This characteristics defines the application frequency ranges when used for phase detection or AM detection.
Quadrant:
The quadrant defines the applicability of the circuit for bipolar signals at its inputs. First – quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four quadrant device accepts two bipolar signals.

Logarithmic summing Technique:

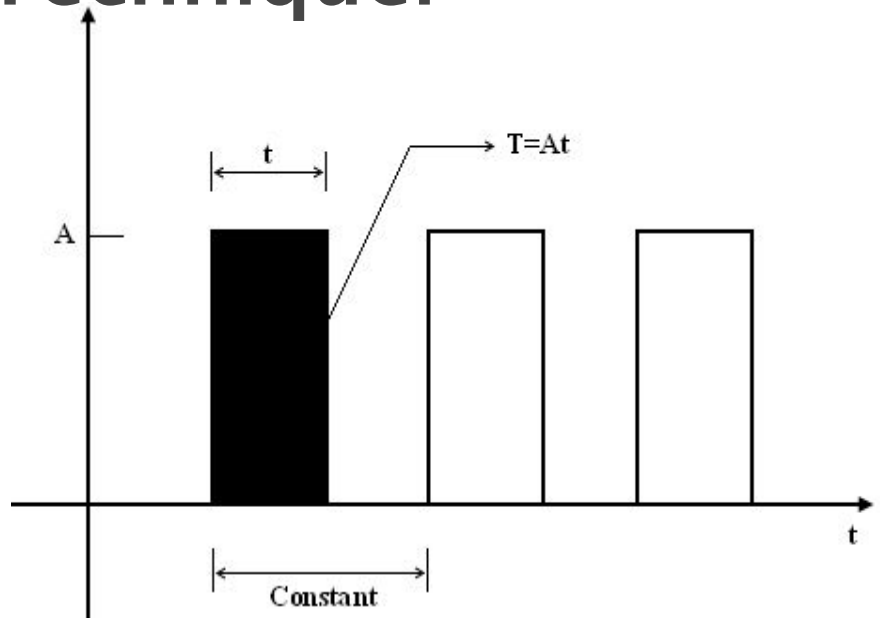
- This technique uses the relationship
  lnVx + lnVy =ln(VxVy)



➢Logarithmic multiplier has low accuracy and high temperature instability. This method is applicable only to positive values of Vx and Vy.

➢ this type of multiplier is restricted to one quadrant operation only.

Pulse Height/ Width Modulation Technique:



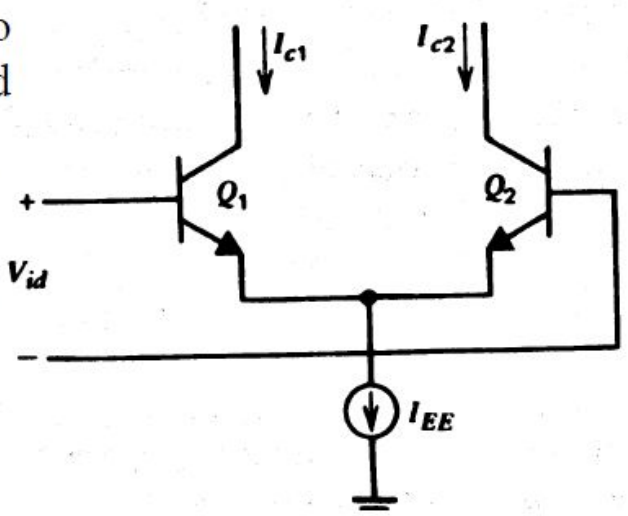
$$V_z = K_z T = K_z At = V_x V_y / K_x K$$

Multiplier using Emitter coupled Transistor pair

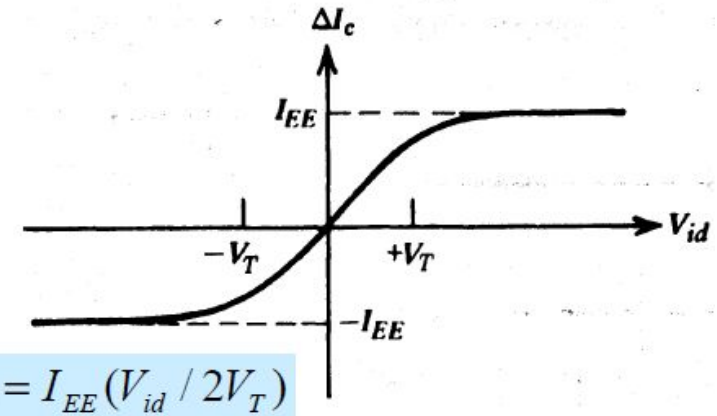
- The emitter-coupled pair, was shown in to produce output currents that were related to the differential input voltage by :

$$I_{c1} = \frac{I_{EE}}{1+\exp(-V_{id}/V_T)} \qquad I_{c2} = \frac{I_{EE}}{1+\exp(V_{id}/V_T)}$$

$$\Delta I_c = I_{c1} - I_{c2} = I_{EE}\tanh(V_{id}/2V_T)$$



- This relationship is plotted => and shows that the emitter-coupled pair by itself can be used as a primitive multiplier.



or assuming $(V_{id}/2V_T) << 1, \Rightarrow \Delta I_c = I_{EE}(V_{id}/2V_T)$

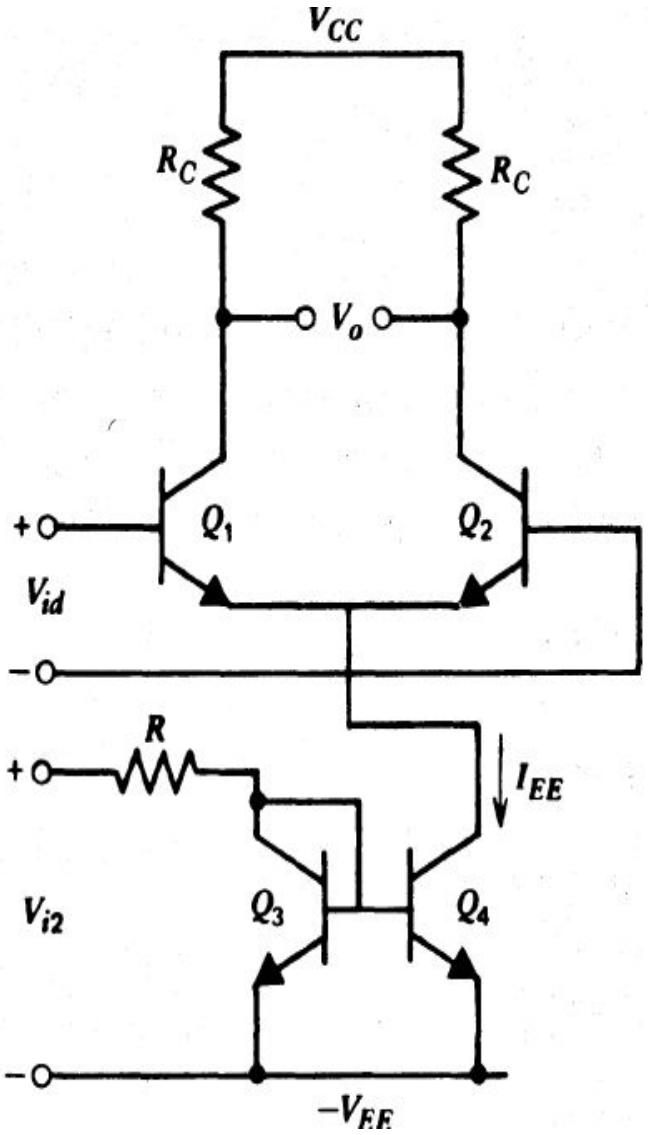
..CONTD

- The current I_{EE} is actually the bias current for the emitter-coupled pair.
- With the addition of more circuitry, we can make I_{EE} proportional to a second input signal.
- Thus we have

$$I_{EE} \cong K_o(V_{i2} - V_{BE(on)})$$

- The differential output current of the emitter-coupled pair can be calculated to give

$$\Delta I_c \cong \frac{K_o V_{id}(V_{i2} - V_{BE(on)})}{2V_T}$$

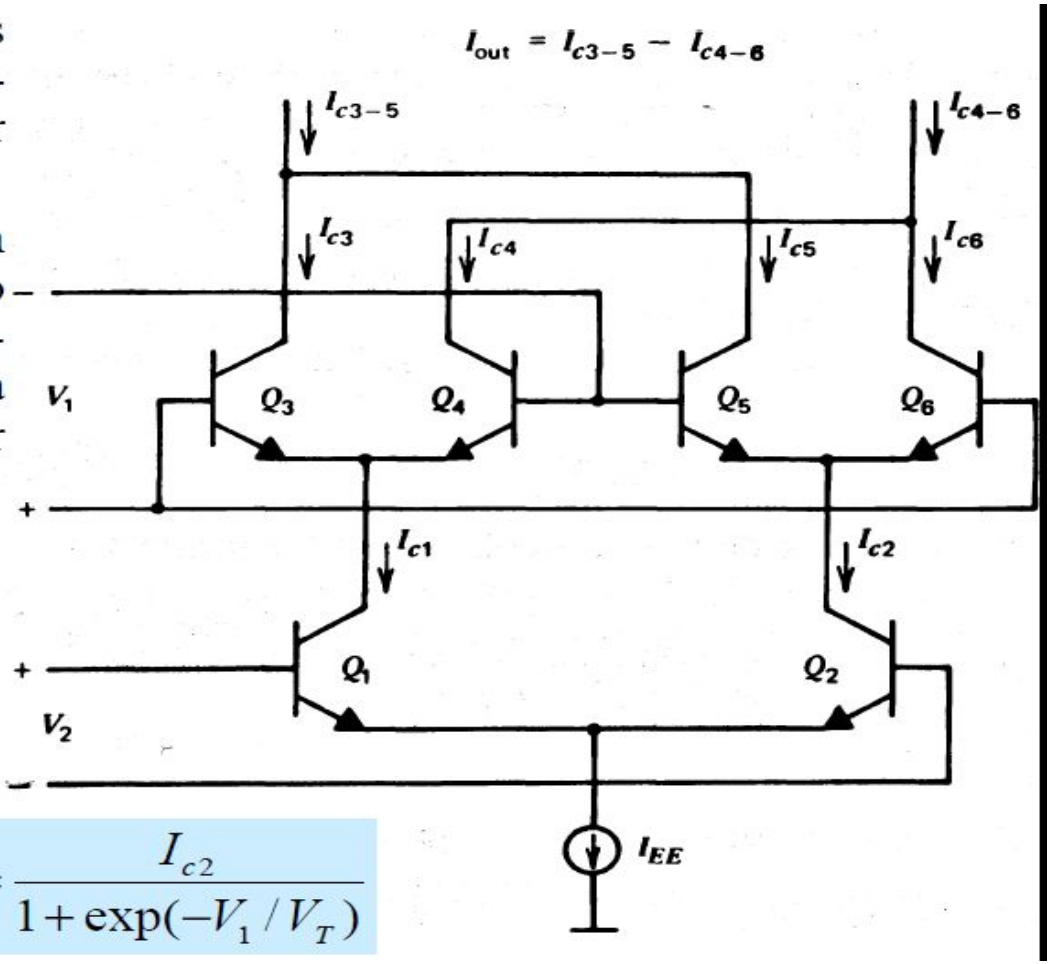


Two-Quadrant restriction

- Thus we have produced a circuit that functions as a multiplier under the assumption that *Vid* is small, and that *Vi2* is greater than $V_{BE(on)}$.
- The latter restriction means that the multiplier functions in only two quadrants of the *Vid* - *Vi2* plane, and this type of circuit is termed a two-quadrant multiplier.
- The restriction to two quadrants of operation is a severe one for many communications applications, and most practical multipliers allow four-quadrant operation.
- The Gilbert multiplier cell, shown, is a modification of the emitter-coupled cell, which allows four-quadrant multiplication.

Gilbert multiplier cell

- The Gilbert multiplier cell is the basis for most integrated-circuit balanced multiplier systems.
- The series connection of an emitter-coupled pair with two cross-coupled, emitter-coupled pairs produces a particularly useful transfer characteristic,.



$$I_{c3} = \frac{I_{c1}}{1+\exp(-V_1/V_T)}$$

$$I_{c4} = \frac{I_{c1}}{1+\exp(V_1/V_T)}$$

$$I_{c5} = \frac{I_{c2}}{1+\exp(V_1/V_T)}$$

$$I_{c6} = \frac{I_{c2}}{1+\exp(-V_1/V_T)}$$

- The two currents I_{c1} and I_{c2} are related to V2

$$I_{c1} = \frac{I_{EE}}{1+\exp(-V_2/V_T)} \qquad I_{c2} = \frac{I_{EE}}{1+\exp(V_2/V_T)}$$

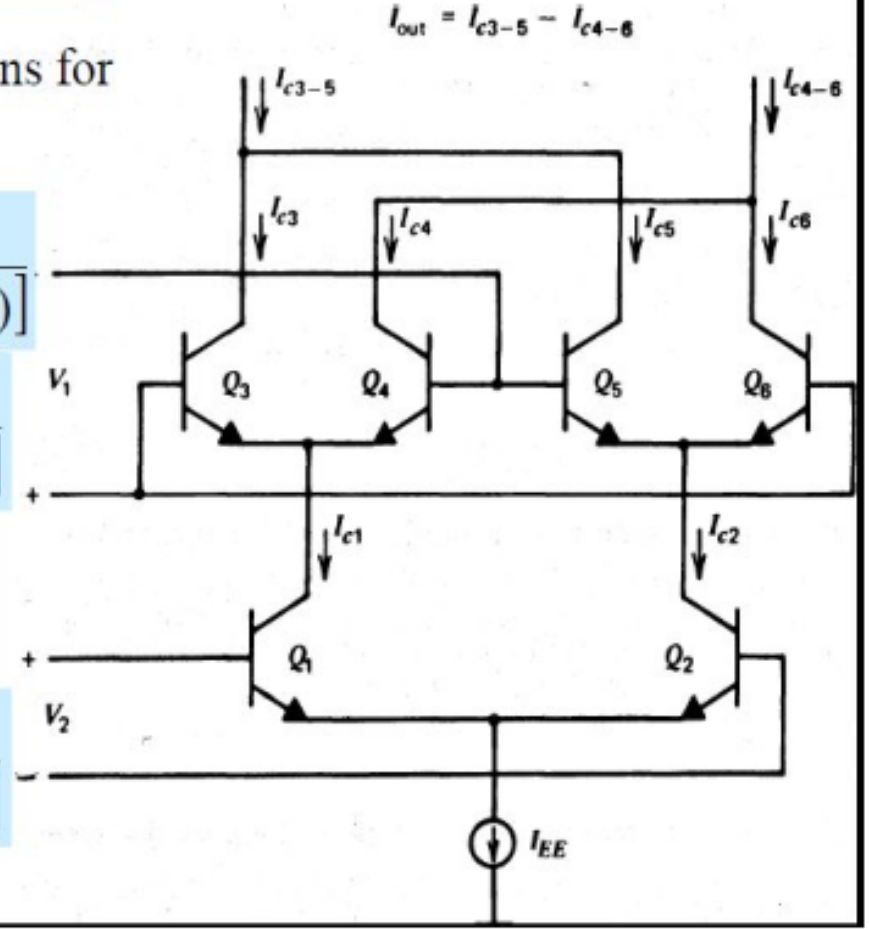
- Substituting I_{c1} and I_{c2} in expressions for
- I_{c3} , I_{c4}, I_{c5} and I_{c6} get :

$$I_{c3} = \frac{I_{EE}}{[1+\exp(-V_1/V_T)][1+\exp(-V_2/V_T)]}$$

$$I_{c4} = \frac{I_{EE}}{[1+\exp(V_1/V_T)][1+\exp(-V_2/V_T)]}$$

$$I_{c5} = \frac{I_{EE}}{[1+\exp(V_1/V_T)][1+\exp(V_2/V_T)]}$$

$$I_{c6} = \frac{I_{EE}}{[1+\exp(-V_1/V_T)][1+\exp(V_2/V_T)]}$$



- The differential output current is then given by

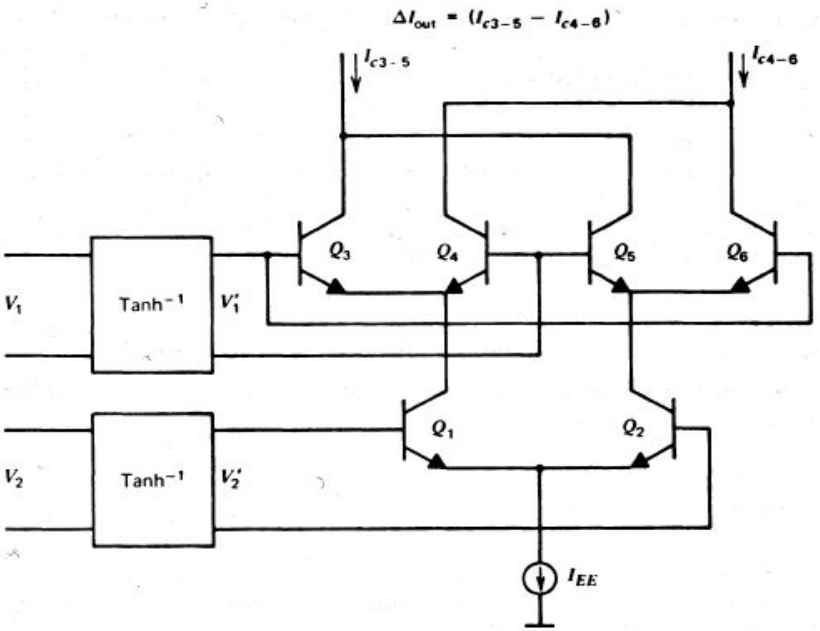
$$\Delta I = I_{c3-5} - I_{c4-6} = I_{c3} + I_{c5} - (I_{c4} + I_{c6}) = (I_{c3} - I_{c6}) - (I_{c4} - I_{c5}) =$$
$$= I_{EE} \tanh(V_1 / 2V_T) \tanh(V_2 / 2V_T)$$

- The dc transfer characteristic, then, is the product of the hyperbolic tangent of the two input voltages. The are three main application of Gilbert cell depending of the V1 an V2 range:
- (1) If $V_1 < V_T$ and $V_2 < V_T$ then : $\tanh(V_{1,2} / 2V_T) \cong V_{1,2} / 2V_T$ and it woks as multiplier
- (2) If one of the inputs of a signal that is large compared to V_T, this effectively multiplies the applied small signal by a square wave, and acts as a modulator.
- (3) If both inputs are large compared to V_T, and all six transistors in the circuit behave as nonsaturating switches. This is useful for the detection of phase differences between two amplitude-limited signals, as is required in phase-locked loops, and is sometimes called the phase-detector mode.

Gilbert cell as Multiplier

(1) If $V_1 < V_T$ and $V_2 < V_T$ then : $\tanh(x) = x + x^3/3 + ... \cong x$

- Thus for small-amplitude signals, the circuit performs an analog multiplication. Unfortunately, the amplitudes of the input signals are often much larger than V_T
- An alternate approach is to introduce a nonlinearity that predistorts the input signals to compensate for the hyperbolic tangent transfer characteristic of the basic cell.
- The required nonlinearity is an inverse hyperbolic tangent characteristic



Pre-warping circuit - inverse hyperbolic tangent

- We assume for the time being that the circuitry within the box develops a differential output current that is linearly related to the input voltage 7i. Thus

$$I_1 = I_{o1} + K_1 V_1 \text{ and } I_2 = I_{o1} - K_1 V_1$$

- Here I_{o1} is the dc current that flows in each output lead if $V1$ is equal to zero, and K1 is the transconductance of the voltage-to-current converter

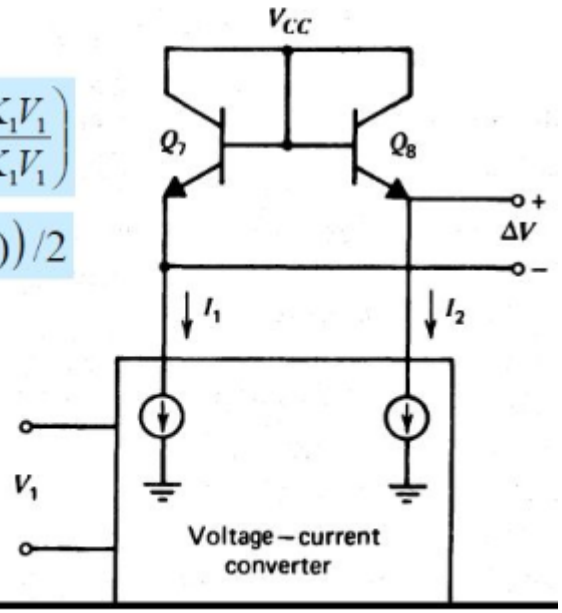
- The differential voltage developed across the two diode-connected transistors is

$$\Delta V = V_T \ln\left(\frac{I_{o1} + K_1 V_1}{I_s}\right) - V_T \ln\left(\frac{I_{o1} - K_1 V_1}{I_s}\right) = V_T \ln\left(\frac{I_{o1} + K_1 V_1}{I_{o1} - K_1 V_1}\right)$$

- Using the identity: $\tanh^{-1} x = \ln\left((1+x)/(1-x)\right)/2$

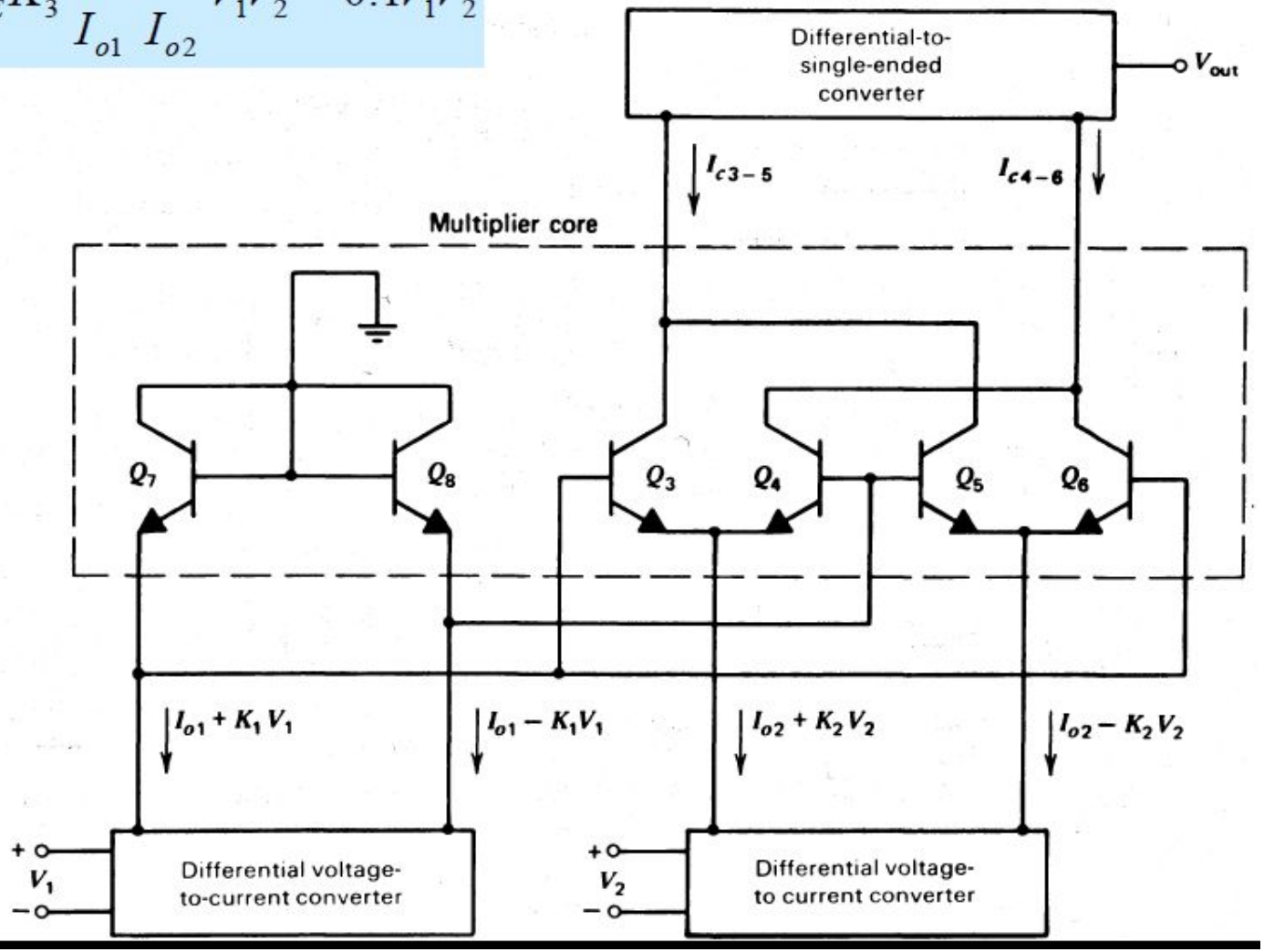
- We get $$\Delta V = 2V_T \tanh^{-1}\left(\frac{K_1 V_1}{I_{o1}}\right)$$

- And finally $$\Delta I = I_{EE}\left(\frac{K_1 V_1}{I_{o1}}\right)\left(\frac{K_2 V_2}{I_{o2}}\right)$$

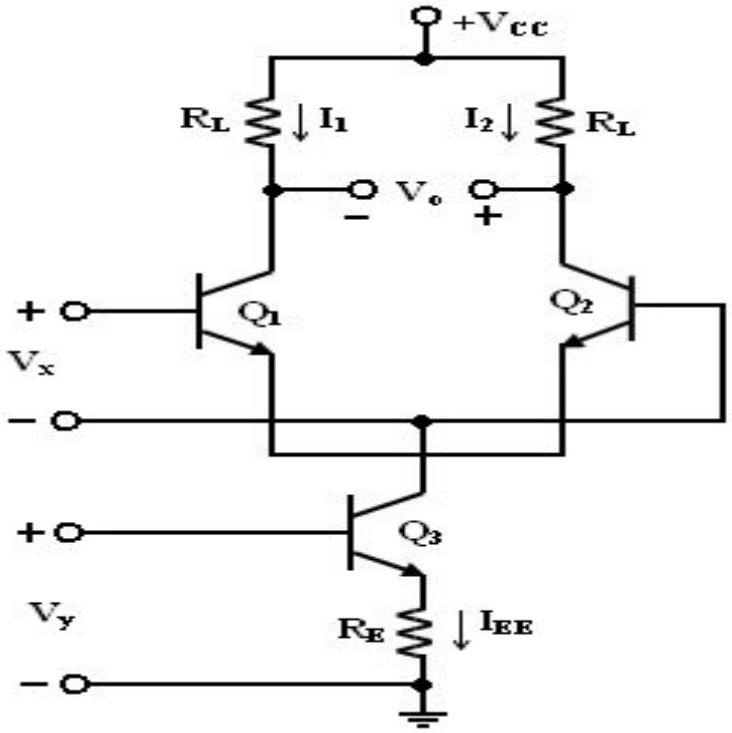


Complete Analog Multiplier

$$V_{out} = I_{EE} K_3 \frac{K_1}{I_{o1}} \frac{K_2}{I_{o2}} V_1 V_2 = 0.1 V_1 V_2$$



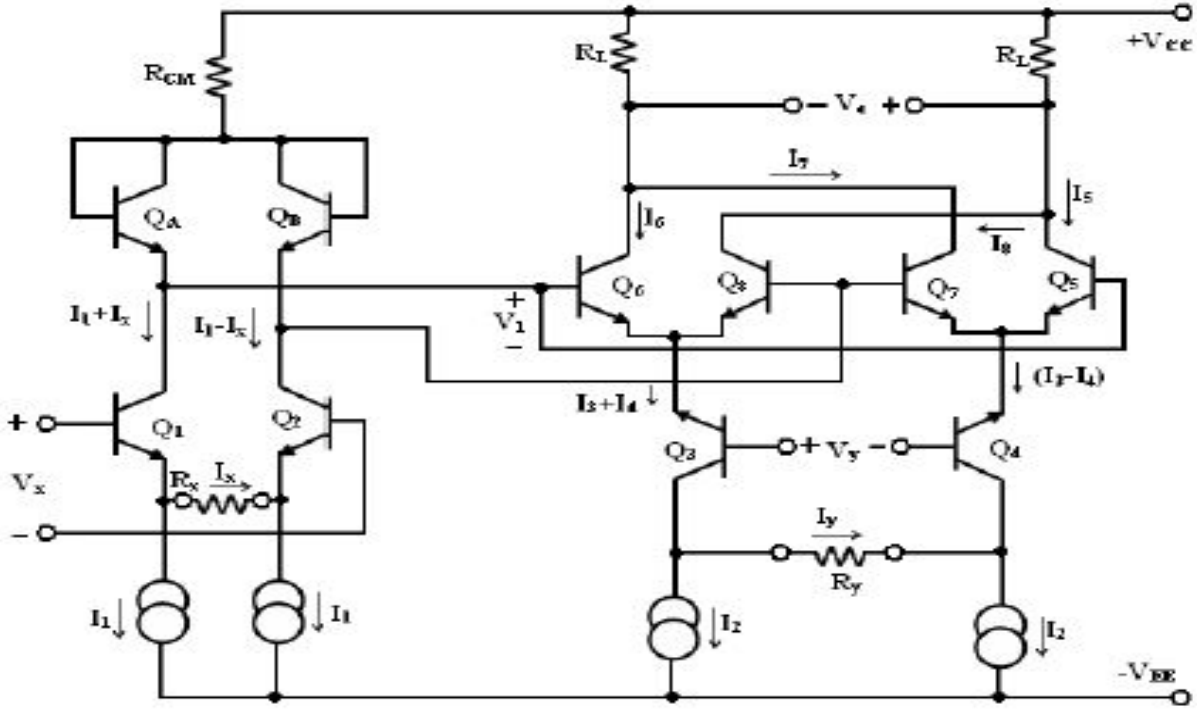
Variable Transconductance Technique:



$V0 = gm\ R_L Vx = (Vy/VTRE)VxRL$
$=(Vx\ Vy\ R_L/V_t\ R_e$

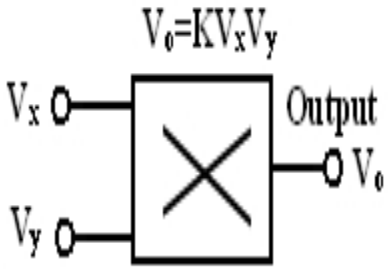
Four Quadrant Variable transconductance multiplier

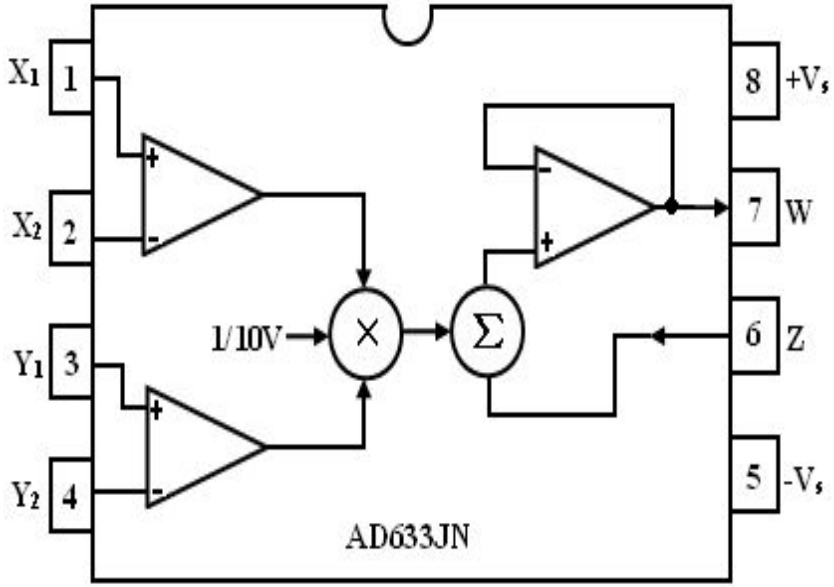
- The four quadrant operation indicates that the output voltage is directly proportional to the product of the two input voltages regardless of the polarity of the inputs and such multipliers can be operated in all the four quadrants of operation



Analog Multiplier ICs

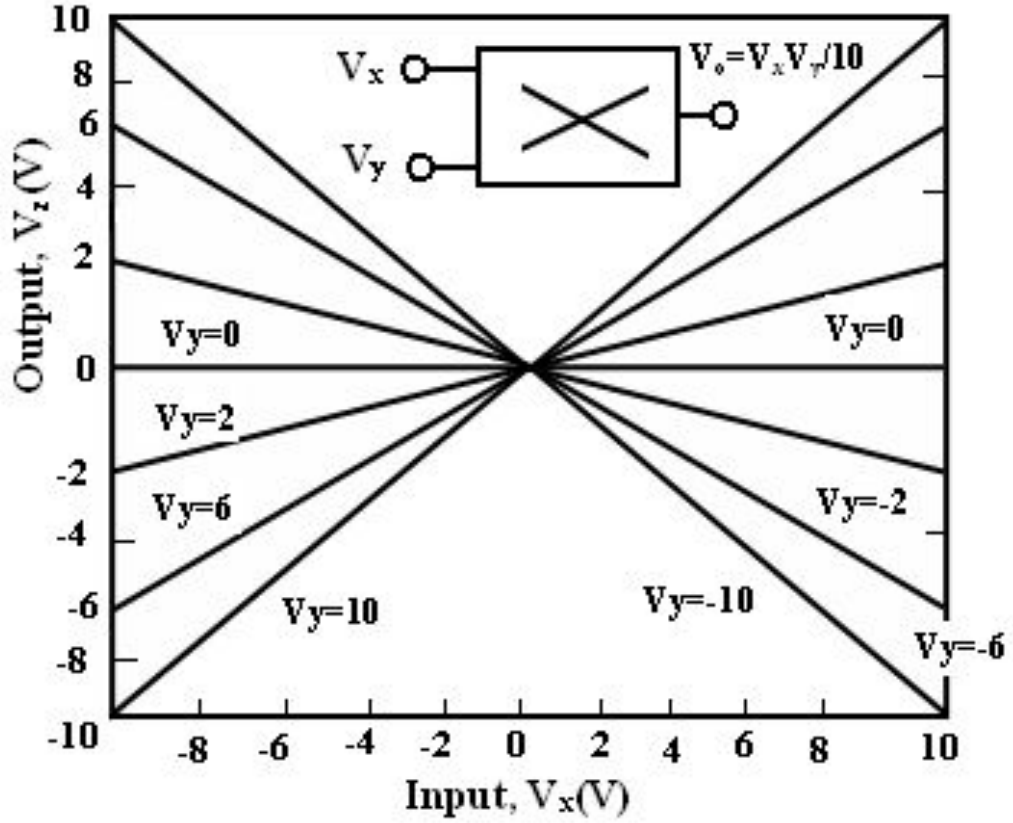
- Analog multiplier is a circuit whose output voltage at any instant is proportional to the product instantaneous value of two individual input voltages.
- The important applications----multiplication, division, squaring and square – rooting of signals, modulation and demodulation.
- These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. $V0 = VxVy/10$





Multiplier quadrants:

- The transfer characteristics of a typical four-quadrant multiplier is shown in figure. Both the inputs
  can be positive or negative to obtain the corresponding output as shown in the transfer
  characteristics.



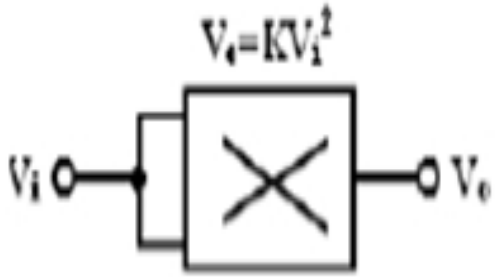
Applications of Multiplier ICs:

The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequency doubler
3. Voltage divider
4. Square rooter
5. Phase angle detector
6. Rectifier

Voltage Squarer:

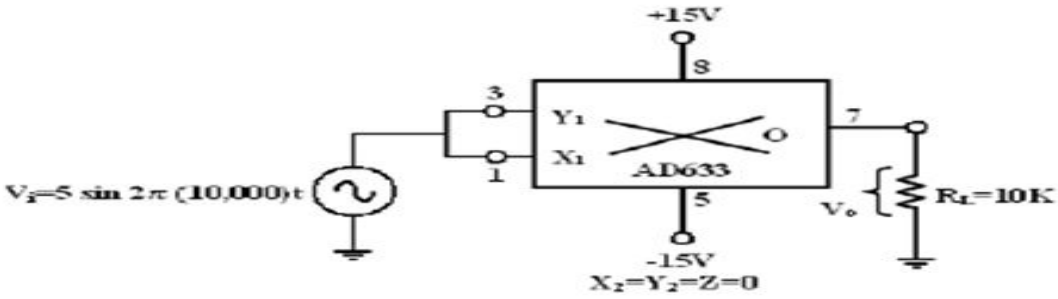
- Figure shows the multiplier IC connected as a squaring circuit. The inputs can be positive or
  negative, represented by any corresponding voltage level between 0 and 10V.
- The input voltage Vi to be squared is simply connected to both the input terminals, and hence we have, Vx = Vy = Vi and the output is V0 = K Vi^2 .
- The circuit thus performs the squaring operation. This application can be extended for frequency doubling applications.

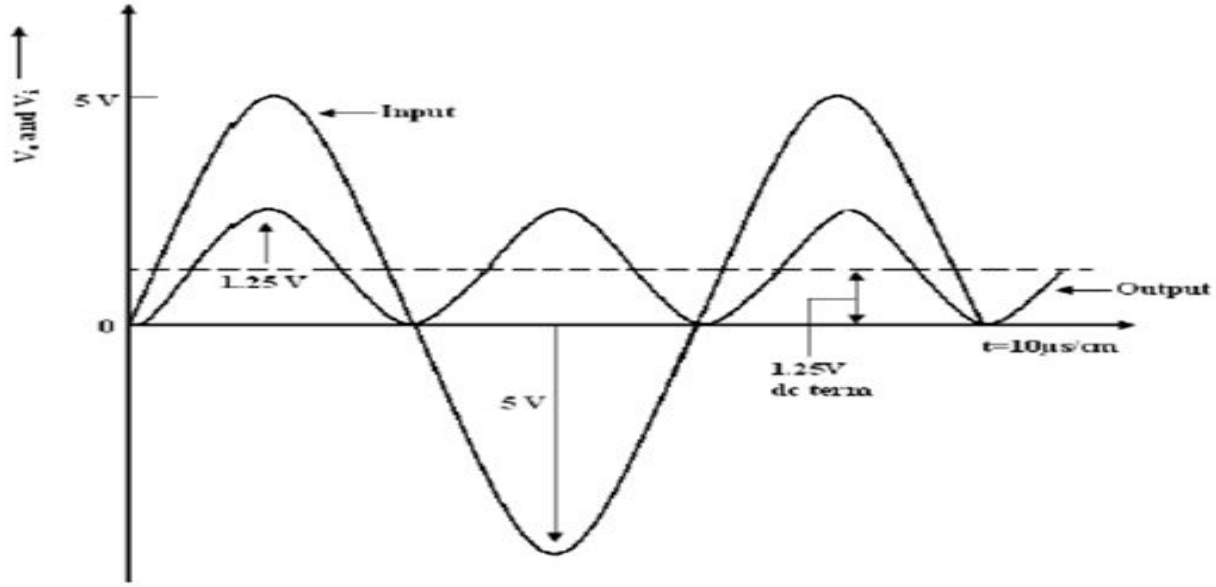


Frequency doubler

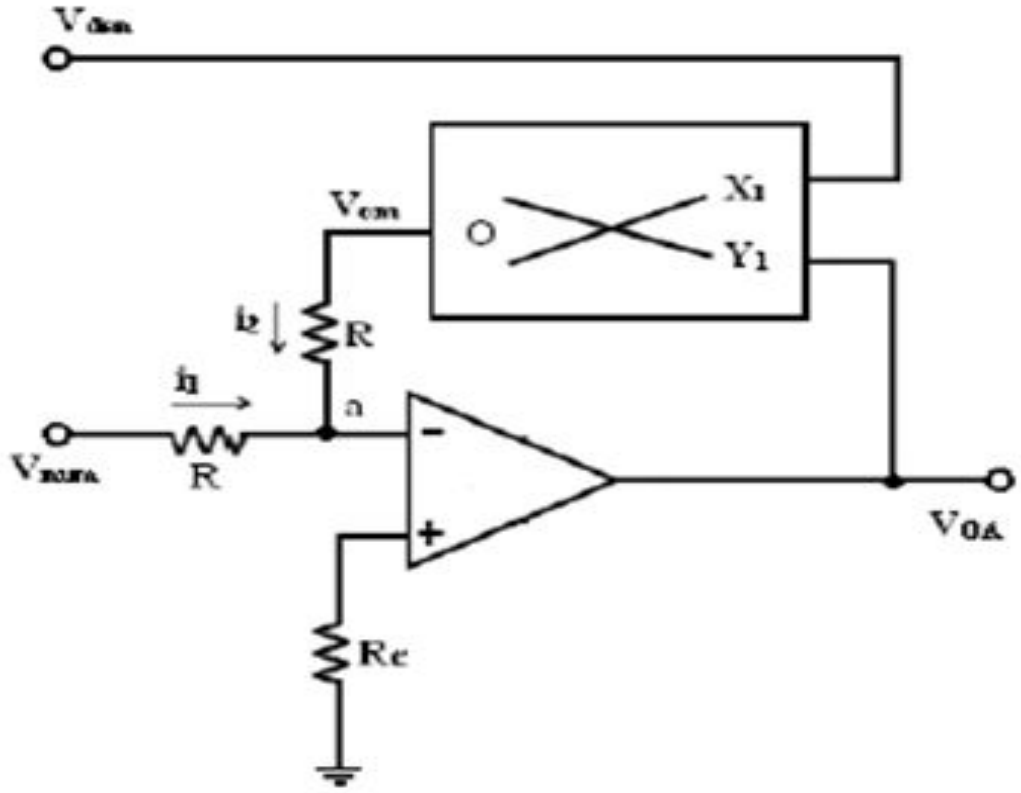
- A sine-wave signal Vi has a peak amplitude of Av and frequency of fHz.
- Assuming a peak amplitude Av of 5V and frequency f of 10KHz, V0 $=1.25 - 1.25 \cos 2\Pi(20000)t$.
  The first term represents the dc term of 1.25V peak amplitude .
- The output waveforms ripples with twice the input frequency in the rectified output of the input signal. This forms the principle of application of analog multiplier as rectifier of ac signals. The dc component of output V0 can be removed by connecting a 1μF coupling capacitor between the output terminal and a load resistor, across which the output can be observed.

Frequency doubler

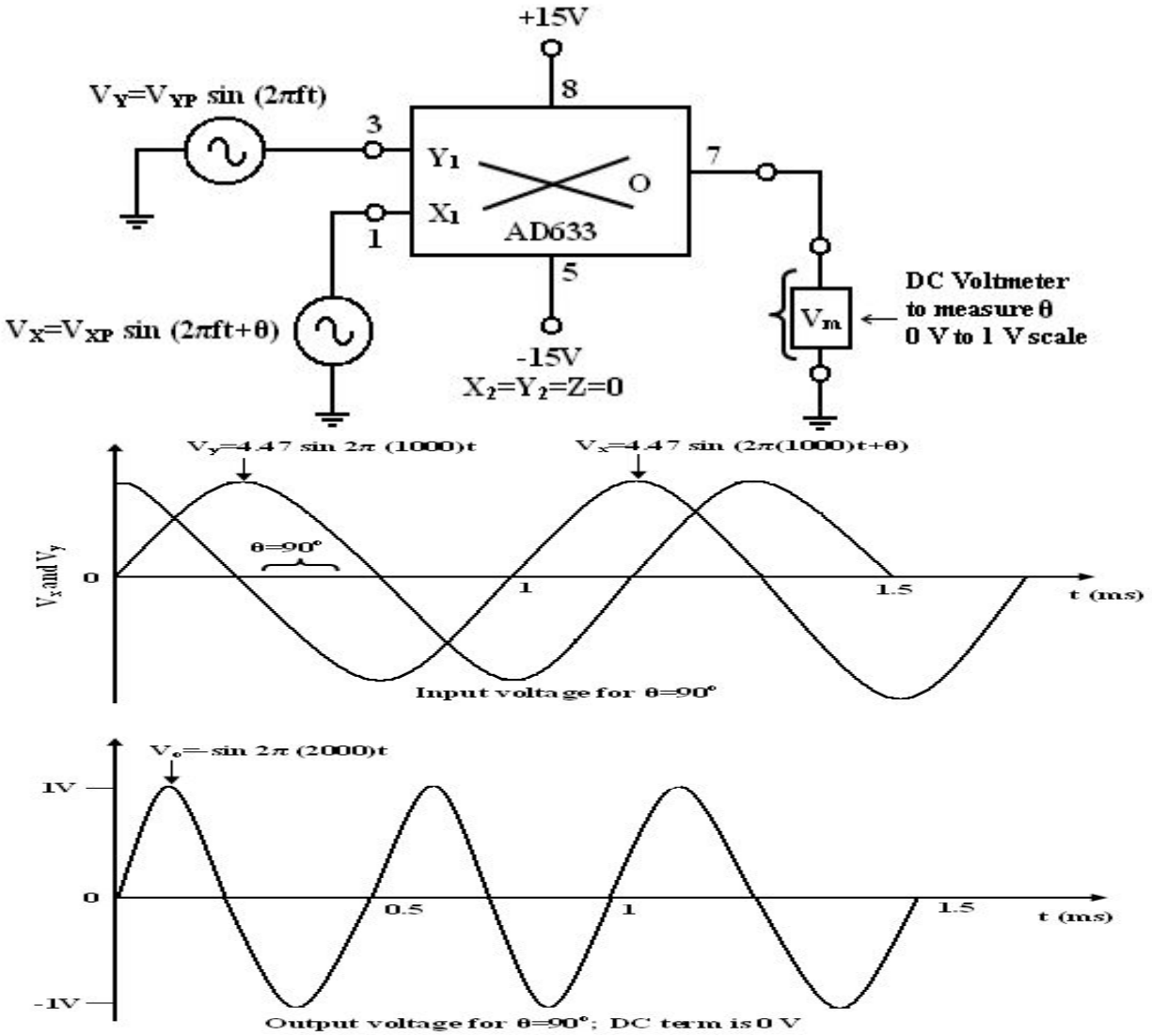




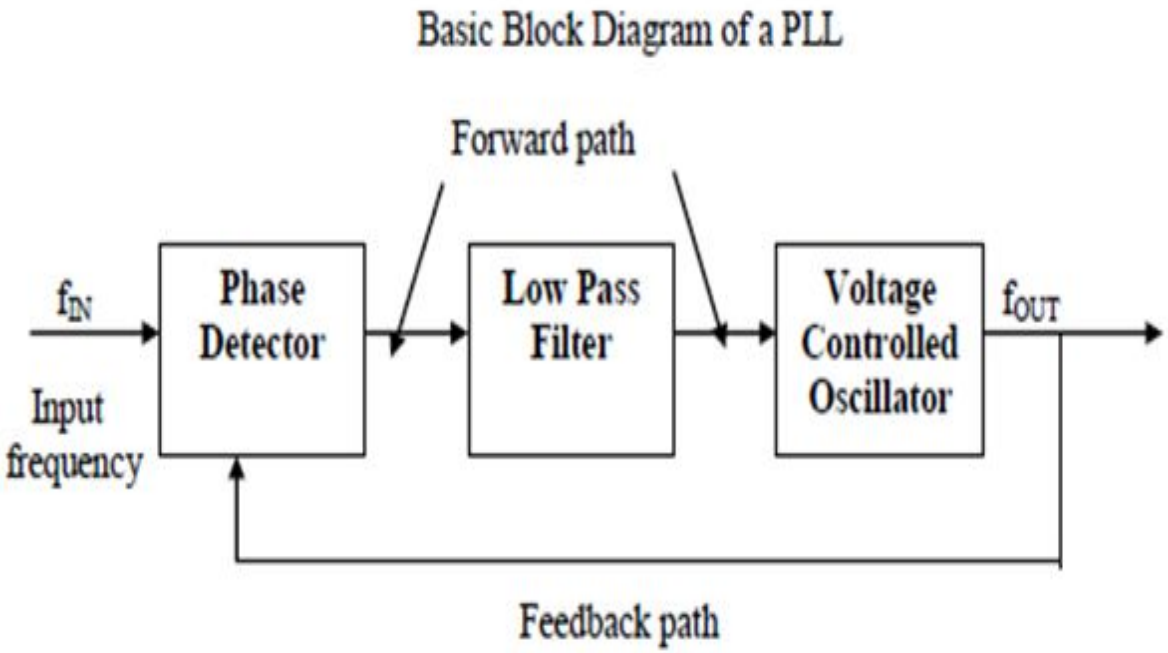
Voltage Divider



Phase angle Detector



PHASE LOCKED LOOP



PLL

Phase detector (PD):

- Analog multiplier
- PD produces an error signal that is proportional to the *phase error*, i.e., to the difference between the phases of input and output signals of the phase-locked loop

Loop filter:

- Low-pass filter
- It is characterized by its transfer function $F(s)$
- Low-pass filter suppresses the noise and unwanted PD outputs. It determines the *dynamics* of phase-locked loop

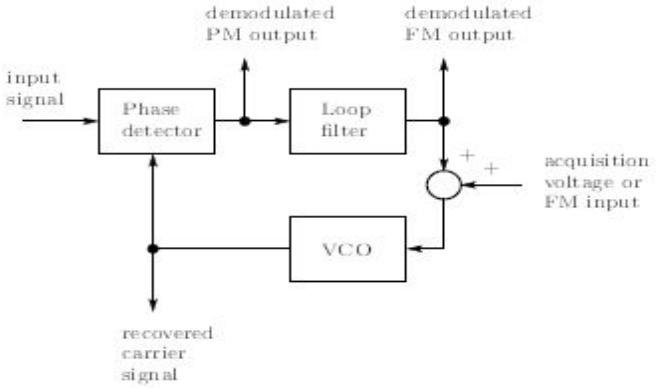
Voltage-controlled oscillator (VCO):

- VCO generates a sinusoidal signal
- The instantaneous VCO frequency is controlled by its input voltage

PLL

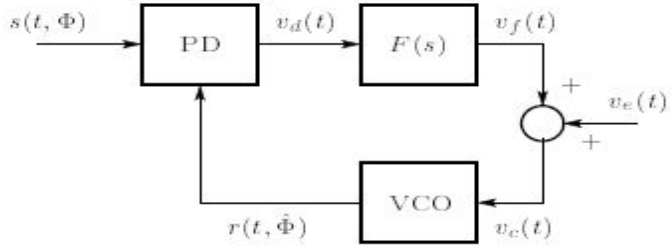
OPERATION PRINCIPLE OF PHASE-LOCKED LOOP – Part I

Basic loop configuration



PLL block diagram

Voltages appearing in the loop are also shown



Phase detector (PD) compares the phase of the input signal $s(t, \Phi)$ against the phase of the VCO output $r(t, \hat{\Phi})$ and produces an error signal $v_d(t)$

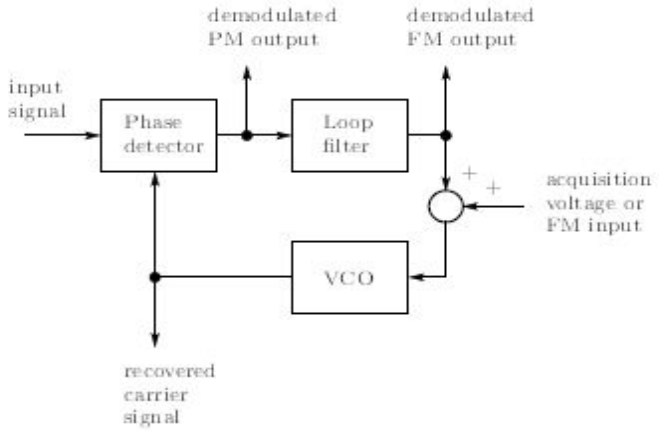
This error signal is then filtered, in order to remove noise and other unwanted components of the input spectrum

The sum of filter output $v_f(t)$ and an additive external control voltage $v_e(t)$ controls the instantaneous VCO frequency

PLL

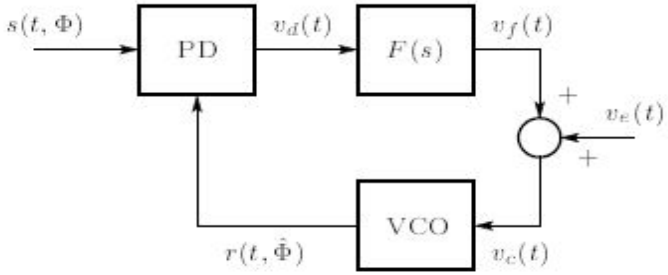
OPERATION PRINCIPLE OF PHASE-LOCKED LOOP – Part II

Basic loop configuration



PLL block diagram

Voltages appearing in the loop are also shown



A nonzero output voltage must be provided by the PD, in order to tune the VCO frequency to the input one if the input frequency differs from the VCO center frequency

Consequently, the PLL tracks the phase of input signal with some phase error. However, this phase error can be kept very small in a well-designed PLL

PLL- construction and operation

- The phase detector or comparator compares the input frequency fs with feedback frequency fo. The output of the phase detector is proportional to the phase difference between fs & fo. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.

- LPF removes the high frequency noise and produces a dc level. The high frequency component (fs + fo) is removed by the low pass filter

- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.

- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

- Before the input is applied, the PLL is in free running state.

- Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode.

- When Phase locked, the loop tracks any change in the input frequency through its repetitive

PLL

- The phase detector is basically a multiplier and produces the sum (fs + fo) and difference (fs – fo) components at its output. The high frequency component (fs + fo) is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage vc to VCO.

- The signal vc shifts the VCO frequency in a direction to reduce the frequency difference between fs and fo. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked.

- Once locked, the output frequency fo of VCO is identical to fs except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage vc to shift the VCO frequency from f0 to fs and thereby maintain the lock. Once locked,PLL tracks the frequency changes of the input signal.

- Thus, a PLL goes through three stages (i)free running, (ii) capture and (iii) locked or tracking.

- Capture range: the range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of fo.

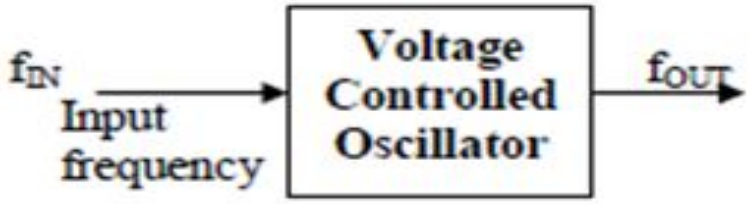
Low – Pass filter

- The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise.
- LPF controls the characteristics of the phase locked loop. i.e, capture range, lock ranges, bandwidth

  Lock range(Tracking range):The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fIN.
- Capture range:Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.
- Filter Bandwidth:Filter Bandwidth is reduced, its response time increases. However reduced Bandwidth reduces the capture range of the PLL. Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

Voltage Controlled Oscillator (VCO)

- The third section of PLL is the VCO; it generates an output frequency that is directly proportional to its input voltage.
- **Voltage controlled oscillator**
- A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage
- The maximum output frequency of NE/SE 566 is 500 Khz.



Equations

$x_m(t)$ is given by

$$x_m(t) = x_c(t) \cdot x_r(t)$$

the VCO frequency may be written as a function of the VCO input $y(t)$ as

$$\omega_r(t) = \omega_f + g_v y(t)$$

where g_v is the *sensitivity* of the VCO and is expressed in Hz / V.

Hence the VCO output takes the form

$$x_r(t) = A_r \cos\left(\int_0^t \omega_r(\tau)\, d\tau\right) = A_r \cos(\omega_f t + \varphi(t))$$

where

$$\varphi(t) = \int_0^t g_v y(\tau)\, d\tau$$

The loop filter receives this signal as input and produces an output

$$x_f(t) = F_{\text{filter}}(x_m(t))$$

where F_{Filter} is the operator representing the loop filter transformation.

When the loop is closed, the output from the loop filter becomes the input to the VCO thus

$$y(t) = x_f(t) = F_{\text{filter}}(x_m(t))$$

We can deduce how the PLL reacts to a sinusoidal input signal:

$$x_c(t) = A_c \sin(\omega_c t).$$

The output of the phase detector then is:

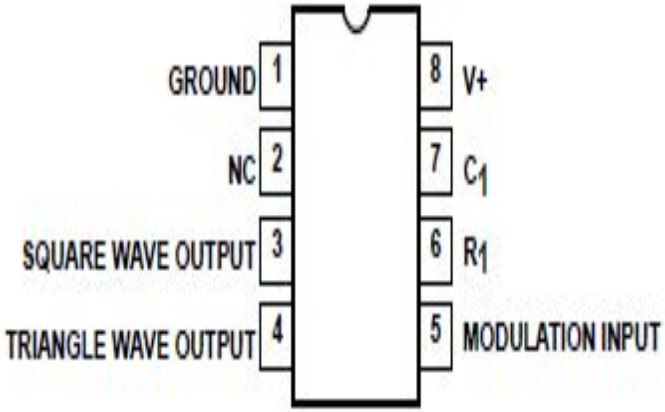
$$x_m(t) = A_c \sin(\omega_c t) A_r \cos(\omega_f t + \varphi(t)).$$

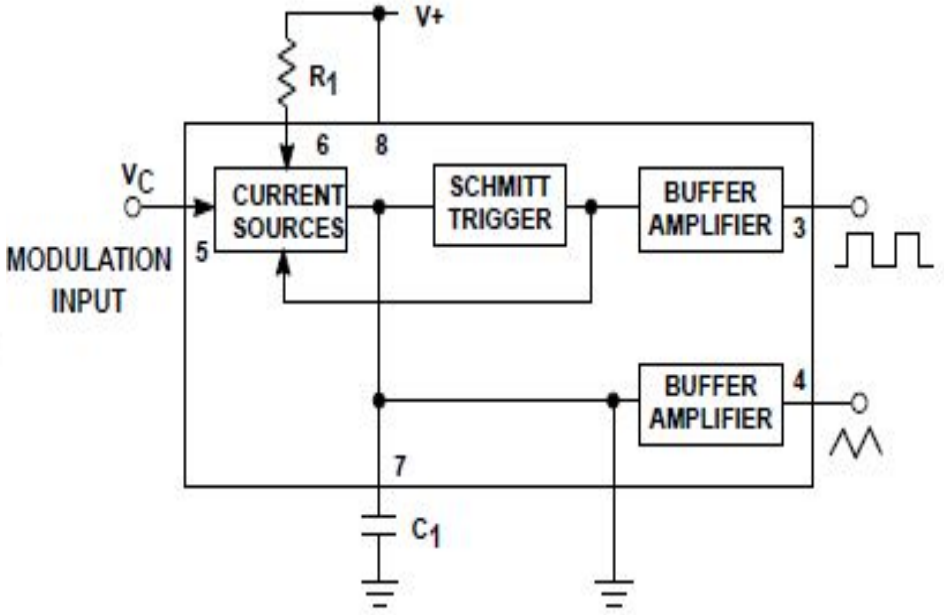
This can be rewritten into sum and difference components using trigonometric identities:

$$x_m(t) = \frac{A_c A_f}{2} \sin(\omega_c t - \omega_f t - \varphi(t)) + \frac{A_c A_f}{2} \sin(\omega_c t + \omega_f t + \varphi(t))$$

If we can make $\omega_f \approx \omega_c$, then the $\sin(\cdot)$ can be approximated by its argument resulting in: $y(t) = x_f(t) \simeq -A_c A_f \varphi(t)/2$. The phase-locked loop is said to be *locked* if this is the case.

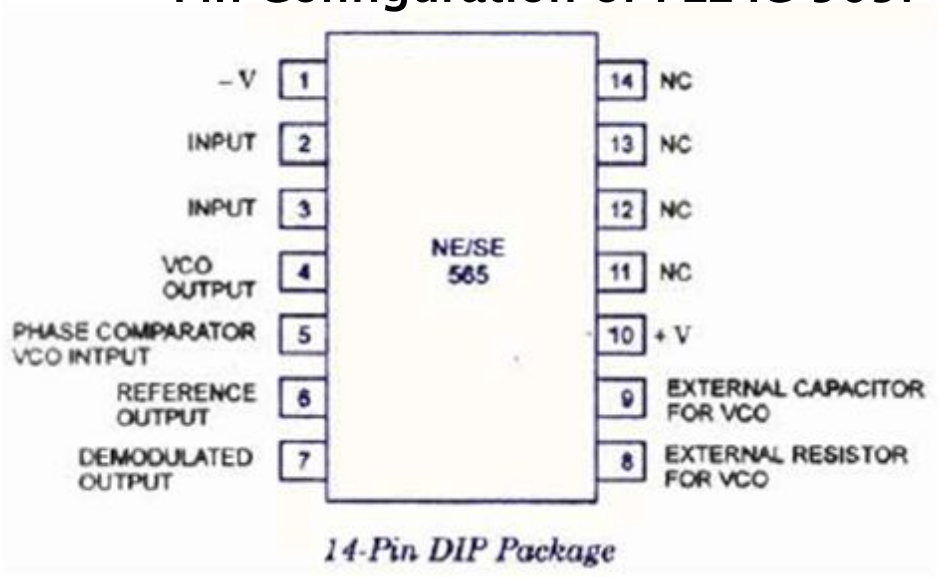
Monilithic VCO-IC 566





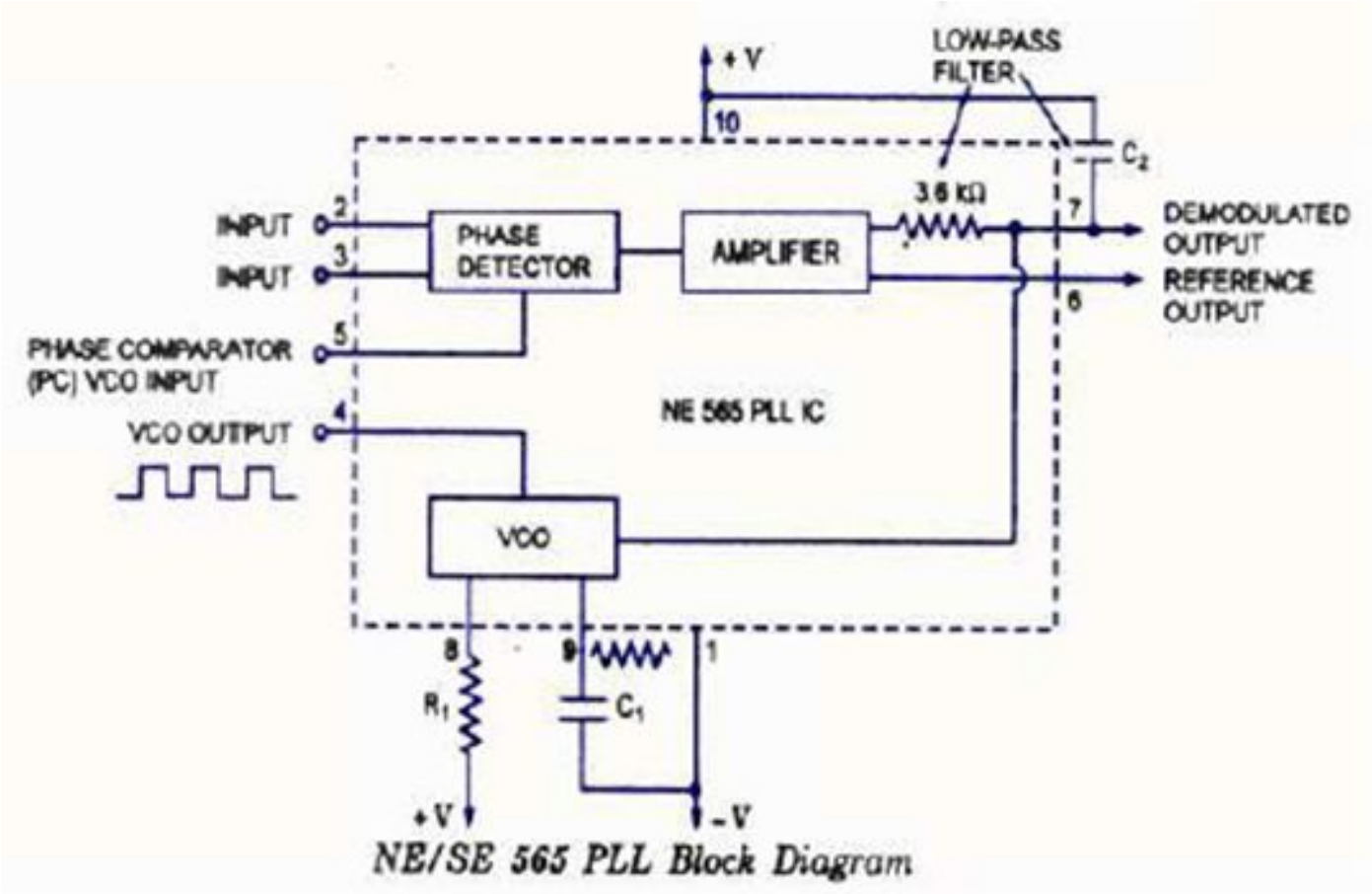
MONOLITHIC PHASE LOCKED LOOPS (PLL IC 565)

Pin Configuration of PLL IC 565:



14-Pin DIP Package

Block Diagram



NE/SE 565 PLL Block Diagram

IC565

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561,
562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency & bandwidth adjustment ranges.
The important electrical characteristics of the 565 PLL are,

- Operating frequency range: 0.001Hz to 500 Khz.
- Operating voltage range: ±6 to ±12v
- Input level required for tracking: 10mv rms min to 3 Vpp max
- Input impedance: 10 K ohms typically.
- Output sink current: 1mA
- Output source current: 10 mA

The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by

$$f_{OUT} = \frac{1.2}{4R1C1} \text{ Hz} \text{----------(1)}$$

where R1&C1 are an external resistor & a capacitor connected to pins 8 & 9.

IC565

- The lock range fL & capture range fc of PLL is given by,

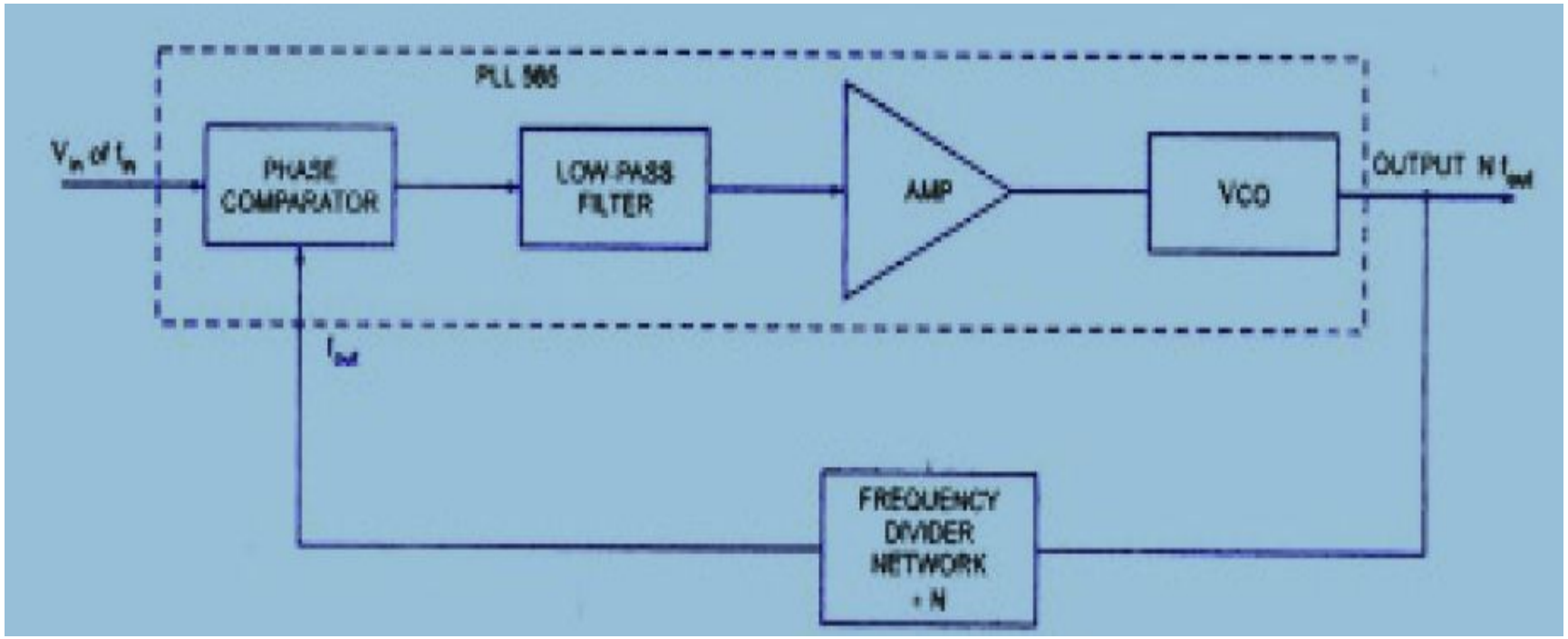
$$f_L = \pm \frac{8\ f_{out}}{V}\ Hz \quad \text{----------(2)}$$

Where f_{OUT} = free running frequency of VCO (Hz)

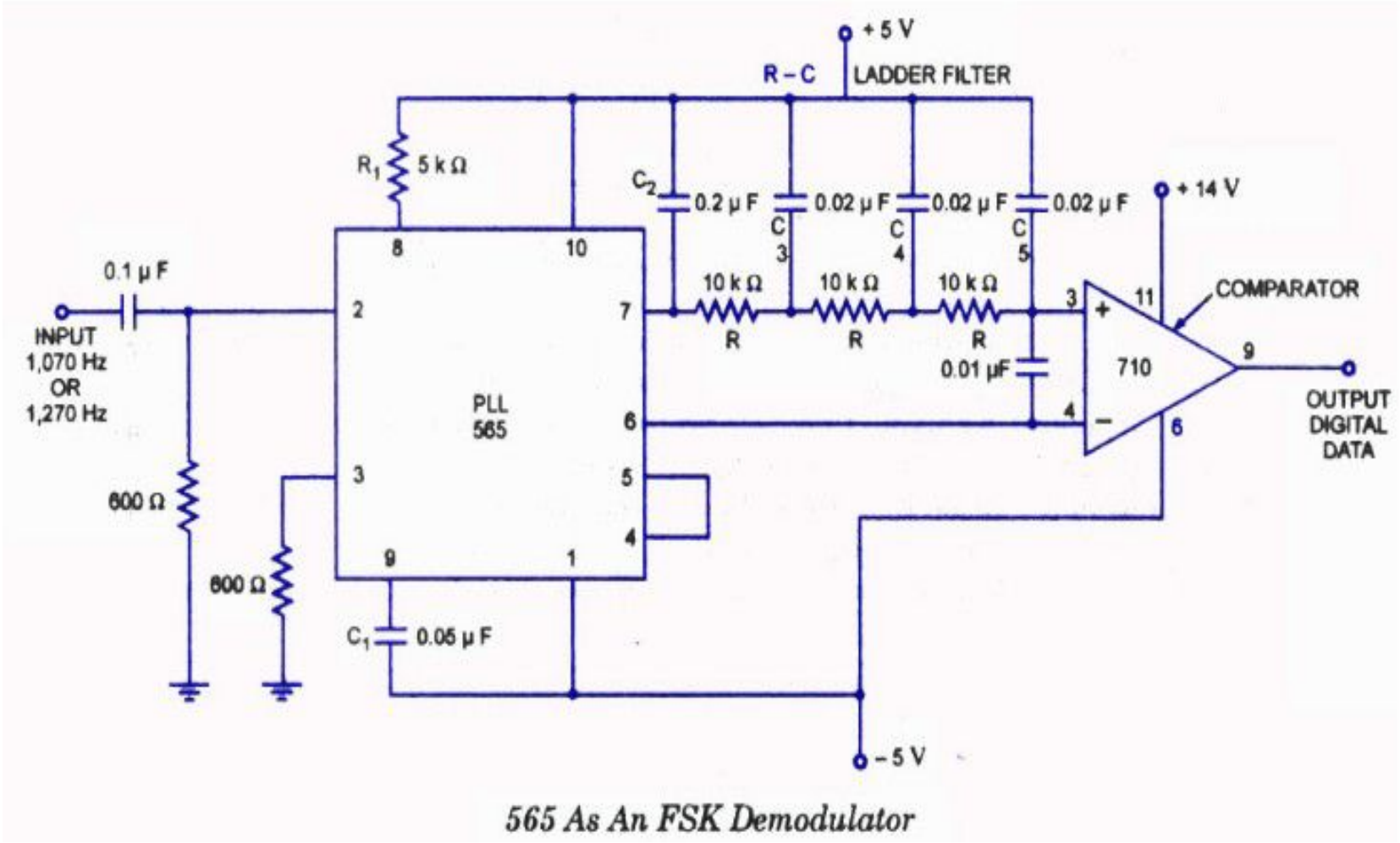
V = (+V)-(-V) volts

$$f_C = \pm \left[\frac{f_L}{(2\Pi)(3.6)(10^3)C_2} \right]^{1/2} \quad \text{----------(3)}$$

Applications of PLL-IC
1.Frequency Multiplier



2.FSK Demodulator



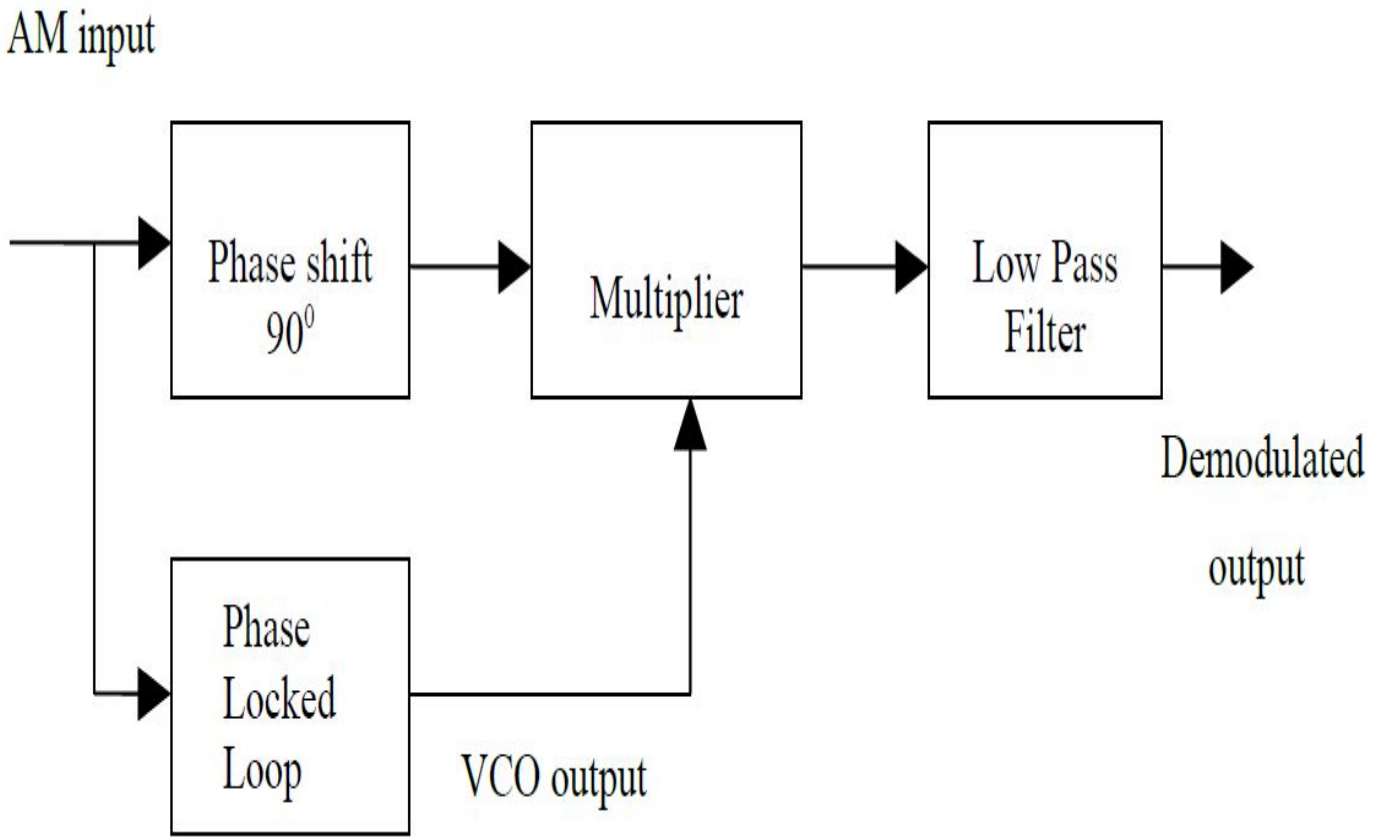
565 As An FSK Demodulator

FSK Demodulator

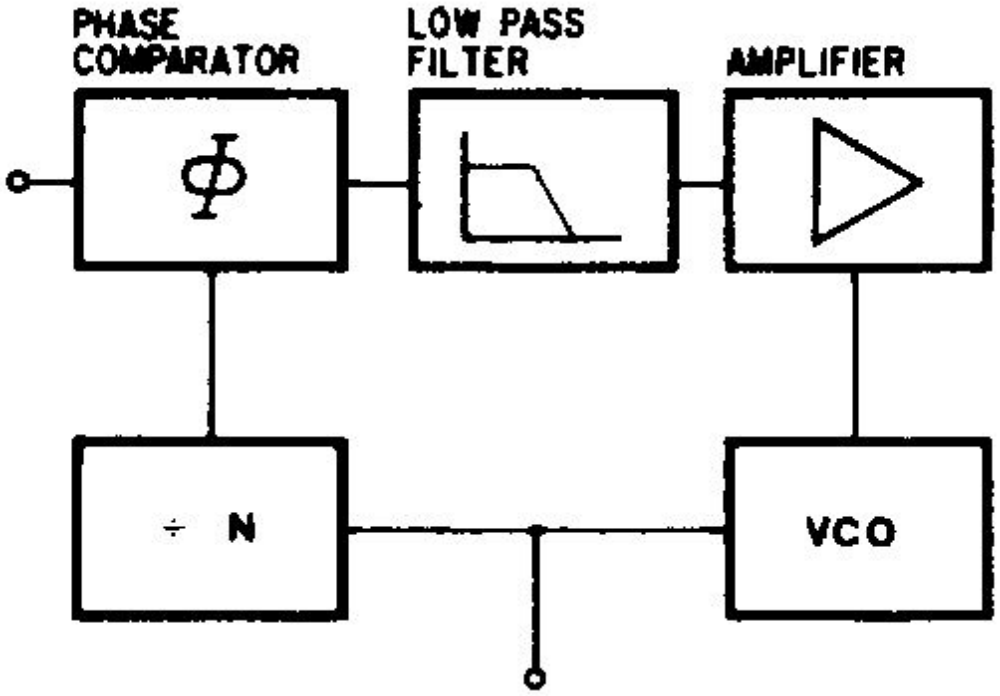
- · The output of 555 FSK generator is applied to the 565 FSK demodulator.
- · Capacitive coupling is used at the input to remove dc line.
- · At the input of 565, the loop locks to the input frequency & tracks it between the 2 frequencies.
- · R1 & C1 determine the free running frequency of the VCO, 3 stage RC ladder filter is used to

  remove the carrier component from the output.

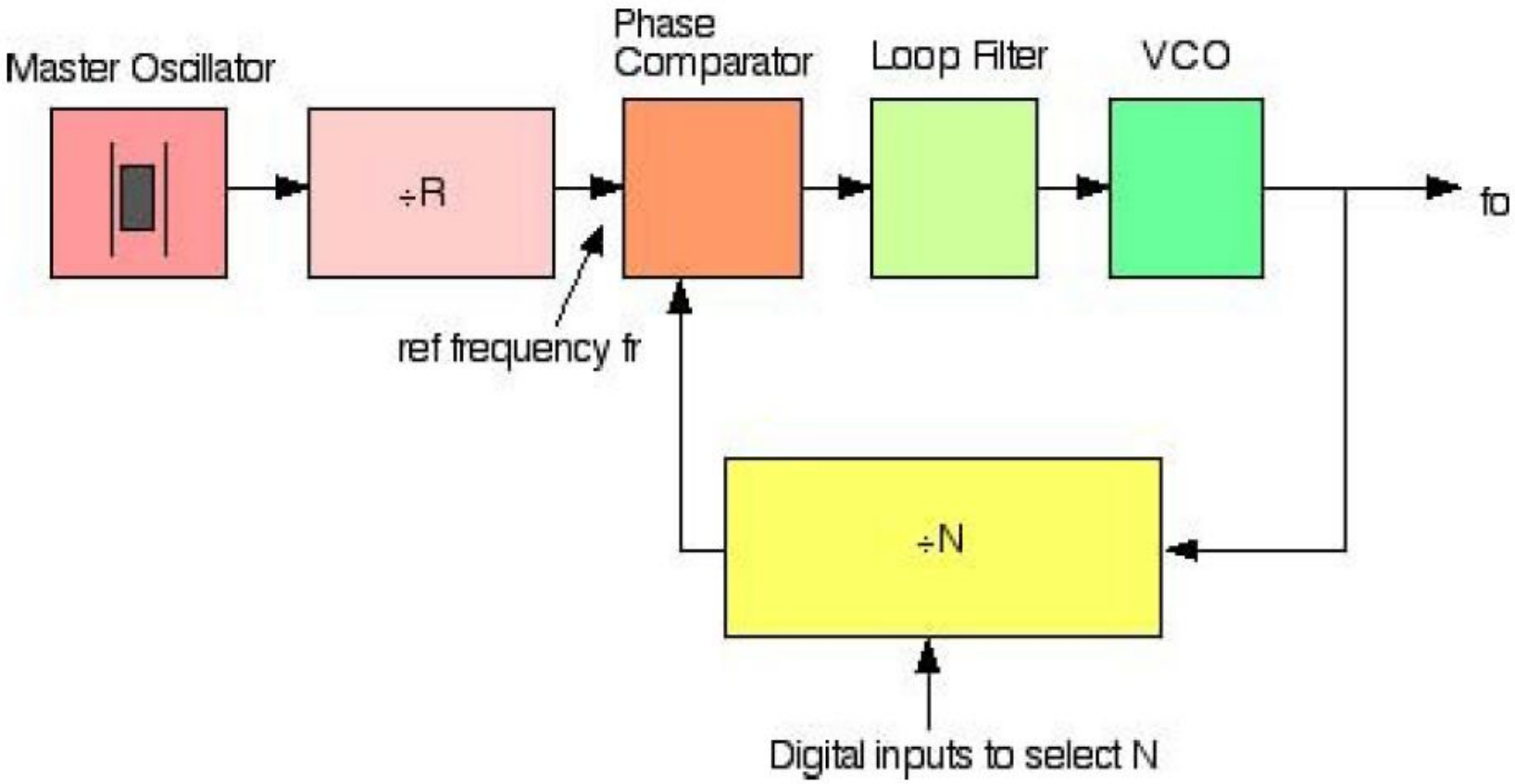
3.AM Demodulation



4.Frequency multiplication/division:



5.Frequency Synthesizer



Analog to Digital
&
Digital to Analog converters

UNIT–IV

Analog Signals

Analog signals – directly measurable quantities in terms of some other quantity

Examples:

- Thermometer – mercury height rises as temperature rises
- Car Speedometer – Needle moves farther right as you accelerate
- Stereo – Volume increases as you turn the knob.

Digital Signals

Digital Signals – have only two states. For digital computers, we refer to binary states, 0 and 1. “1” can be on, “0” can be off.

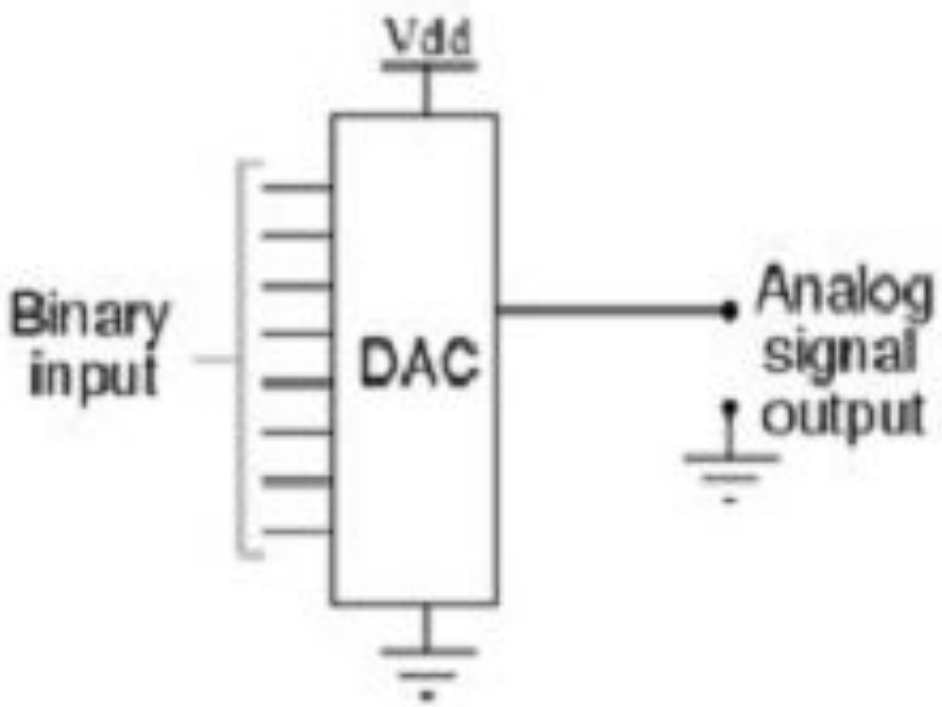
Examples:

- Light switch can be either on or off
- Door to a room is either open or closed

Examples of A/D Applications

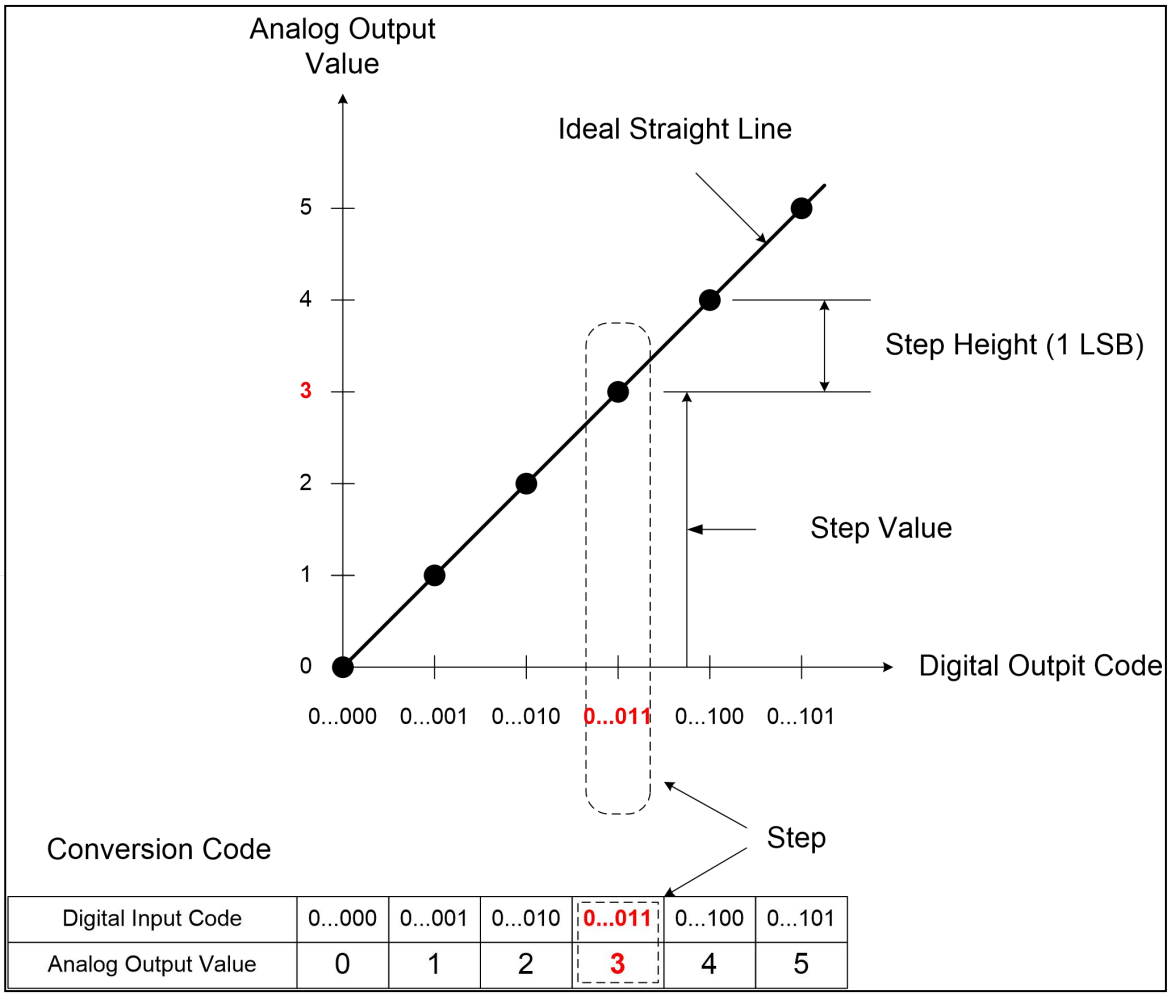
- Microphones – take your voice varying pressure waves in the air and convert them into varying electrical signals
- Strain Gages – determines the amount of strain (change in dimensions) when a stress is applied
- Thermocouple – temperature measuring device converts thermal energy to electric energy
- Voltmeters
- Digital Multimeters

D/A converter (DAC)



The Ideal Transfer Function (DAC)

The DAC theoretical ideal transfer function would also be a straight line with an infinite number of steps but practically it is a series of points that fall on the ideal straight line as shown in Figure



Conversion Code

Digital Input Code	0...000	0...001	0...010	0...011	0...100	0...101
Analog Output Value	0	1	2	3	4	5

Specifications of DAC

Static errors, that is those errors that affect the accuracy of the converter when it is converting static (dc) signals, can be completely described by just four terms.

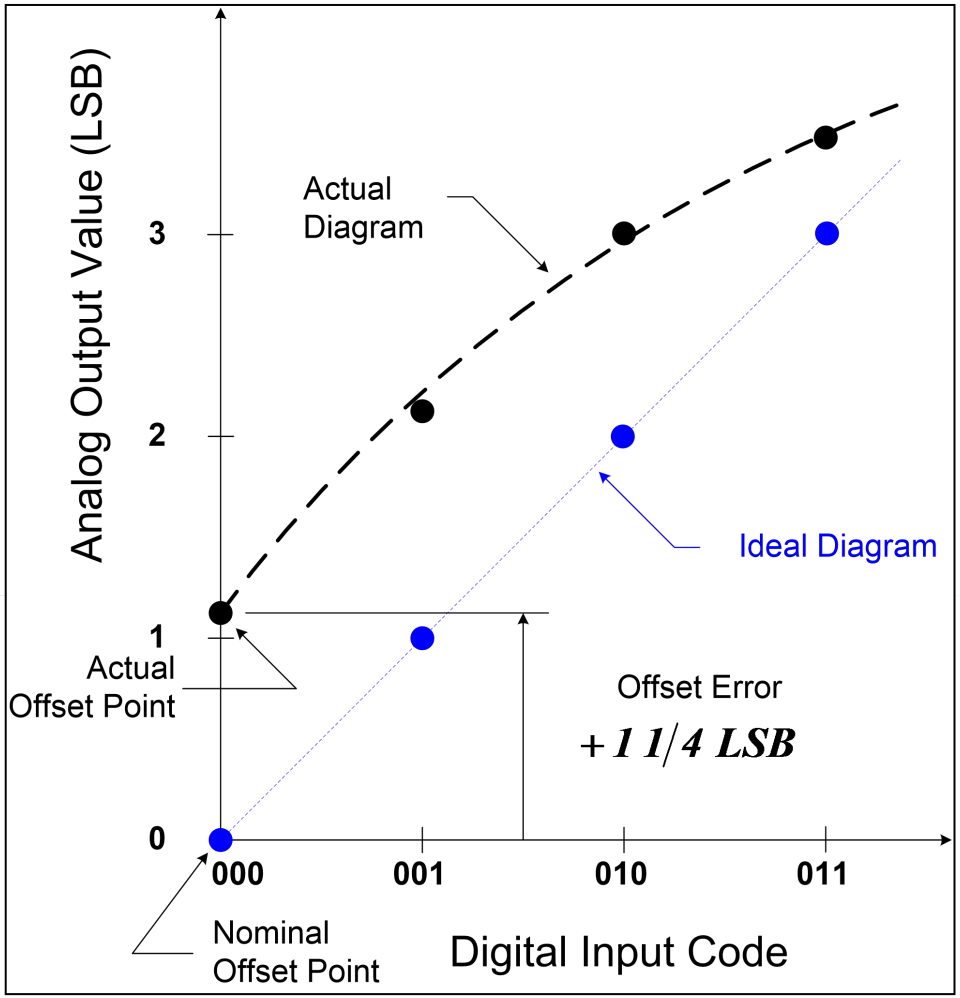
These are :

- **offset error,**
- **gain error,**
- **integral nonlinearity and**
- **differential nonlinearity.**

Each can be expressed in LSB units or sometimes as a percentage of the FSR

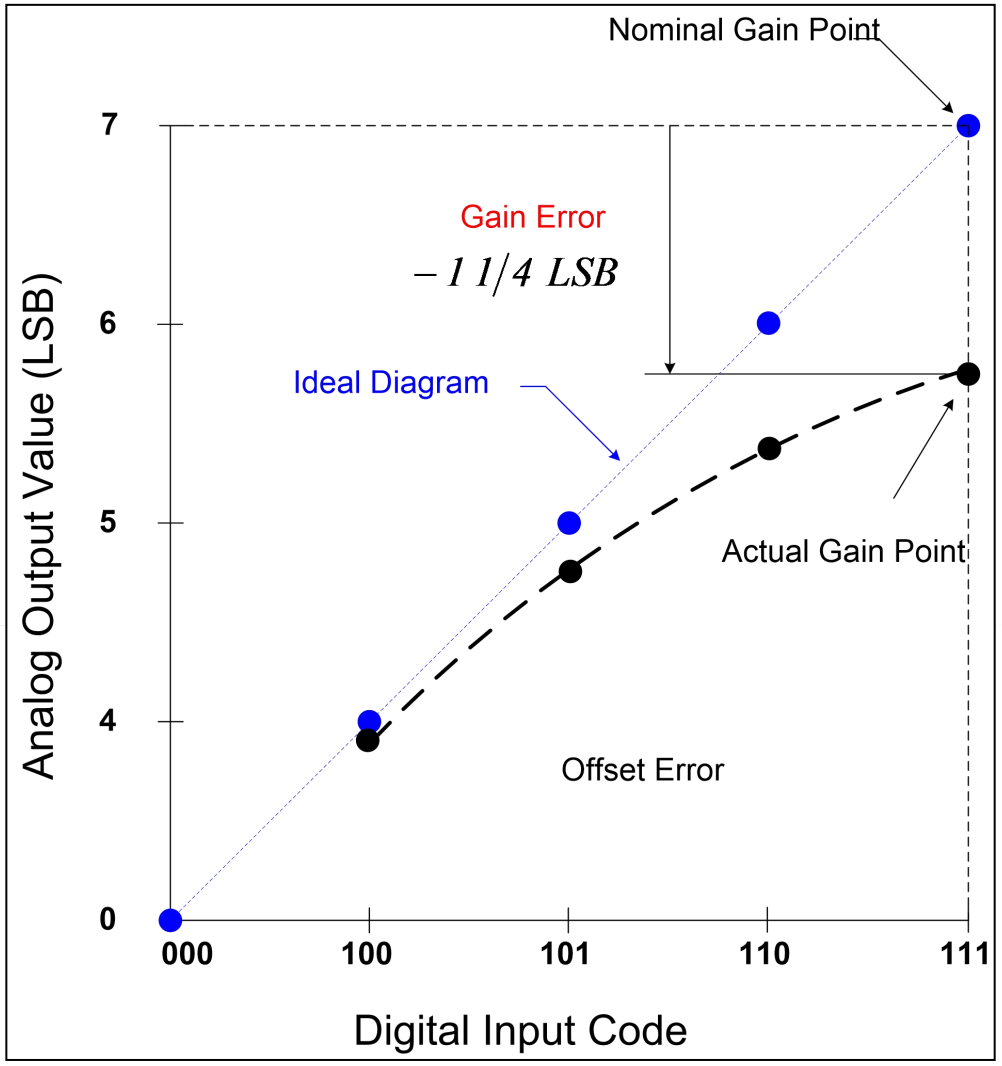
Offset Error – DAC

For a DAC it is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by a **trimming process**. If trimming is not possible, this error is referred to as the **zero-scale error**.



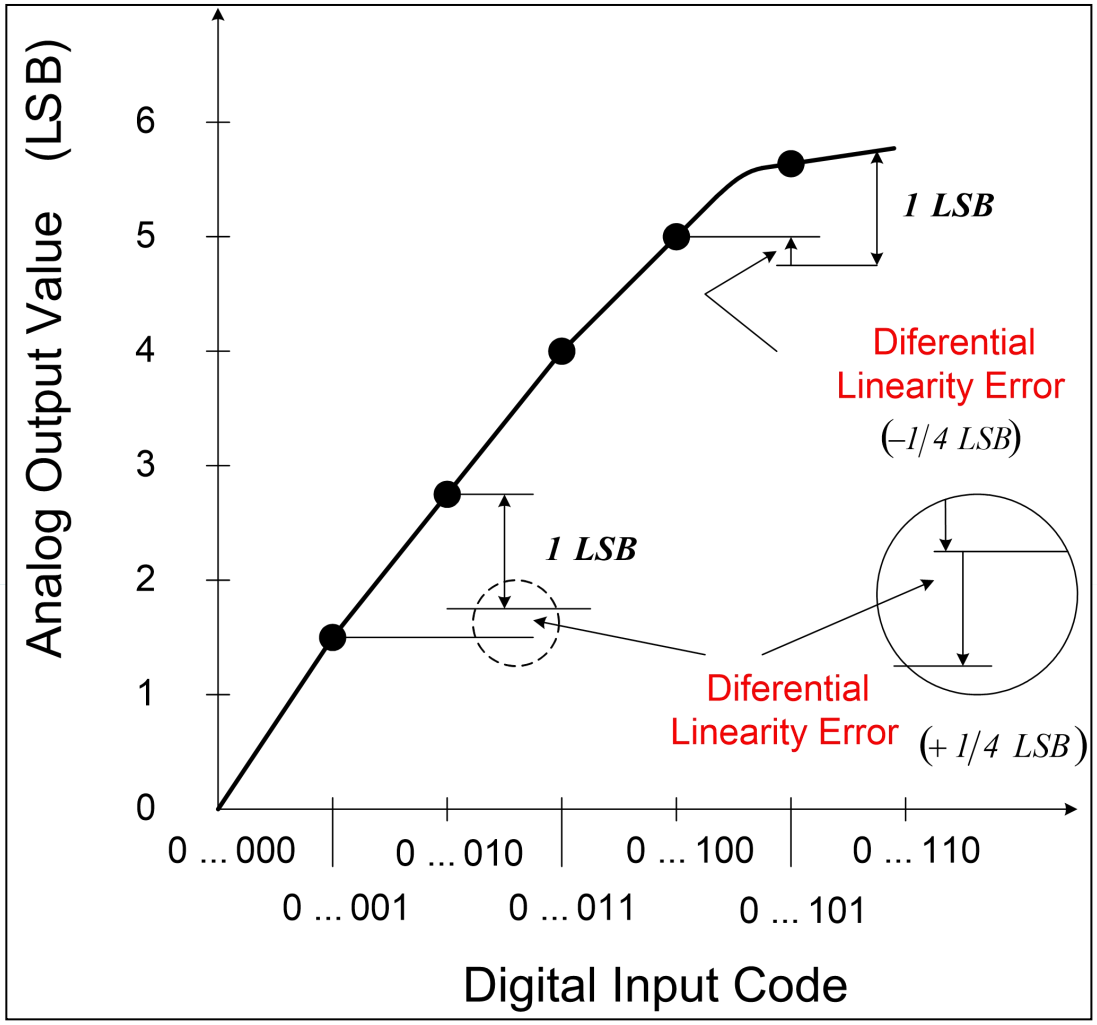
Gain Error – DAC

For a DAC it is the step value when the digital input is full scale. **This error represents a difference in the slope of the actual and ideal transfer functions** This error can also usually be adjusted to zero by trimming.



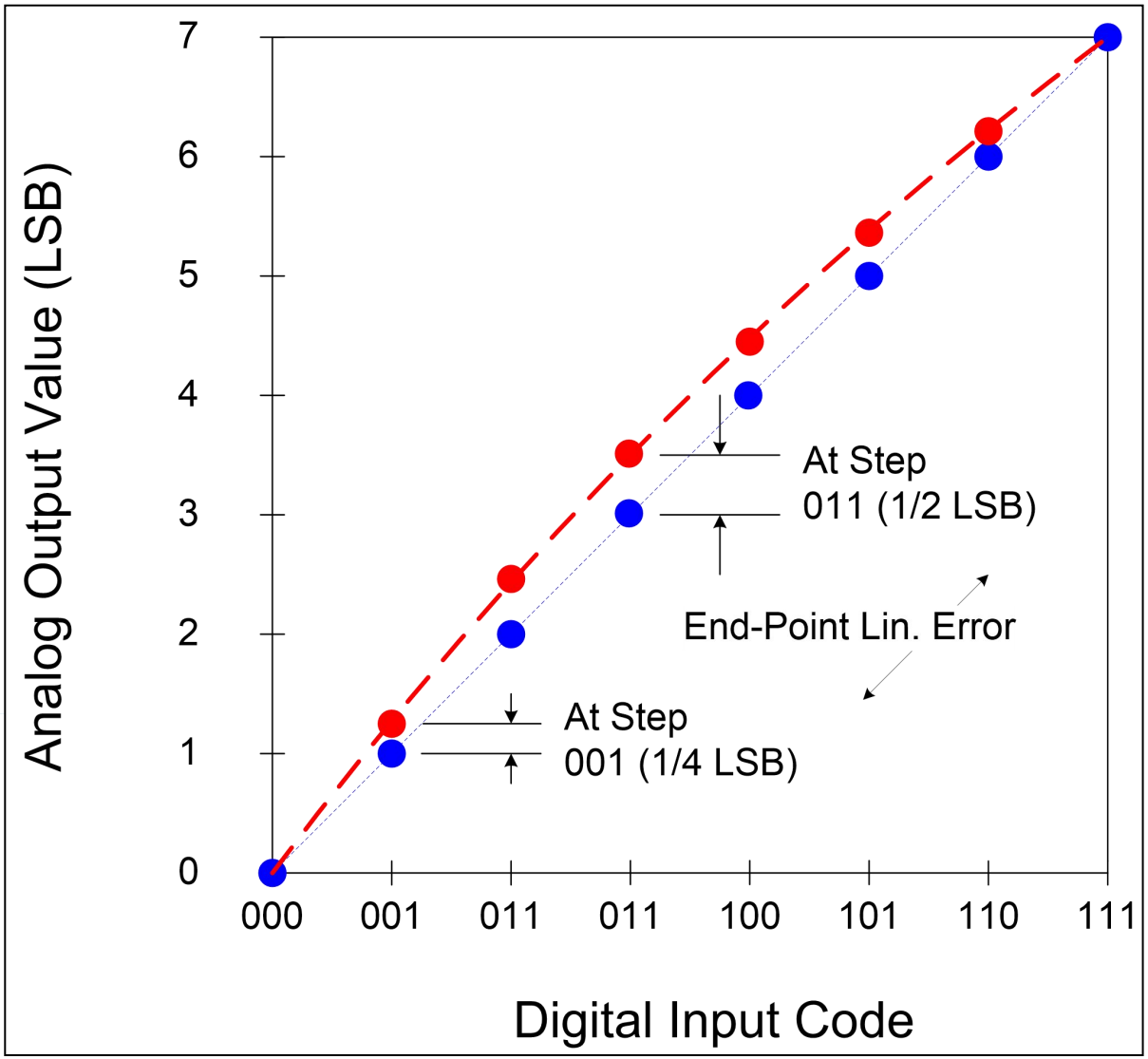
Differential Nonlinearity (DNL) Error – DAC

The differential nonlinearity error shown in Figure is the **difference between an actual step height (for a DAC) and the ideal value of 1 LSB**. Therefore if the step height is exactly 1 LSB, then the differential nonlinearity error is zero

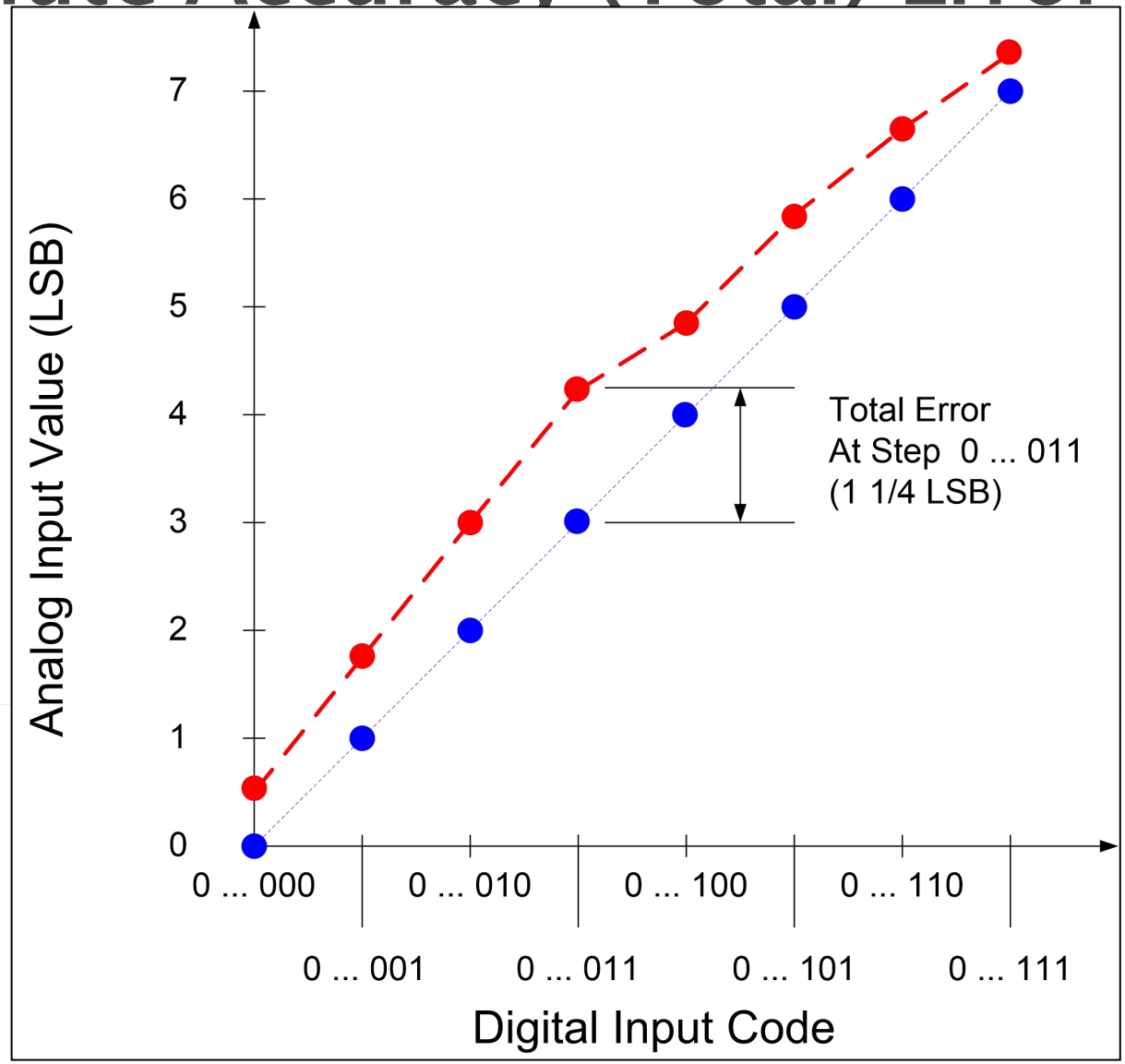


Integral Nonlinerity (INL) Error – DAC

The name integral nonlinearity derives from the fact that the summation of the differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step.



Absolute Accuracy (Total) Error –DAC–



Resolution:

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

$$\text{Resolution (Volts)} = Vo_{FS} / (2^{n} - 1) = 1 \text{ LSB increment}$$

Where 'n' is the number of input bits

'Vo_{FS}' is the full scale output voltage.

Example:

Resolution for an 8 – bit DAC for example is said to have

: 8 – bit resolution

: A resolution of 0.392 of full-Scale (1/255)

: A resolution of 1 part in 255.

Thus resolution can be defined in many different ways.

The following table shows the resolution for 6 to 16 bit DACs

S.No.	Bits	Intervals	LSB size (% of full-scale)	LSB size (For a 10 V full-scale)
1.	6	63	1.588	158.8 mV
2.	8	255	0.392	39.2 mV
3.	10	1023	0.0978	9.78 mV
4.	12	4095	0.0244	2.44 mV
5.	14	16383	0.0061	0.61 mV
6.	16	65535	0.0015	0.15 mV

Accuracy

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The ideal converter is the one which does not suffer from any problem. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

The relative accuracy is the maximum deviation after the gain and offset errors have been removed. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage. Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absolute accuracy.

Linearity

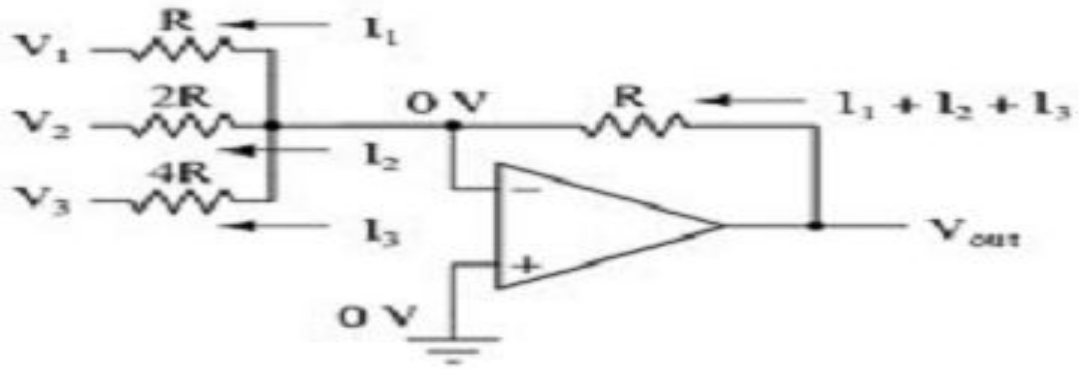
Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale. The linearity of a D/A converter is defined as the precision or exactness with which the digital input is converted into analog output. An ideal D/A converter produces equal increments or step sizes at output for every change in equal increments of binary input.

Monotonicity

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristics is essential in control applications. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition.

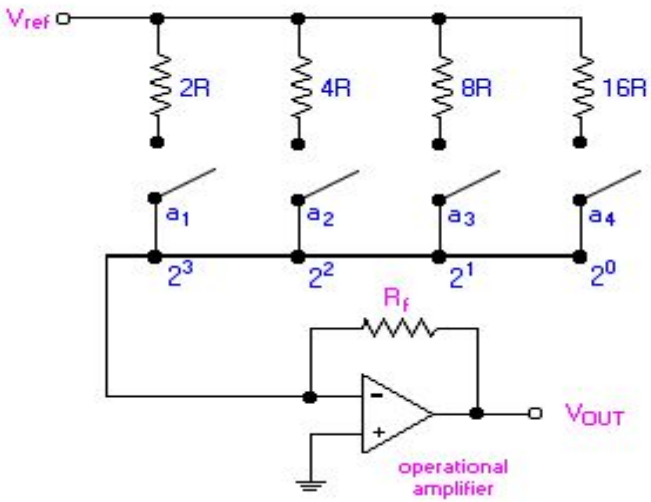
When a D/A Converter doesn't satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

Binary weighted Resistor DAC



$$V_{out} = -\left(V_1 + \frac{V_2}{2} + \frac{V_3}{4}\right)$$

4-bit Binary weighted Resistor DAC



$$
\begin{aligned}
V_{OUT} &= -\, iR_f \\
&= -\left[V_{ref}\left(\frac{a_1}{2R}+\frac{a_2}{4R}+\frac{a_3}{8R}+\frac{a_4}{16R}\right)\right]R_f \\
&= -\,\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2}+\frac{a_2}{4}+\frac{a_3}{8}+\frac{a_4}{16}\right) \\
&= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1}+\frac{a_2}{2^2}+\frac{a_3}{2^3}+\frac{a_4}{2^4}\right)
\end{aligned}
$$

Binary weighted Resistor DAC

For a n-bit DAC, the relationship between V_{out} and the binary input is as follows:

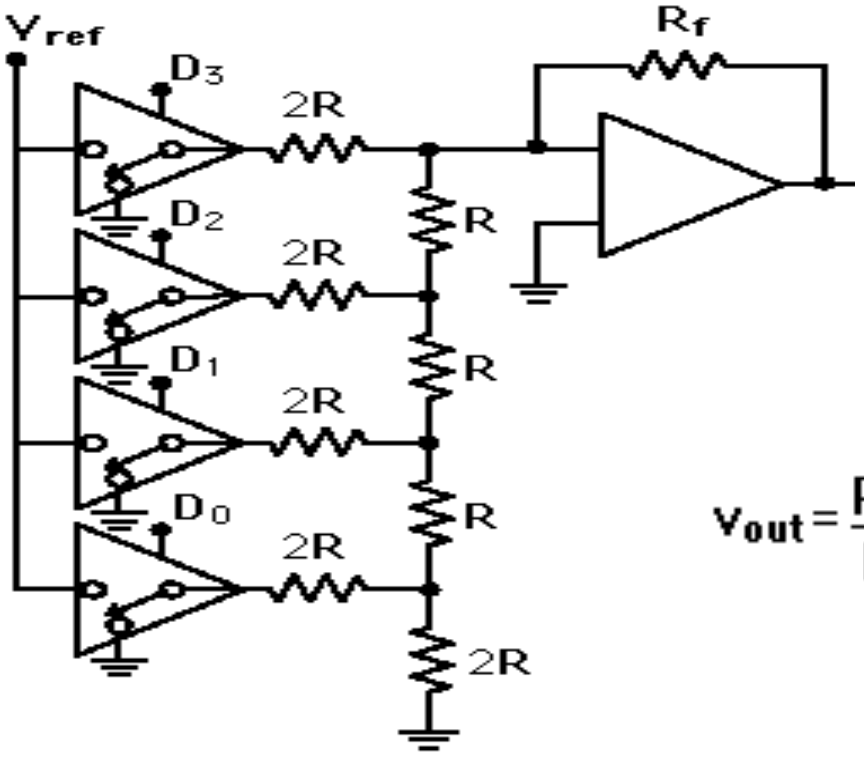
$$V_{OUT} = -\frac{V_{ref} R_f}{R} \sum_{i=1}^{n} \frac{a_i}{2^i}$$

Digital Input				V_{OUT} (Volts)
a_1	a_2	a_3	a_4	
0	0	0	0	0
0	0	0	1	- 0.625
0	0	1	0	- 1.250
0	0	1	1	- 1.875
0	1	0	0	- 2.500
0	1	0	1	- 3.125
0	1	1	0	- 3.750
0	1	1	1	- 4.375
1	0	0	0	- 5.000
1	0	0	1	- 5.625
1	0	1	0	- 6.250
1	0	1	1	- 6.875
1	1	0	0	- 7.500
1	1	0	1	- 8.125
1	1	1	0	- 8.750
1	1	1	1	- 9.375

Weighted Sum DAC

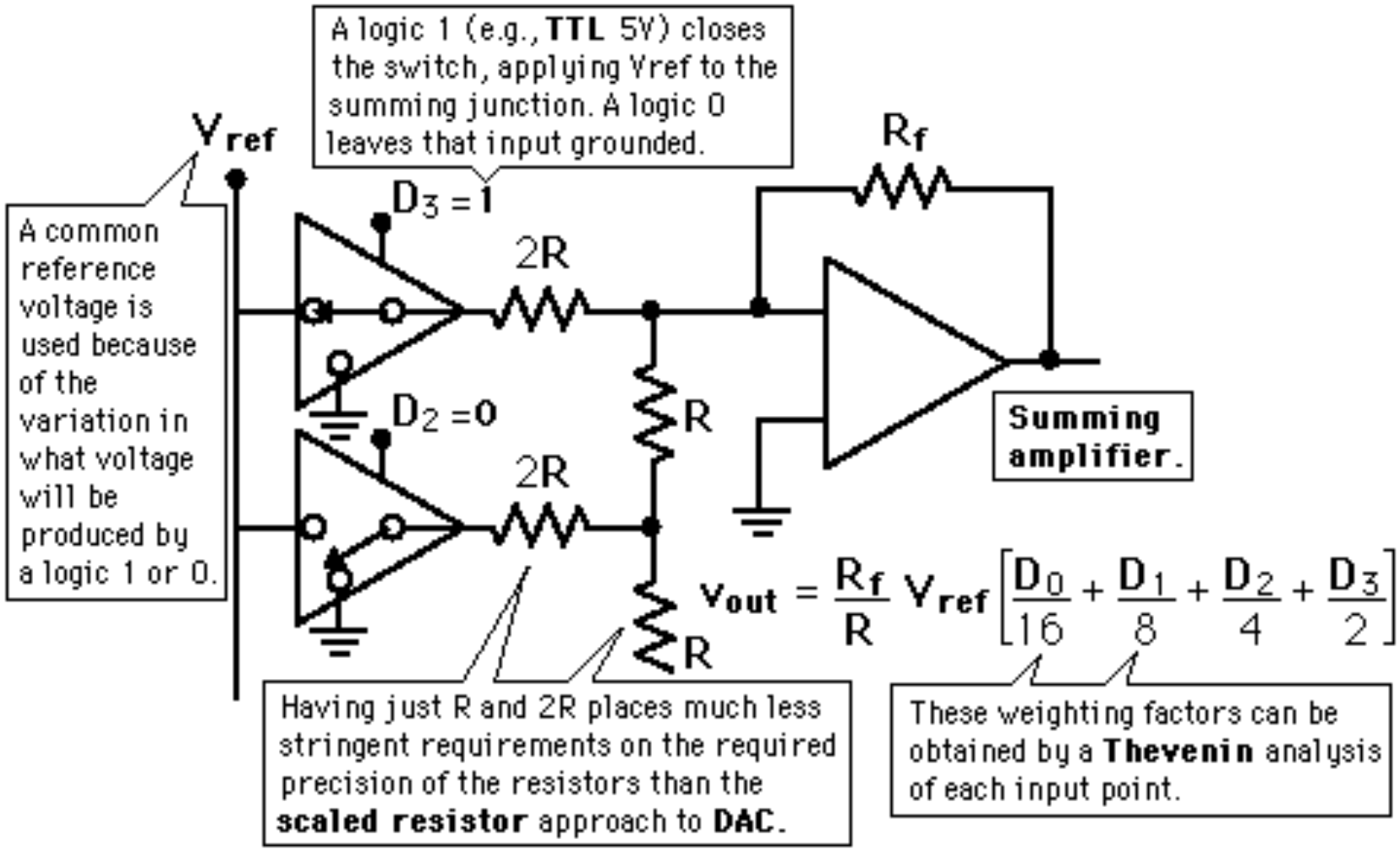
- One way to achieve D/A conversion is to use a summing amplifier.
- This approach is not satisfactory for a large number of bits because it requires too much precision in the summing resistors.
- This problem is overcome in the R-2R network DAC.

R–2R Ladder type DAC



$$V_{out} = \frac{R_f}{R} V_{ref} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right]$$

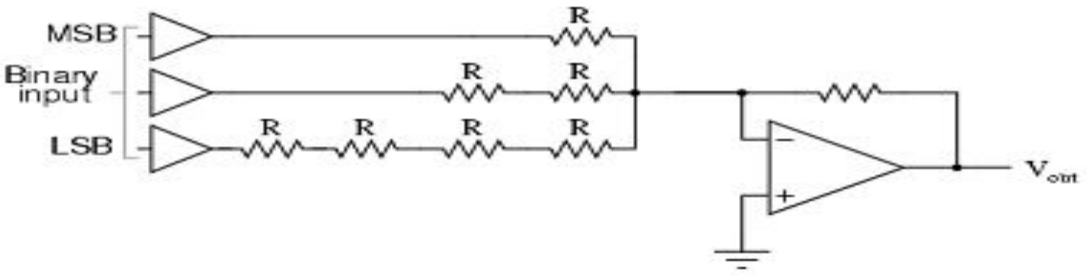
R–2R Ladder DAC

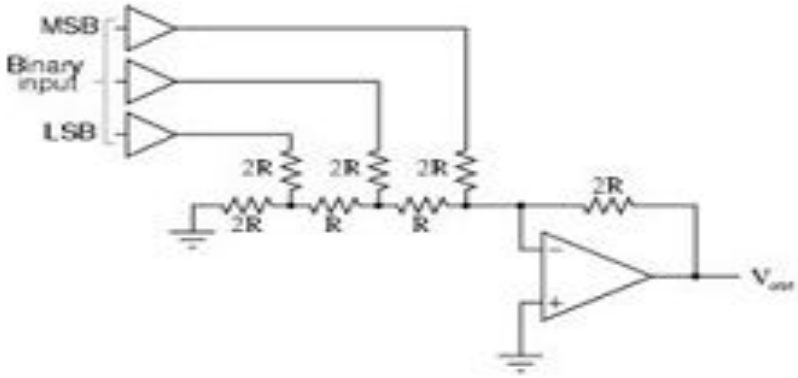


R-2R Ladder DAC

- The summing amplifier with the R-2R ladder of resistances shown produces the output where the D's take the value 0 or 1.
- The digital inputs could be TTL voltages which close the switches on a logical 1 and leave it grounded for a logical 0.
- This is illustrated for 4 bits, but can be extended to any number with just the resistance values R and 2R.

R–2R Ladder DAC



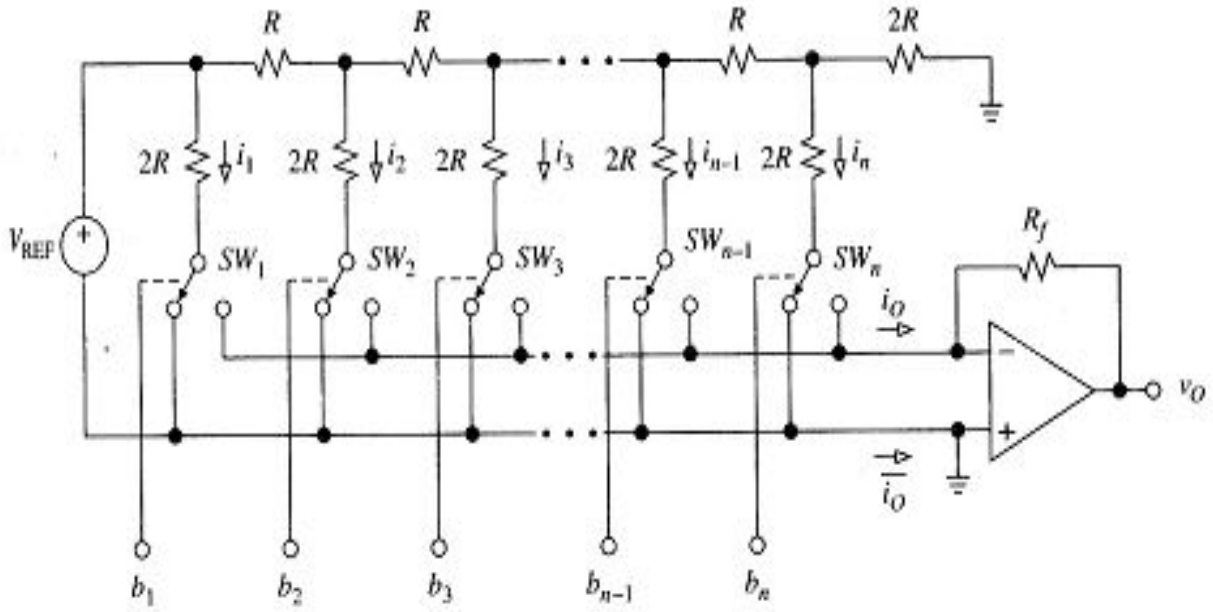


$$Vout = -(VMSB + Vn + VLSB) = -(VRef + VRef/2 + VRef/4)$$

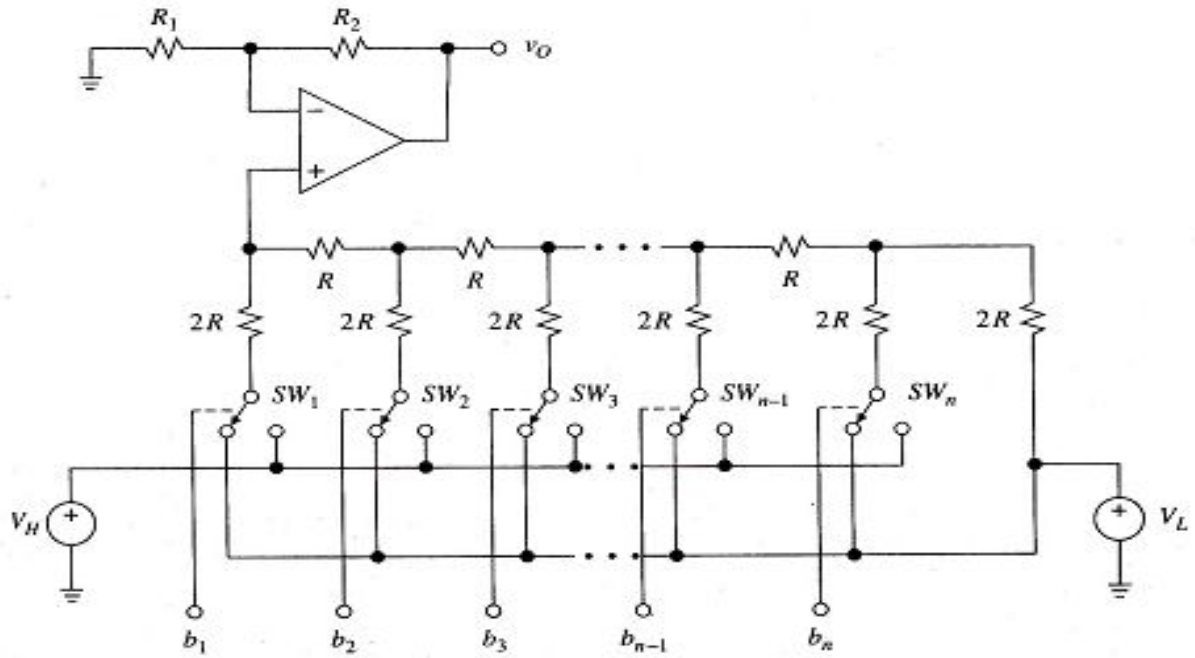
R–2R Ladder DAC

Binary	Output voltage
000	0.00 V
001	-1.25 V
010	-2.50 V
011	-3.75 V
100	-5.00 V
101	-6.25 V
110	-7.50 V
111	-8.75 V

Inverted or Current Mode DAC



Voltage Mode DAC

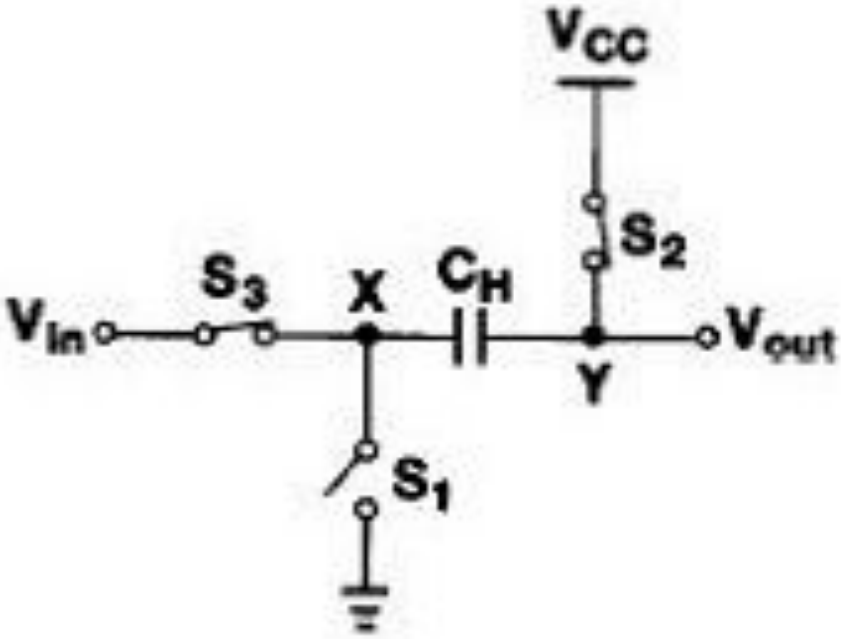


Switches for DAC

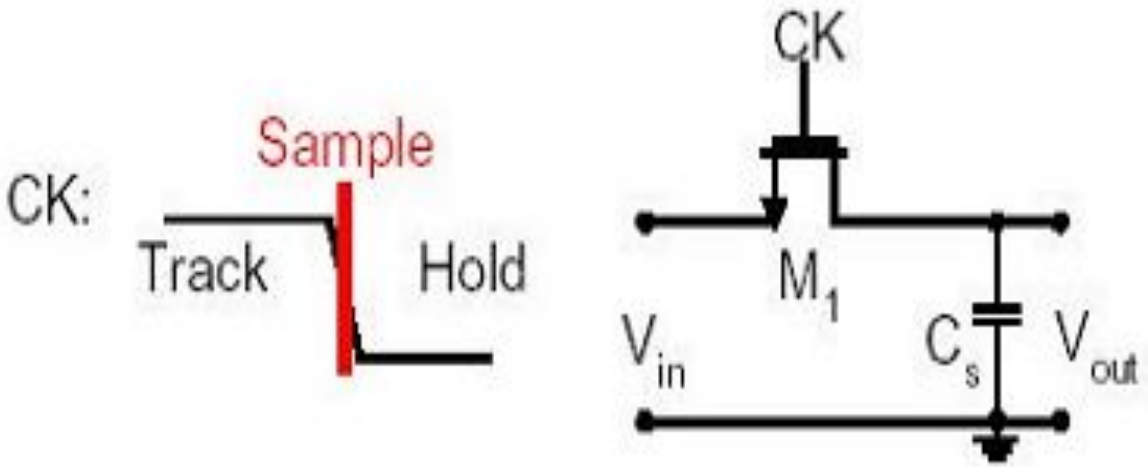
- Switches using Over-driven Emitter Followers
- Switches using MOS Transistor-Totem Pole

  MOSFET switch and CMOS Inverter Switch
- CMOS Switch for Multiplying type DACs
- CMOS Transmission gate switches

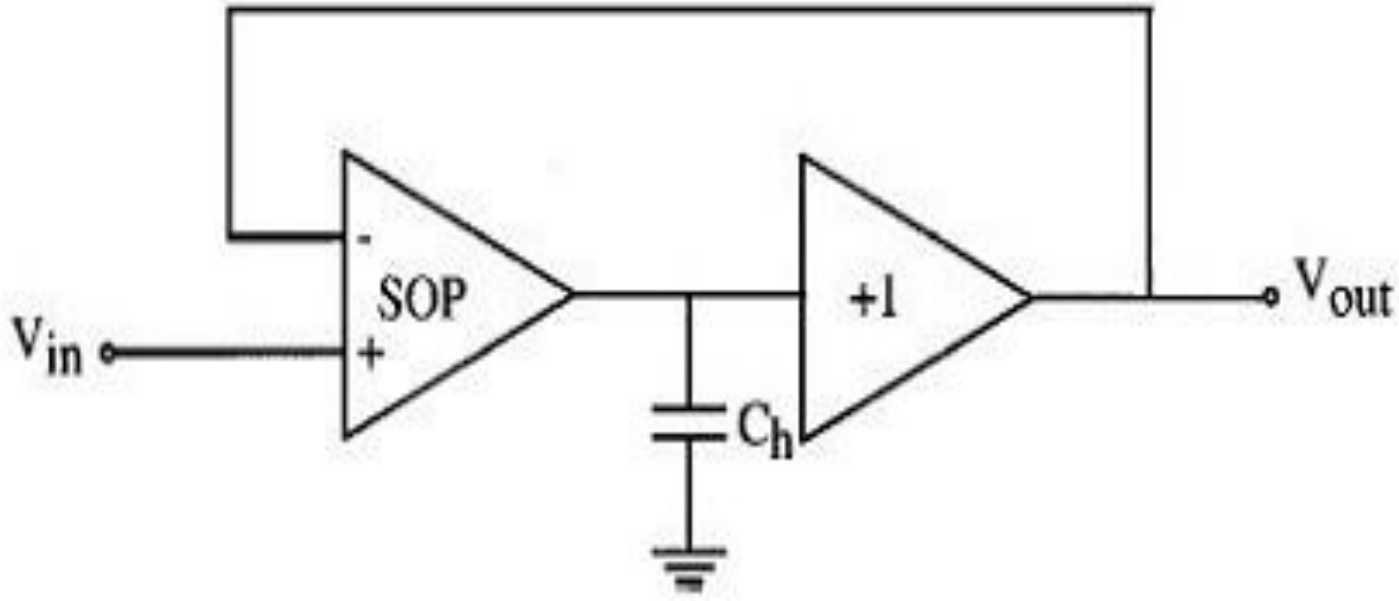
Series Sampling



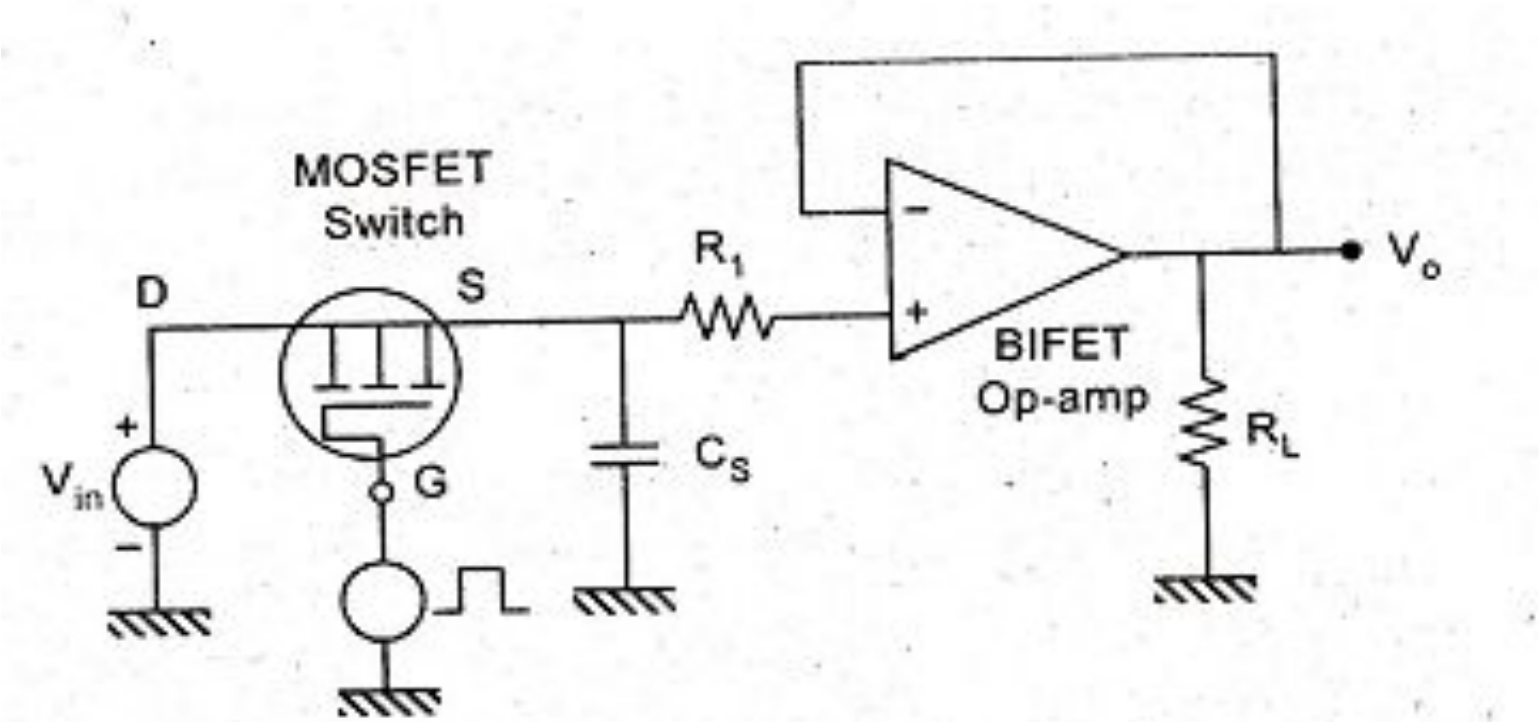
High Speed Sample & Hold circuit



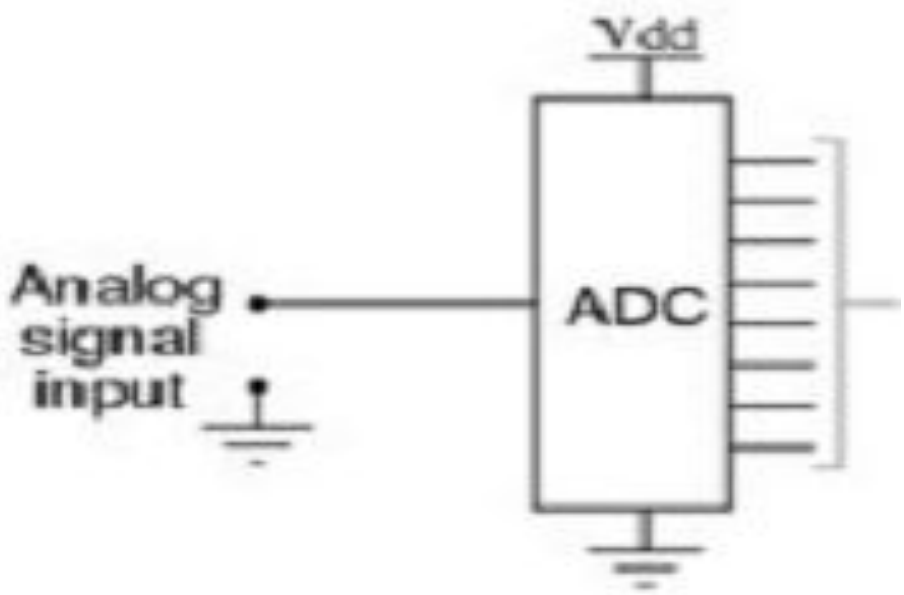
Switched op-amp based Sample and Hold Circuit



Sample and Hold circuit with MOSFET as a switch

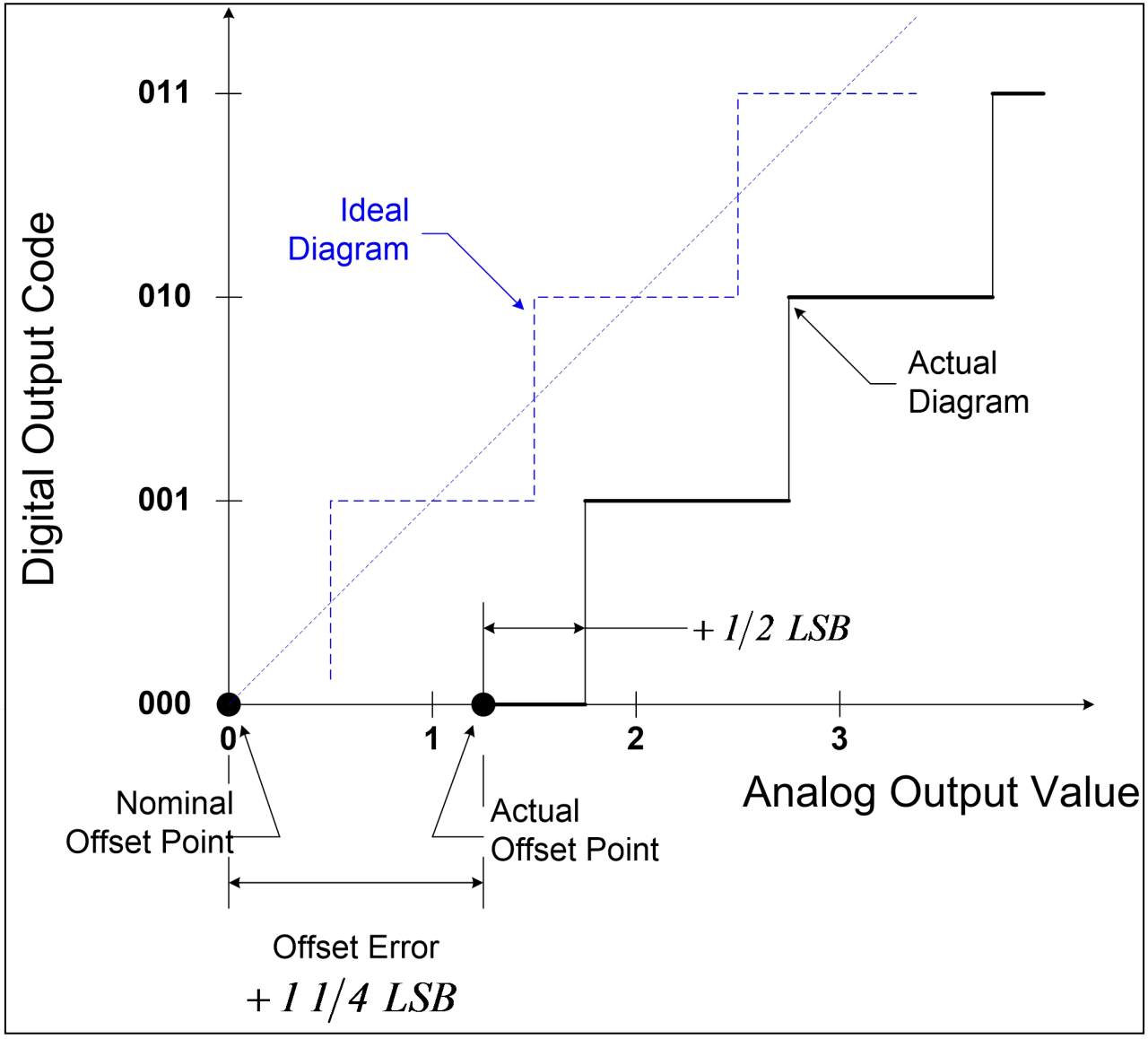


Analog to Digital Converters



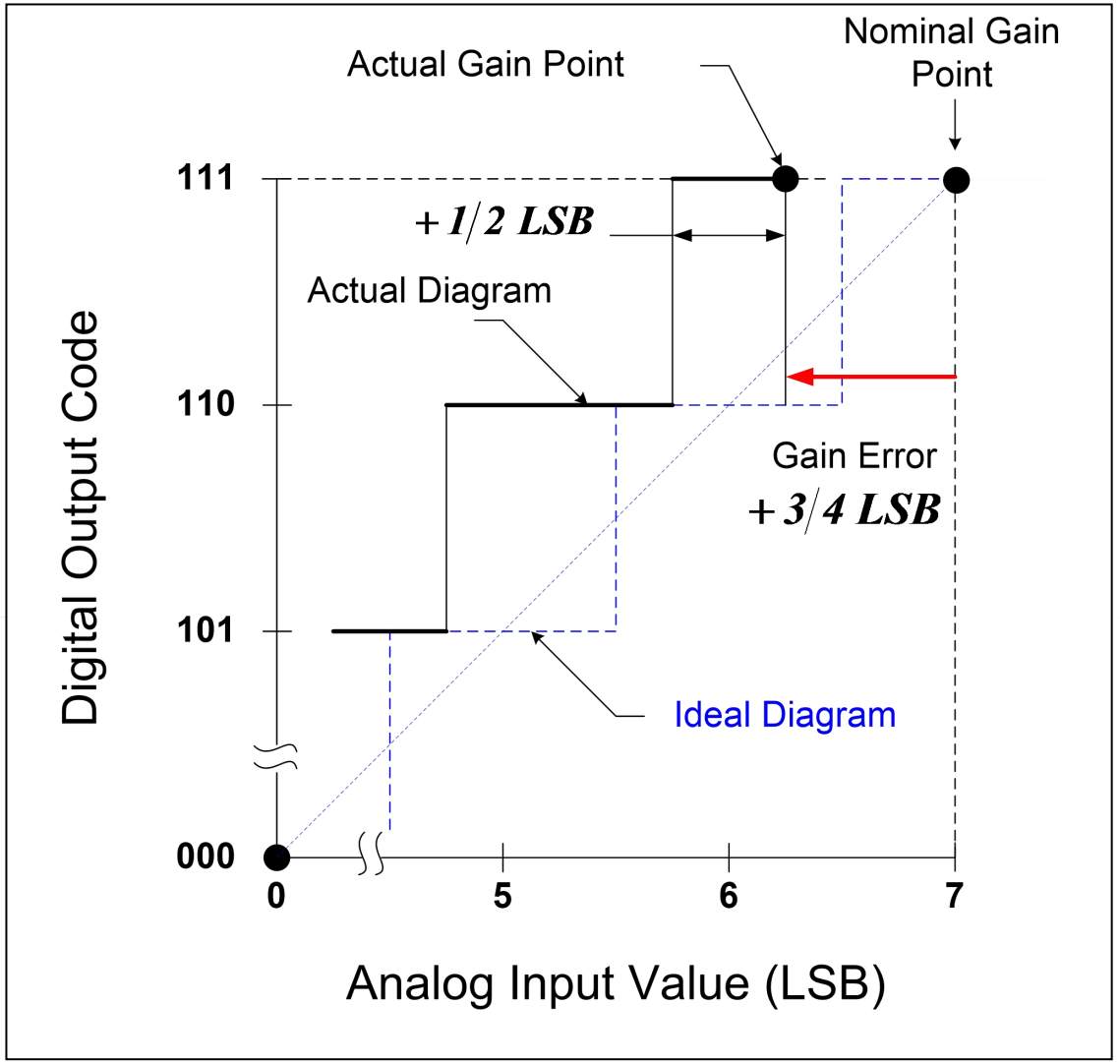
Offset Error – ADC

The offset error is efined as the difference between the nominal and actual offset points.



Gain Error – ADC

The gain error is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale,

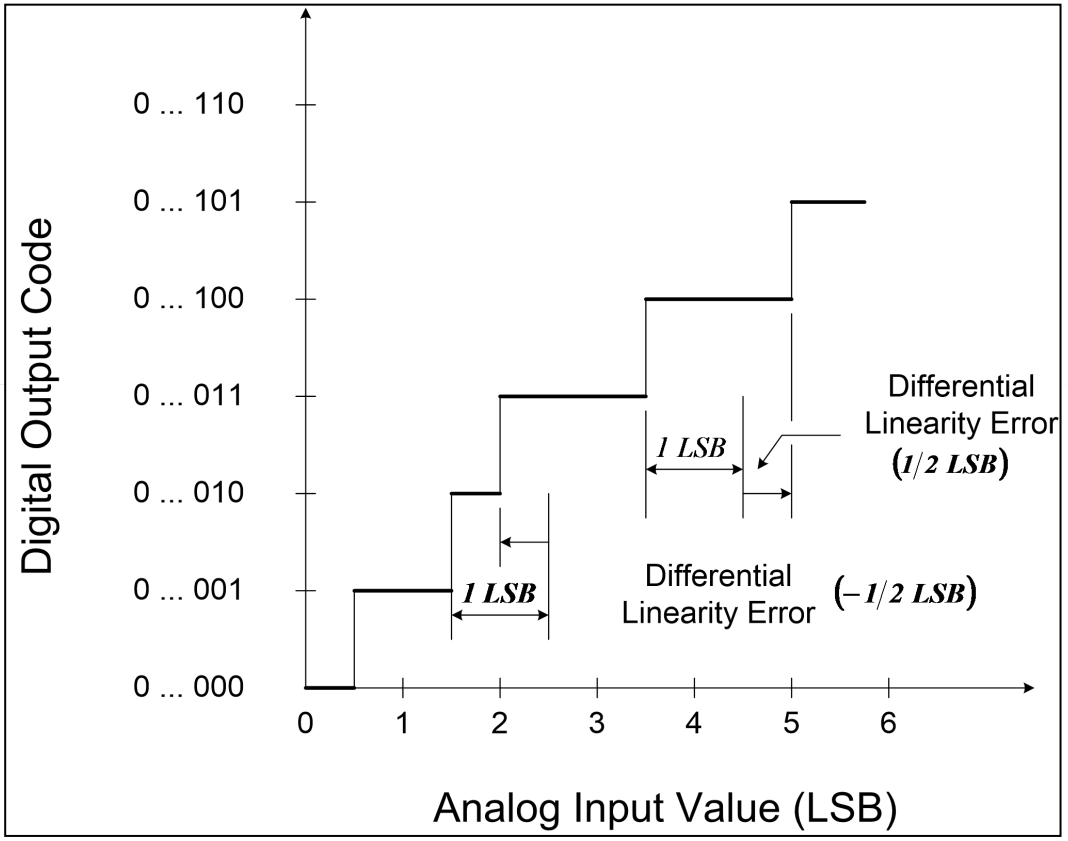


Differential Nonlinearity (DNL) Error – ADC

DNL is the **difference between an actual step width** (for an ADC) **and the ideal value of 1 LSB**. Therefore if the step width is exactly 1 LSB, then the differential nonlinearity error is zero.

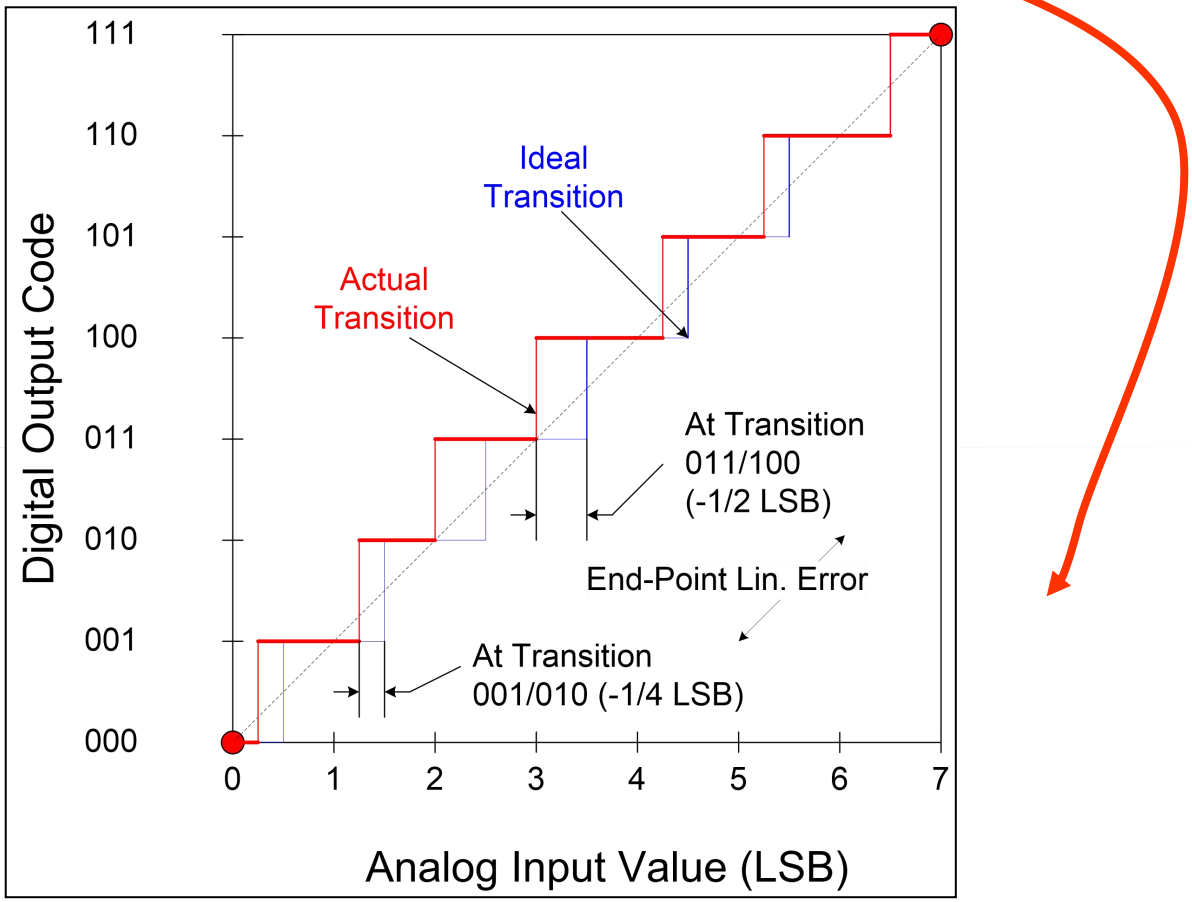
If the DNL exceeds 1 LSB $\Rightarrow$ **nonmonotonic** (this means that the magnitude of the output gets smaller for an increase in the magnitude of the input)

If the DNL error of – 1 LSB there is also a possibility that there can be **missing codes** i.e., one or more of the possible 2n binary codes are never output.



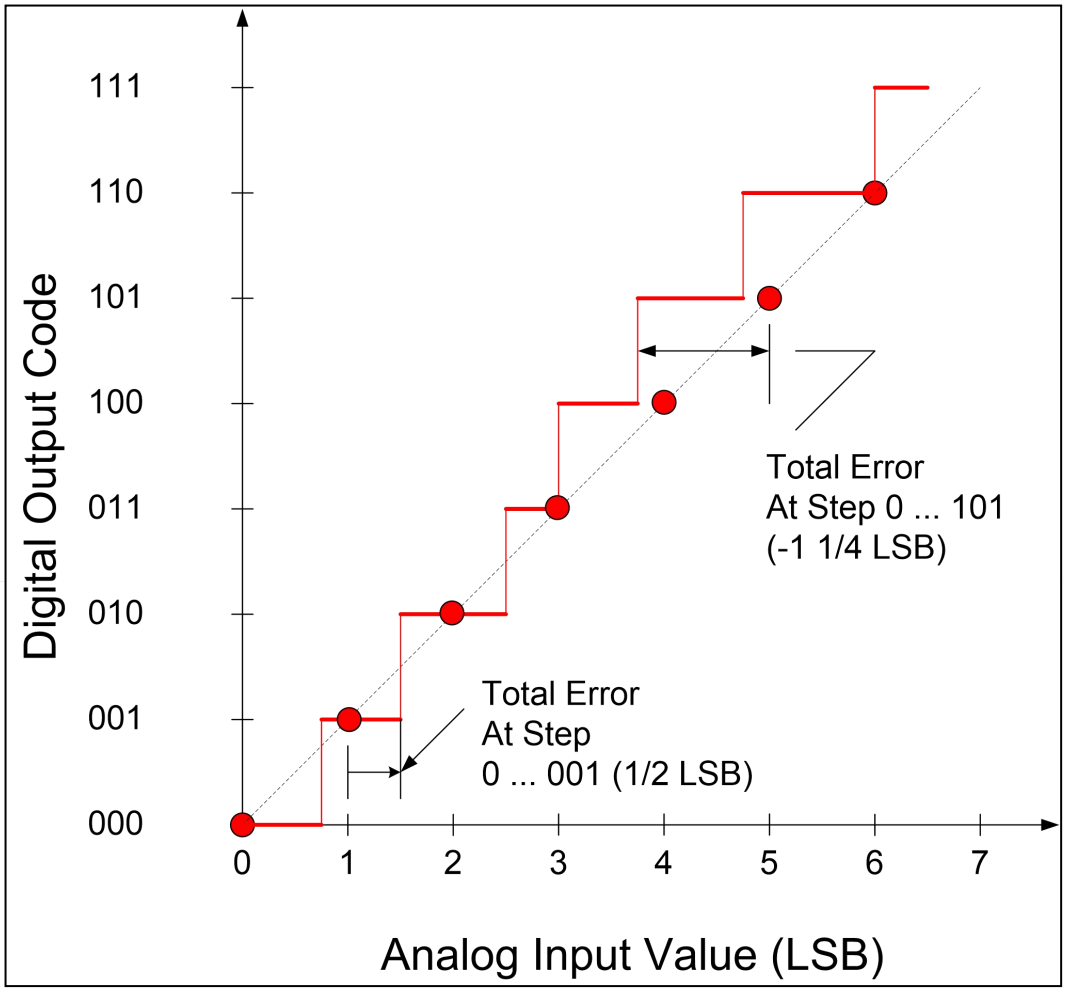
Integral Nonlinerity (INL) Error – ADC

The integral nonlinearity error shown in Figure is **the deviation of the values on the actual transfer function from a straight line**.
This straight line can be either a **best straight line** which is drawn so as to minimize these deviations or
it can be a line drawn between **the end points** of the transfer function once the gain and offset errors have been nullified (end-point linearity)



Absolute Accuracy (Total) Error –ADC

The absolute accuracy or total error of an ADC as shown in Figure is the maximum value of the difference between an analog value and the ideal midstep value.
It includes offset, gain, and integral linearity errors and also the quantization error in the case of an ADC



Resolution

The resolution refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to number of bits. It is given as $1/2^n$, where 'n' is the number of bits in the digital output word. As it is clear, that the resolution can be improved by increasing the number of bits or the number of bits representing the given analog input voltage.

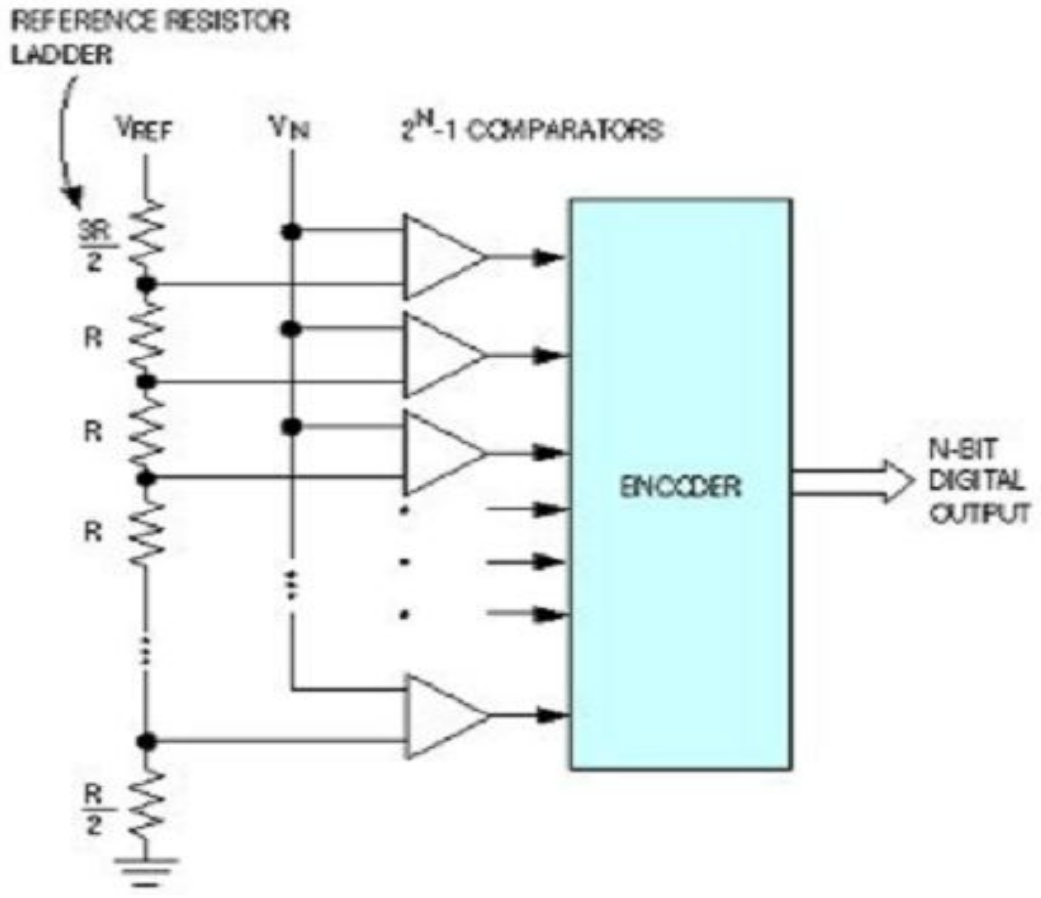
Resolution can also be defined as the ratio of change in the value of input voltage V_i, needed to change the digital output by 1 LSB. It is given as

$$\text{Resolution} = V_{iFS} / (2^n - 1)$$

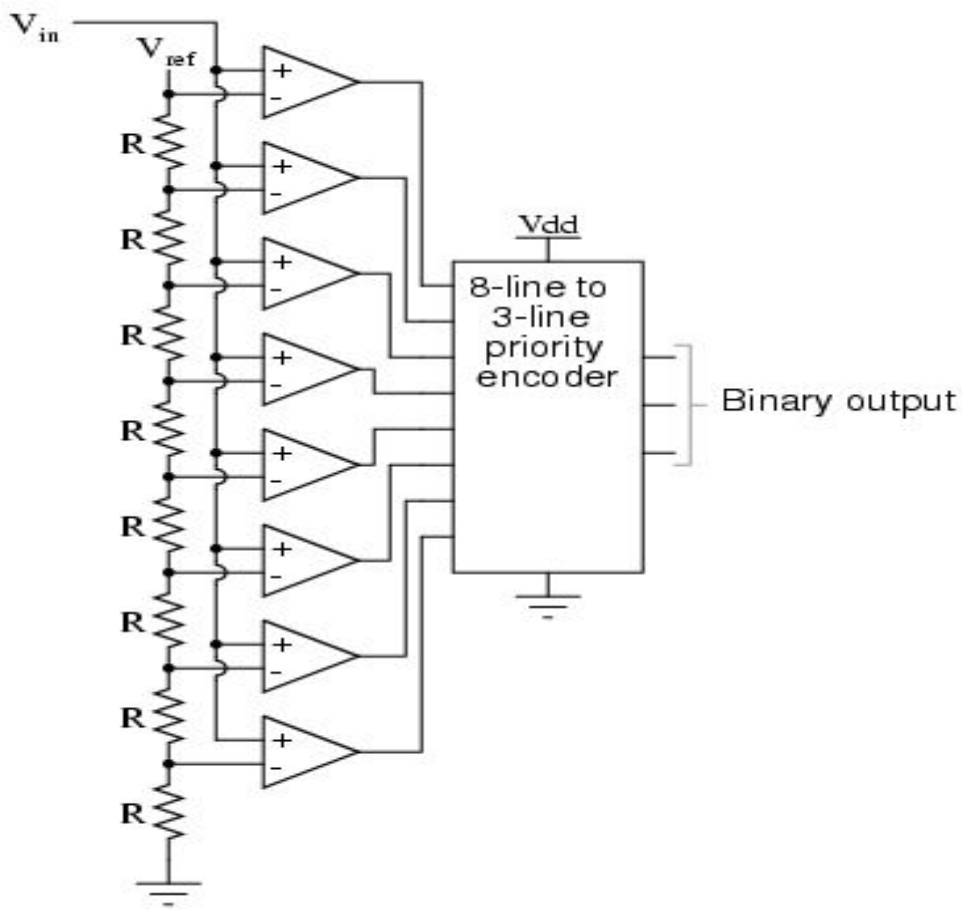
Where 'V_{iFS}' is the full-scale input voltage.

'n' is the number of output bits.

Flash type ADC



Flash ADC Circuit



Flash ADC Circuit

Advantages

- Simplest in terms of operational theory
- Most efficient in terms of speed, very fast
  - limited only in terms of comparator and gate propagation delays

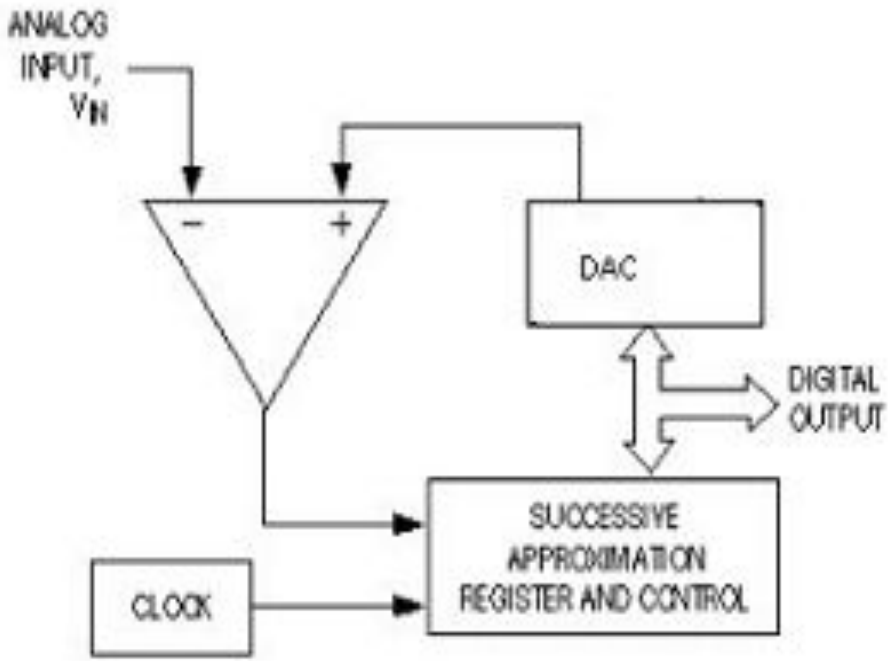
Disadvantages

- Lower resolution
- Expensive
- For each additional output bit, the number of comparators is doubled
  - i.e. for 8 bits, 256 comparators needed

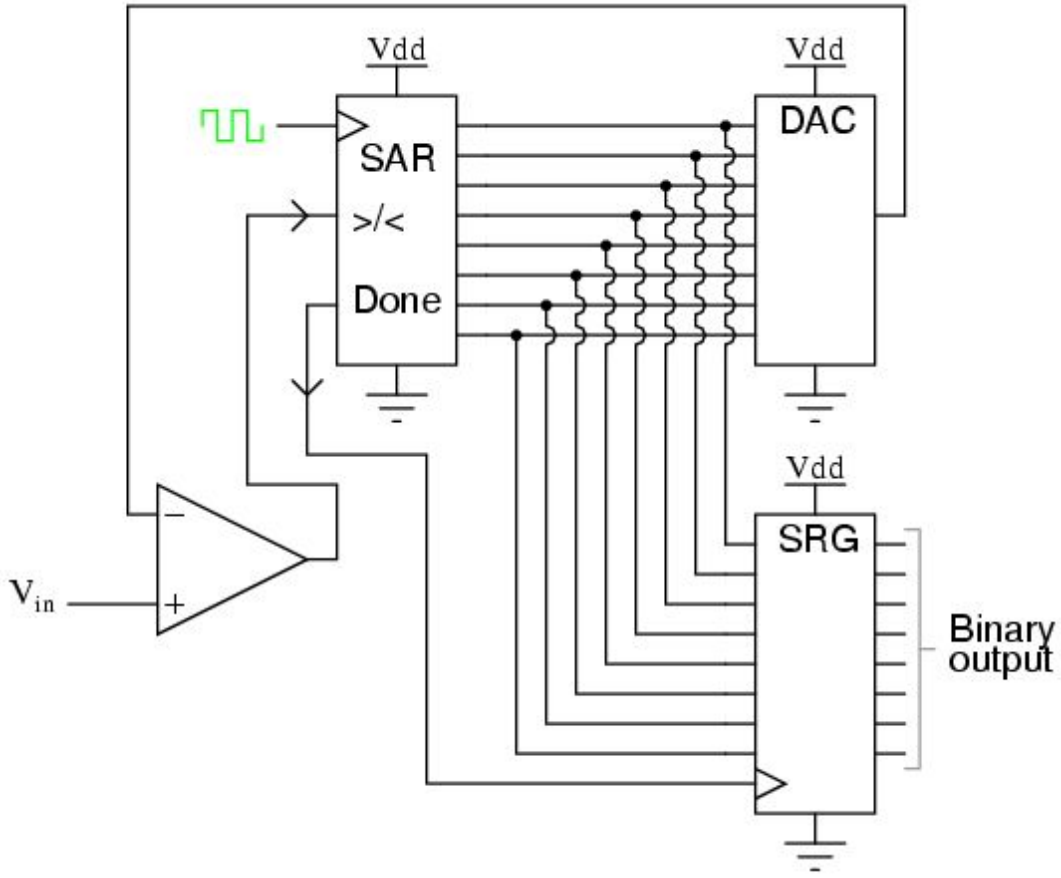
Successive Approximation ADC

- A Successive Approximation Register (SAR) is added to the circuit
- Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the MSB and finishing at the LSB.
- The register monitors the comparators output to see if the binary count is greater or less than the analog signal input and adjusts the bits accordingly

Successive Approximation ADC



Successive Approximation ADC Circuit



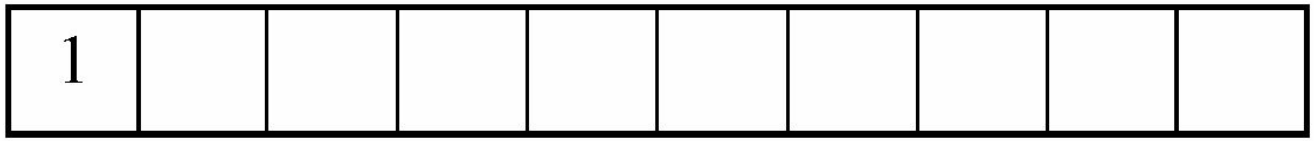
Successive Approximation Example

- 10 bit resolution or 0.0009765625V of Vref
- Vin= .6 volts
- Vref=1volts
- Find the digital value of Vin

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625

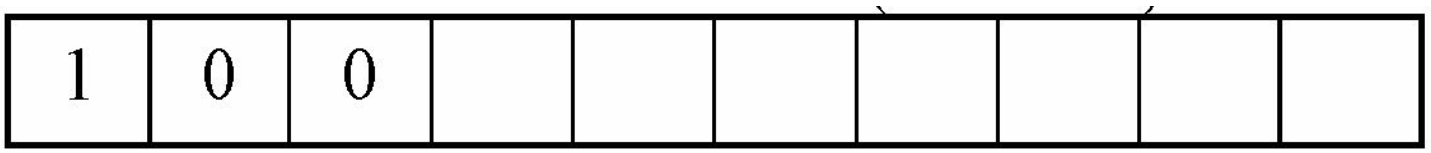
Successive Approximation

- MSB (bit 9)
  - Divided V_{ref} by 2
  - Compare V_{ref} /2 with V_{in}
  - If V_{in} is greater than V_{ref} /2 , turn MSB on (1)
  - If V_{in} is less than V_{ref} /2 , turn MSB off (0)
  - V_{in} =0.6V and V=0.5
  - Since V_{in}>V, MSB = 1 (on)



Successive Approximation

- Next Calculate MSB-1 (bit 8)
  - Compare V_{in}=0.6 V to V=V_{ref}/2 + V_{ref}/4= 0.5+0.25 =0.75V
  - Since 0.6<0.75, MSB is turned off
- Calculate MSB-2 (bit 7)
  - Go back to the last voltage that caused it to be turned on (Bit 9) and add it to V_{ref}/8, and compare with V_{in}
  - Compare V_{in} with (0.5+V_{ref}/8)=0.625
  - Since 0.6<0.625, MSB is turned off



Successive Approximation

- Calculate the state of MSB-3 (bit 6)
  - Go to the last bit that caused it to be turned on (In this case MSB-1) and add it to $V_{ref}/16$, and compare it to V_{in}
  - Compare V_{in} to $V = 0.5 + V_{ref}/16 = 0.5625$
  - Since $0.6 > 0.5625$, MSB-3=1 (turned on)

MSB	MSB-1	MSB-2	MSB-3	…					
1	0	0	1						

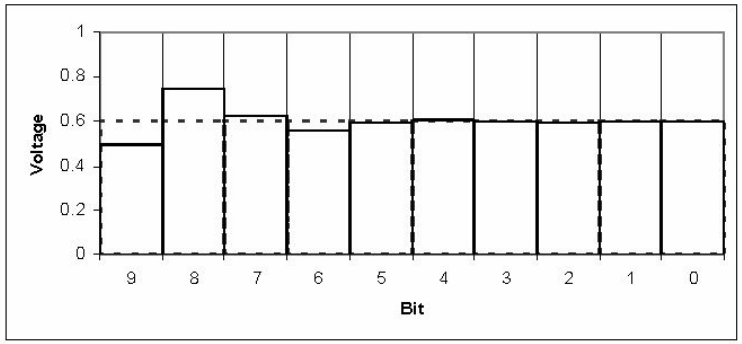
Successive Approximation

- This process continues for all the remaining bits.

•Digital Results:

MSB	MSB-1	MSB-2	MSB-3	…					LSB
1	0	0	1	1	0	0	1	1	0

•Results: $\frac{1}{2}+\frac{1}{16}+\frac{1}{32}+\frac{1}{256}+\frac{1}{512}=.599609375\ \text{V}$



Successive Approximation ADC

Advantages

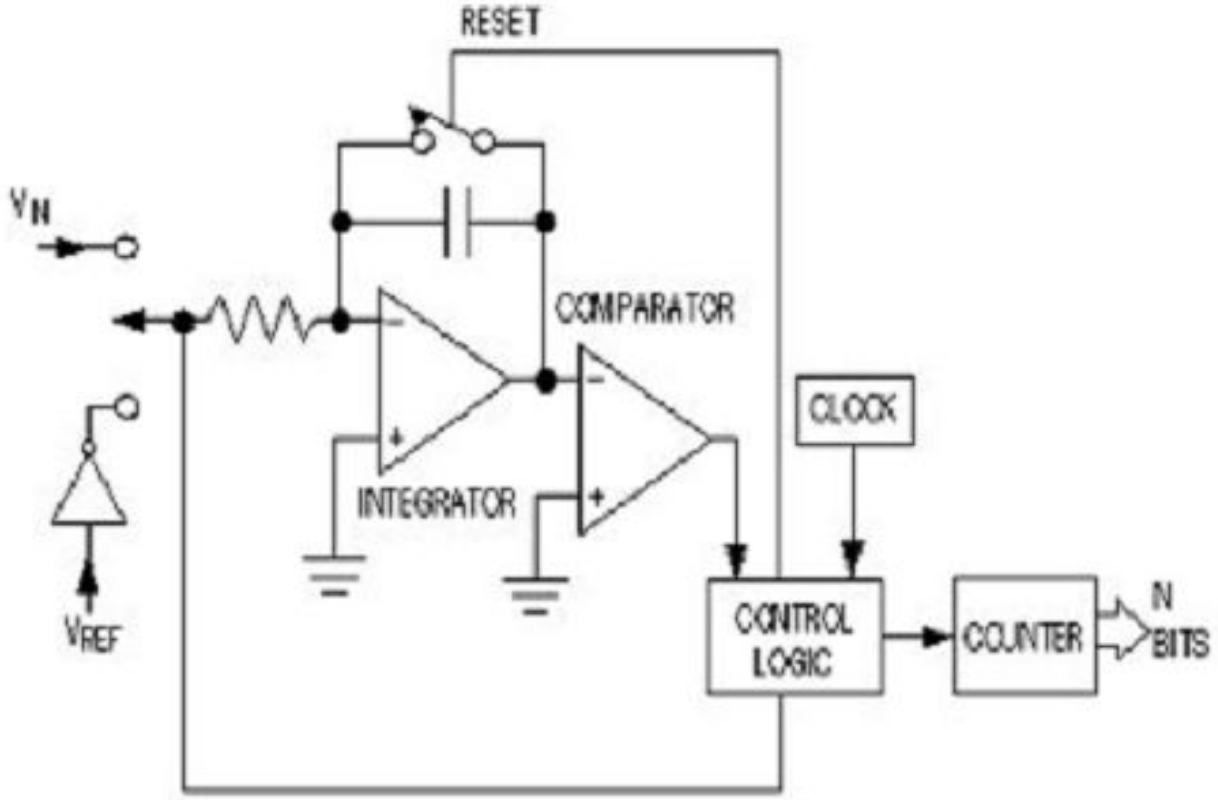
- Capable of high speed and reliable
- Medium accuracy compared to other ADC types
- Good tradeoff between speed and cost

- Capable of outputting the binary number in serial (one bit at a time) format.

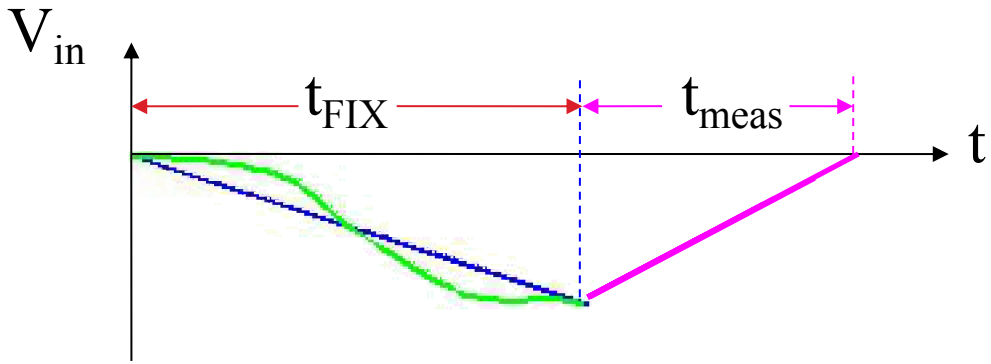
Disadvantages

- Higher resolution successive approximation ADC's will be slower
- Speed limited to ~5Msps

Integrating ADC



Dual Slope Converter



- The sampled signal charges a capacitor for a fixed amount of time
- By integrating over time, noise integrates out of the conversion
- Then the ADC discharges the capacitor at a fixed rate with the counter counts the ADC's output bits. A longer discharge time results in a higher count

Dual Slope Converter

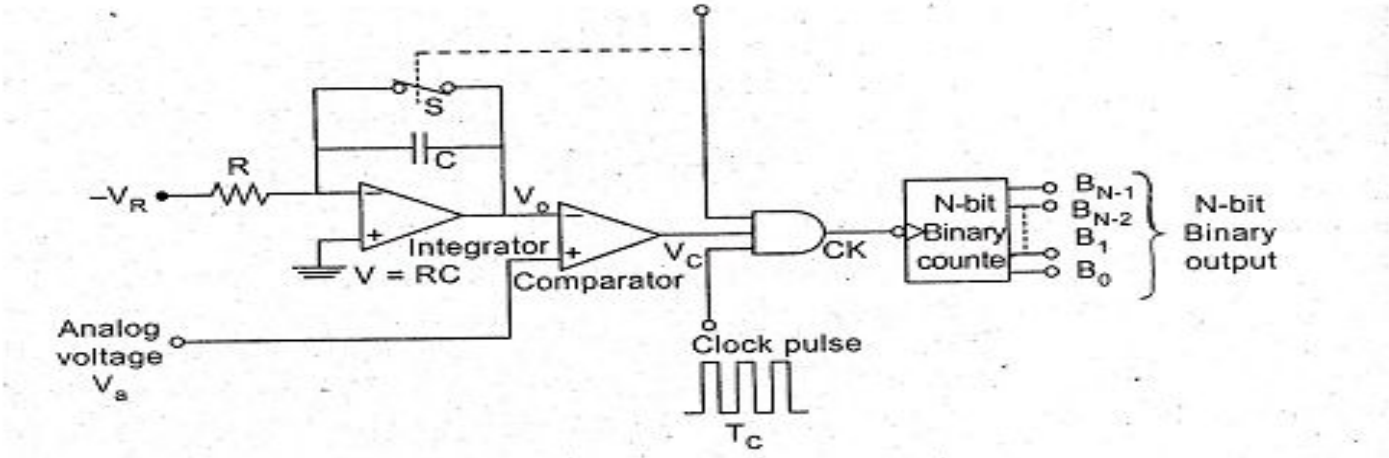
Advantages

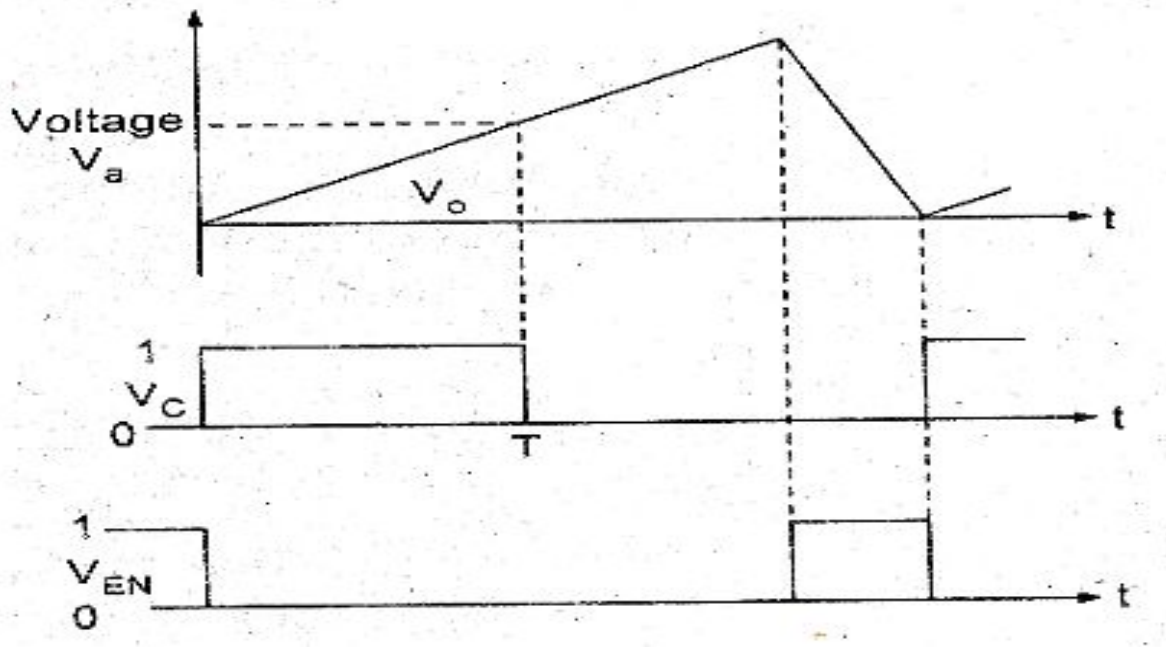
- Input signal is averaged
- Greater noise immunity than other ADC types
- High accuracy

Disadvantages

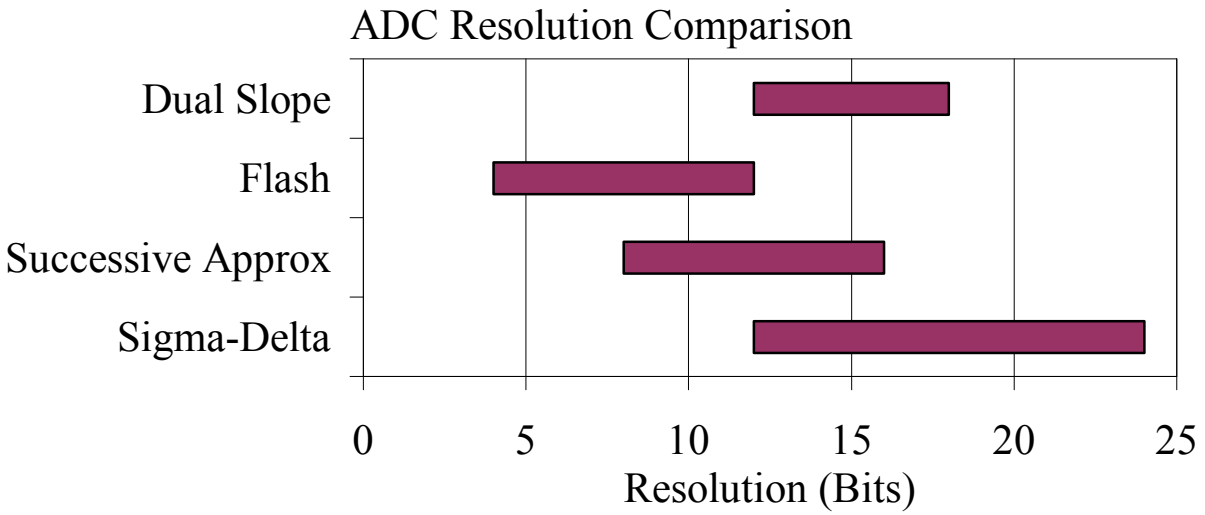
- Slow
- High precision external components required to achieve accuracy

A/D using Voltage to Time conversion





ADC Types Comparison



Type	Speed (relative)	Cost (relative)
Dual Slope	Slow	Med
Flash	Very Fast	High
Successive Appox	Medium – Fast	Low
Sigma-Delta	Slow	Low

Analog Switches

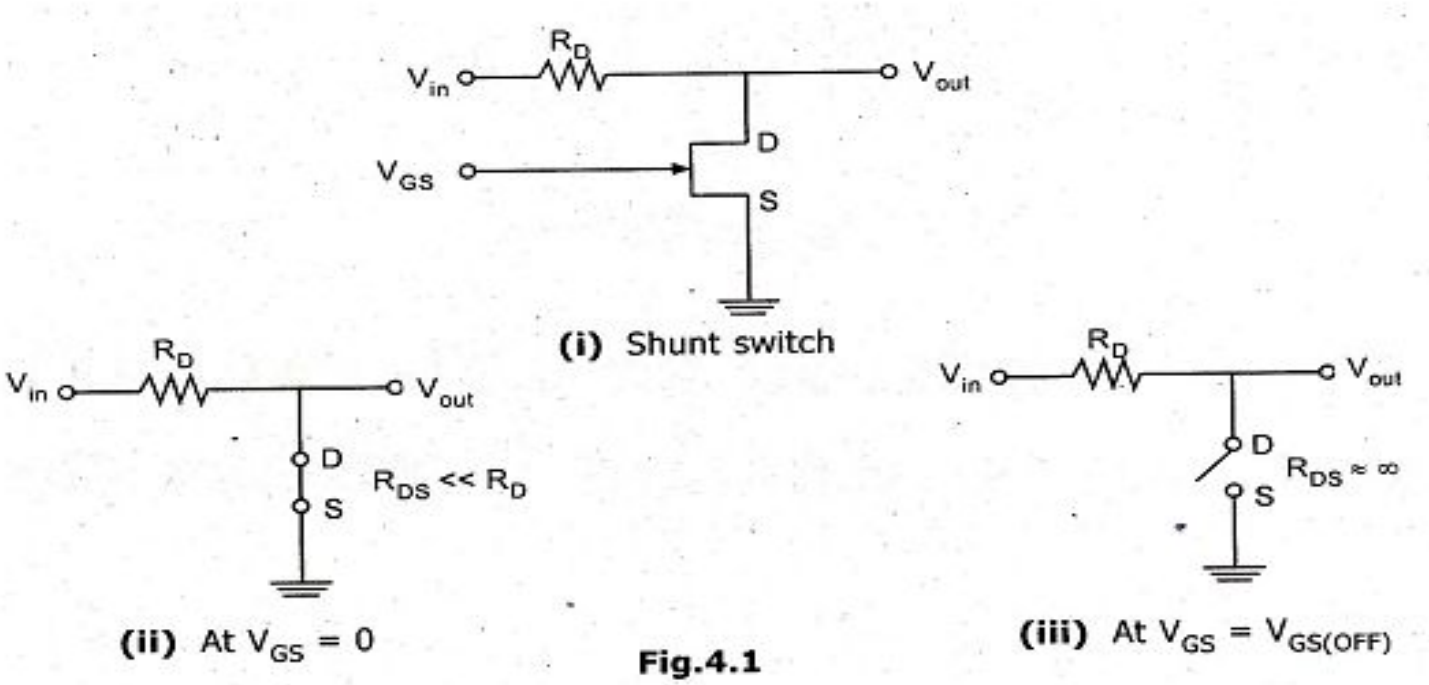


Fig.4.1

Analog Switches

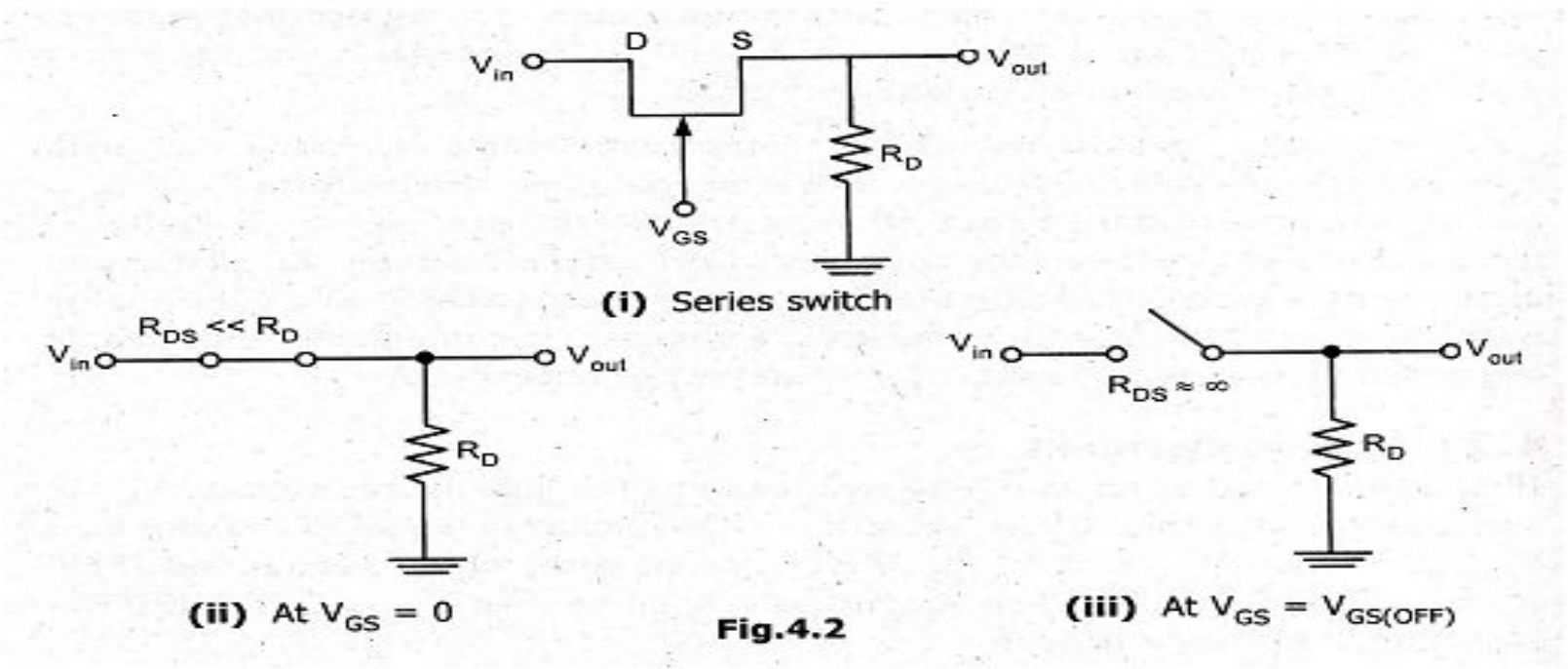
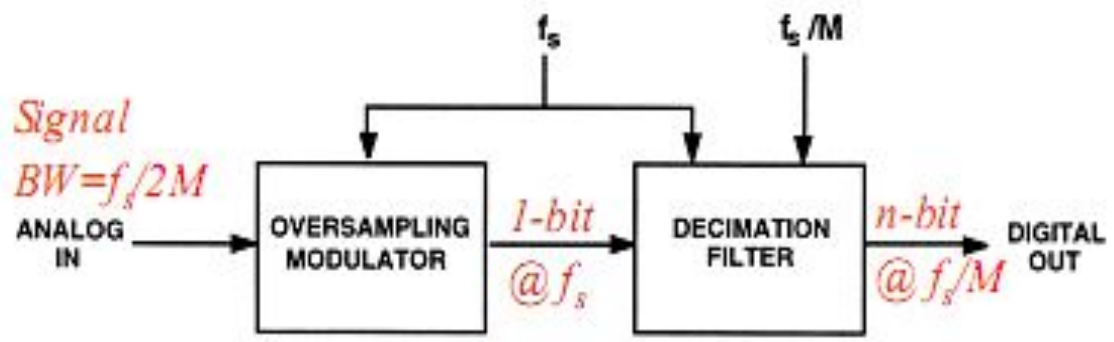


Fig.4.2

Oversampling A/D converters

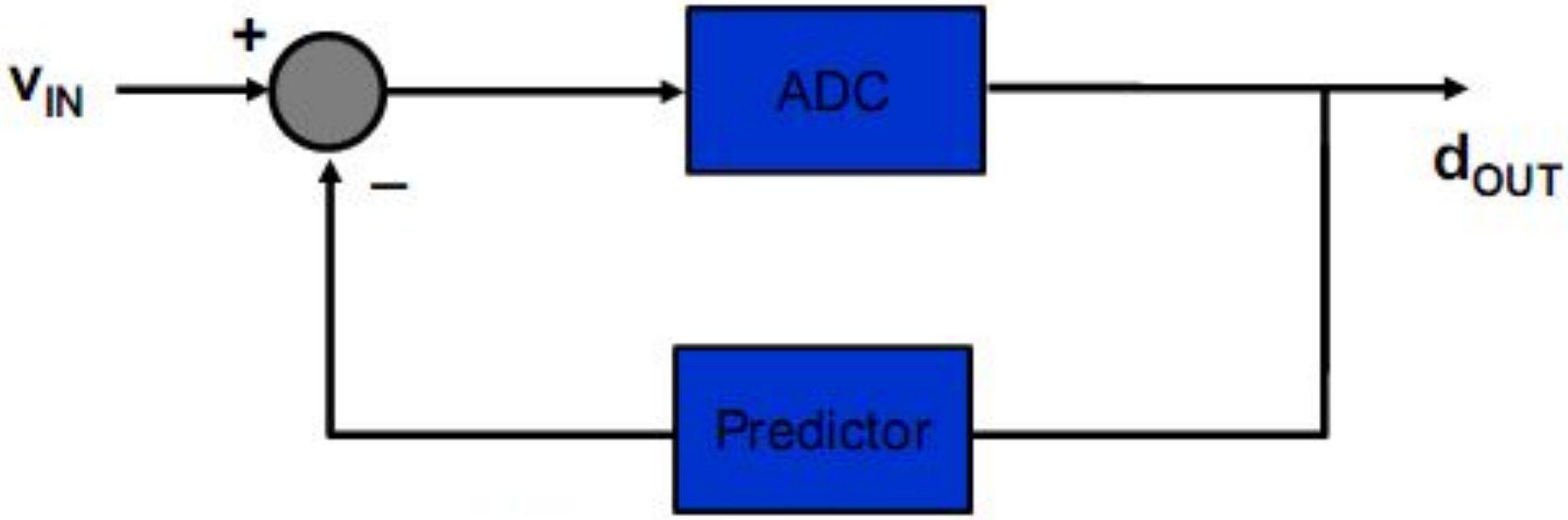


f_s = Sampling Rate

M = Oversampling Ratio

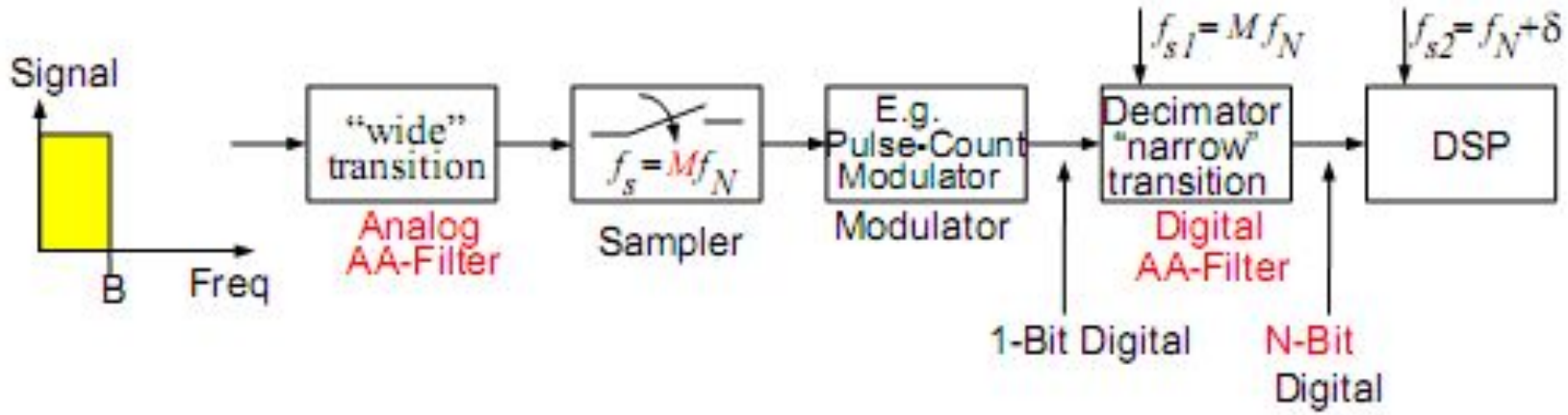
- Analog front-end → oversampled noise-shaping modulator
  - •Converts original signal to a 1-bit digital output at the high rate of $(2MXf_{signal})$
- Digital back-end → digital filter
  - •Removes out-of-band quantization noise
  - •Provides anti-aliasing to allow re-sampling @ lower sampling rate

Oversampled ADC
Predictive Coding



- Quantize the difference signal rather than the signal itself
- Smaller input to ADC → Buy dynamic range
- Only works if combined with oversampling
- 1-Bit digital output
- Digital filter computes "average" →n-Bit output

Oversampled ADC



Decimator:

- Digital (low-pass) filter
- Removes quantization error for f > B
- Provides most anti-alias filtering
- Narrow transition band, high-order
- 1-Bit input, N-Bit output (essentially computes "average")

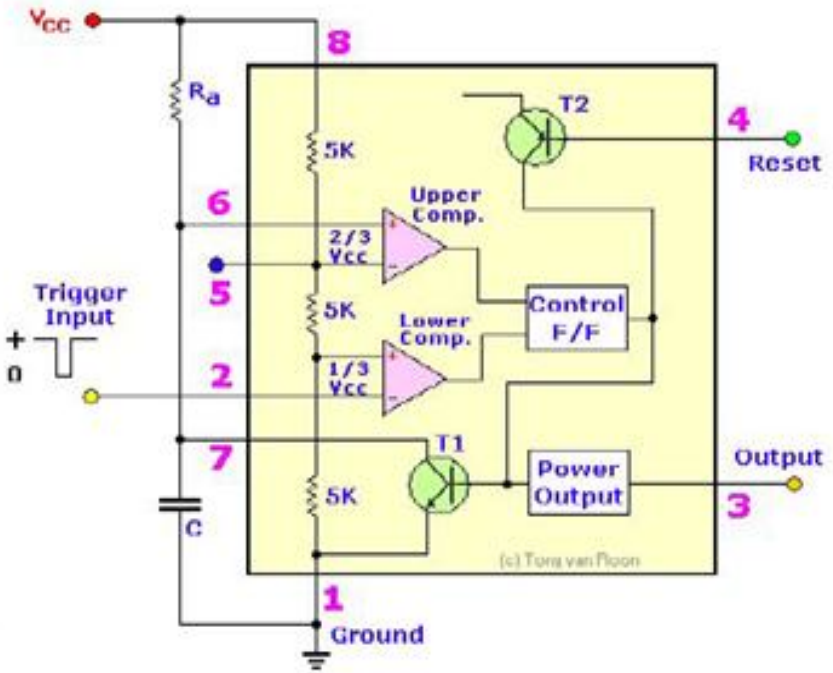
UNIT-V

SPECIAL FUNCTION ICS

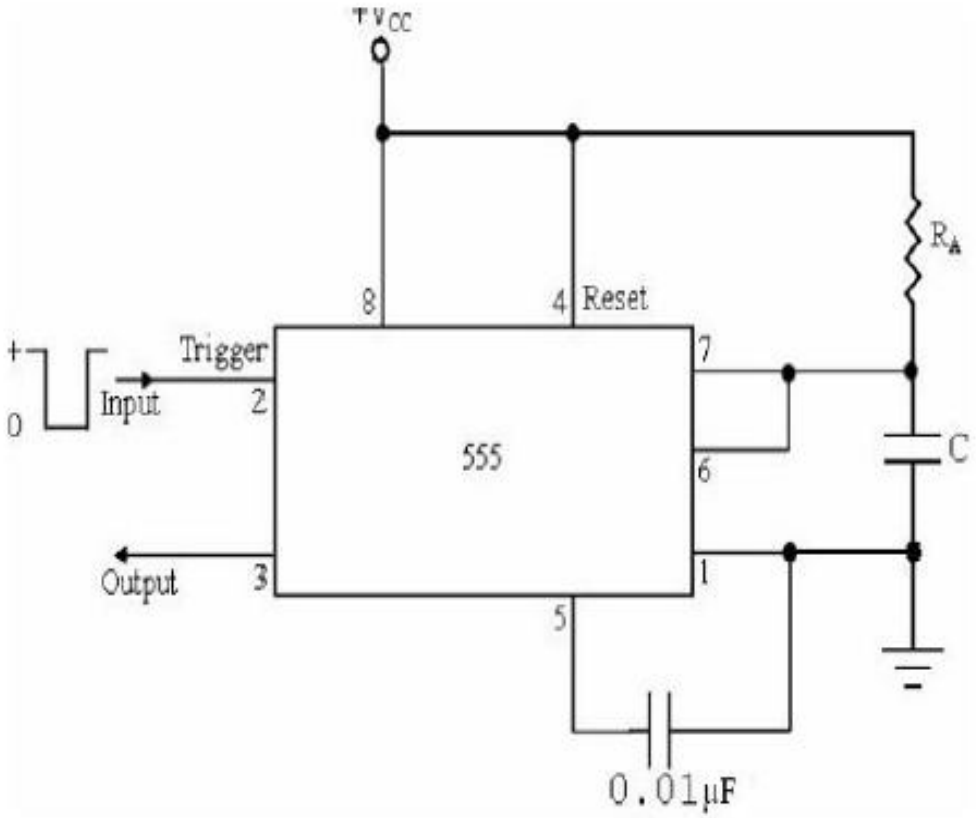
555 Timer

- The 555 timer IC is an integrated circuit (chip) used in a variety of timer, pulse generation, and oscillator applications.
- The 555 is used to provide time delays, as an oscillator, and as a flip-flop element.
- It gets its name from the three 5k ohm resistors which give the two comparators reference voltage.
- Depending on the manufacturer, the standard 555 package includes 25 transistors, 2 diodes and 15 resistors on a silicon chip installed in an 8-PIN DIP (Dual in-line) package.

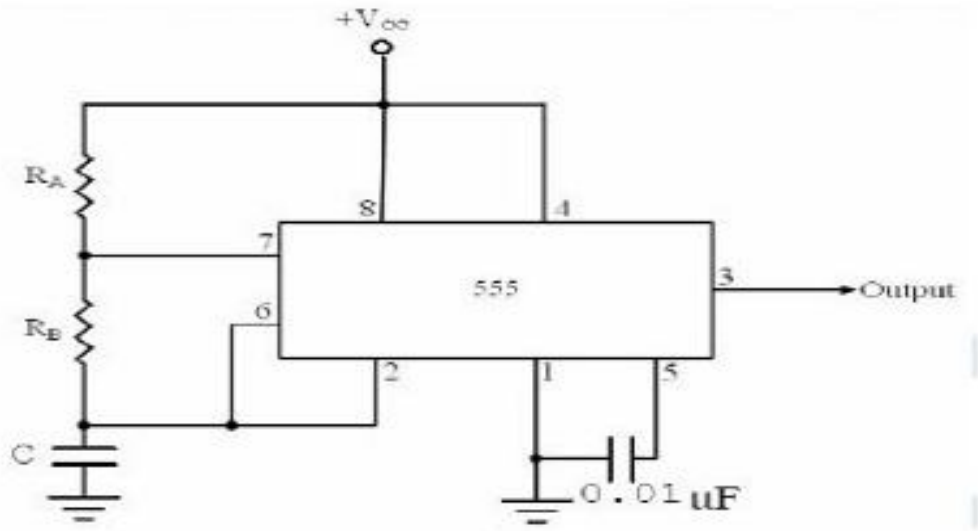
Block Diagram of 555 timer



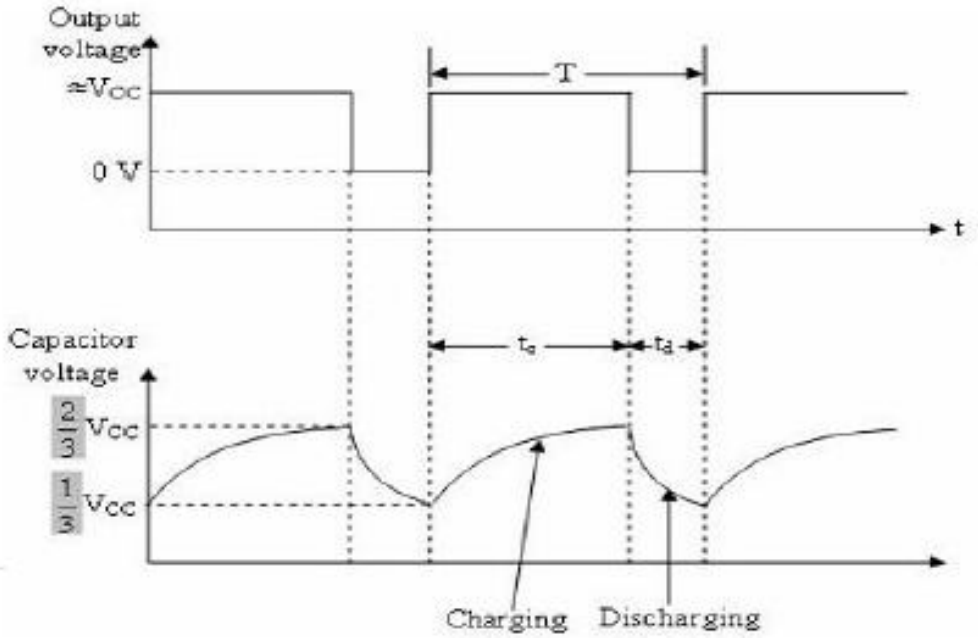
555 timer –Monostable Multivibrator



555 timer –Astable Multivibrator



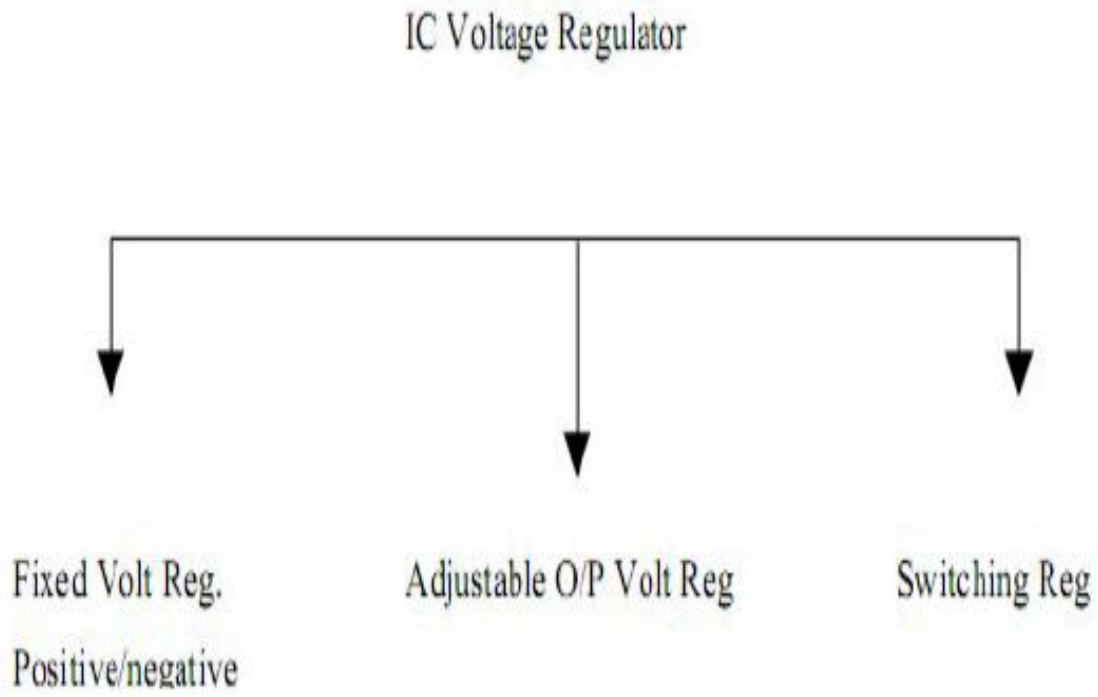
555 timer –Astable Multivibrator



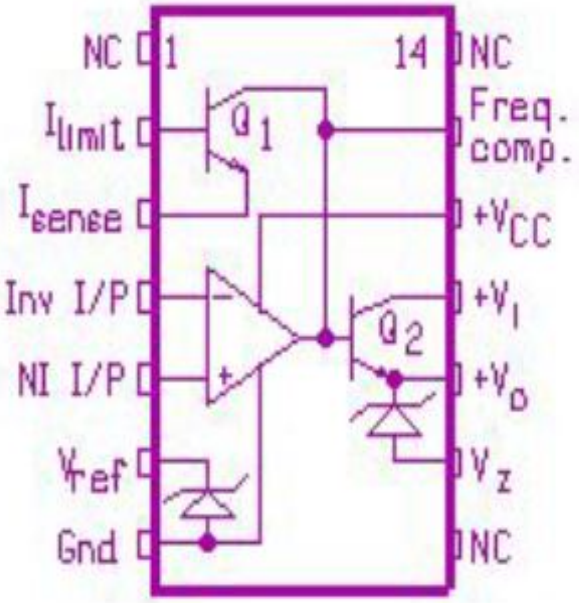
IC Voltage Regulators

- There are basically two kinds of IC voltage regulators:
  - Multipin type, e.g. LM723C
  - 3-pin type, e.g. 78/79XX
- Multipin regulators are less popular but they provide the greatest flexibility and produce the highest quality voltage regulation
- 3-pin types make regulator circuit design simple

Classification of IC Voltage regulator



Multipin IC Voltage Regulator



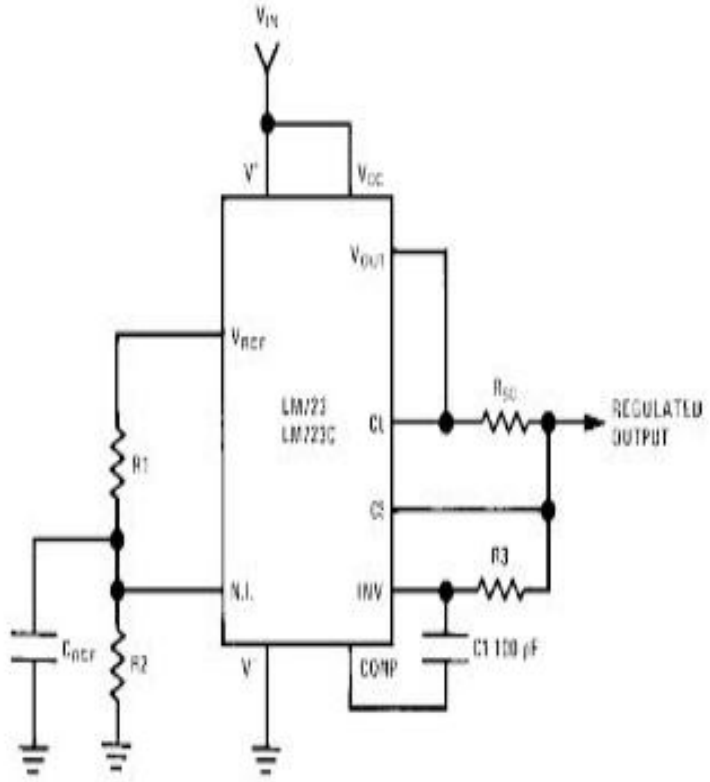
LM 723C Schematic

- The LM723 has an equivalent circuit that contains most of the parts of the op-amp voltage regulator discussed earlier.
- It has an internal voltage reference, error amplifier, pass transistor, and current limiter all in one IC package.

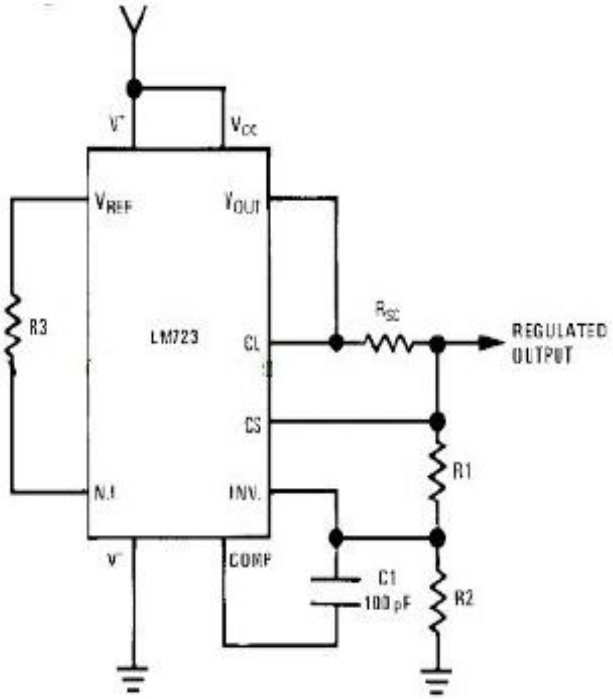
LM723 Voltage Regulator

- Can be either 14-pin DIP or 10-pin TO-100 can
- May be used for either +ve or -ve, variable or fixed regulated voltage output
- Using the internal reference (7.15 V), it can operate as a high-voltage regulator with output from 7.15 V to about 37 V, or as a low-voltage regulator from 2 V to 7.15 V
- Max. output current with heat sink is 150 mA
- Dropout voltage is 3 V (i.e. $V_{CC} > V_{o(max)} + 3$)

IC723 as a LOW voltage LOW current



IC723 as a HIGH voltage LOW current



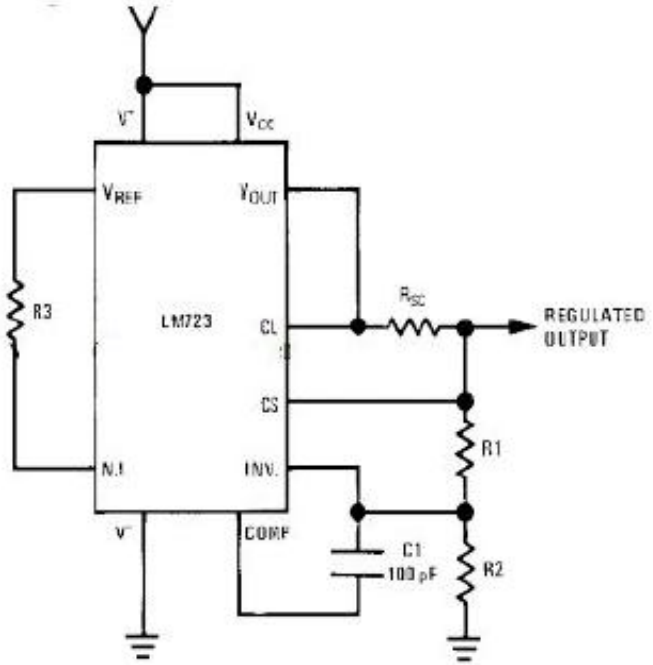
$$Vin = Vref = \frac{R2}{R1+R2} Vo$$

$$Vo = \frac{R1+R2}{R2} Vref$$

Or

$$Vo = [1 + \frac{R1}{R2}] Vref$$

IC723 as a HIGH voltage HIGH current



$$Vin = Vref = \frac{R2}{R1+R2} Vo$$

$$Vo = \frac{R1+R2}{R2} Vref$$

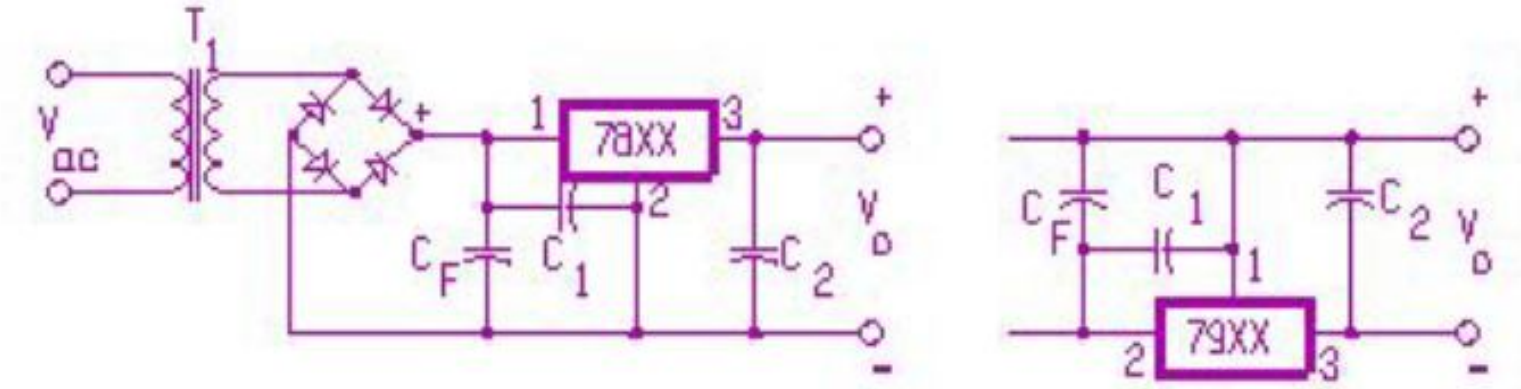
Or

$$Vo = [1 + \frac{R1}{R2}] Vref$$

Three-Terminal Fixed Voltage Regulators

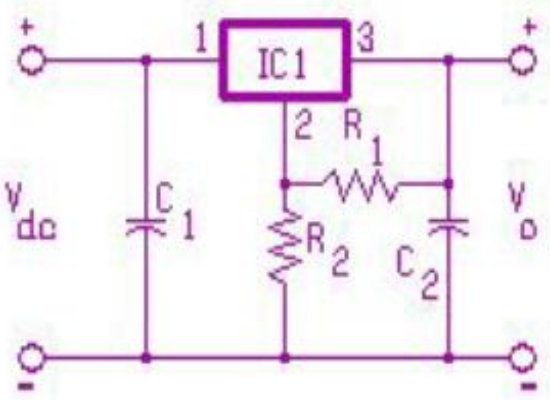
- Less flexible, but simple to use
- Come in standard TO-3 (20 W) or TO-220 (15 W) transistor packages
- 78/79XX series regulators are commonly available with 5, 6, 8, 12, 15, 18, or 24 V output
- Max. output current with heat sink is 1 A
- Built-in thermal shutdown protection
- 3-V dropout voltage; max. input of 37 V
- Regulators with lower dropout, higher in/output, and better regulation are available.

Basic Circuits With 78/79XX Regulators



- Both the 78XX and 79XX regulators can be used to provide +ve or –ve output voltages
- C_1 and C_2 are generally optional. C_1 is used to cancel any inductance present, and C_2 improves the transient response. If used, they should preferably be either 1 μF tantalum type or 0.1 μF mica type capacitors.

78XX Floating Regulator



- It is used to obtain an output > the V_{reg} value up to a max.of 37 V.
- R_1 is chosen so that $R_1 \leq 0.1\ V_{reg}/I_Q$, where I_Q is the

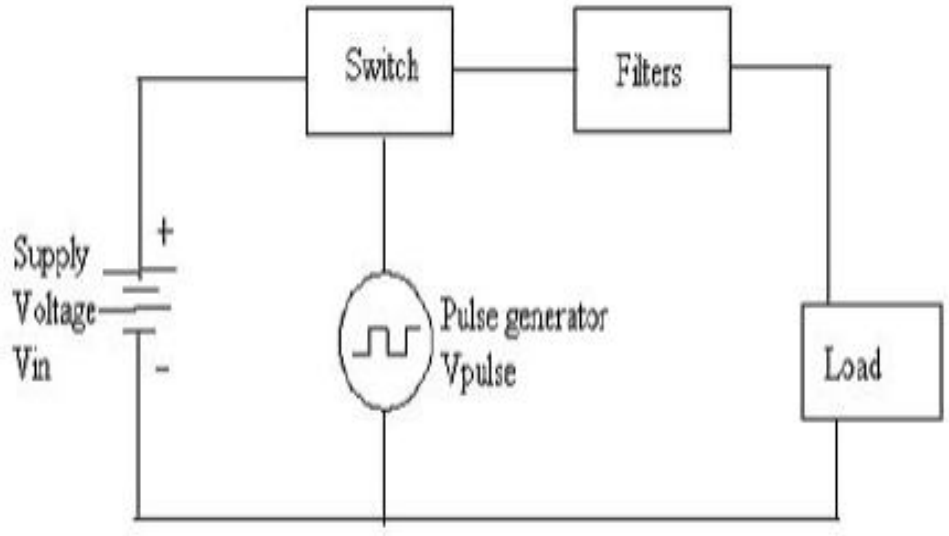
$$V_o = V_{reg} + \left(\frac{V_{reg}}{R_1} + I_Q\right)R_2 \quad \text{or} \quad R_2 = \frac{R_1(V_o - V_{reg})}{V_{reg} + I_Q R_1}$$

t of

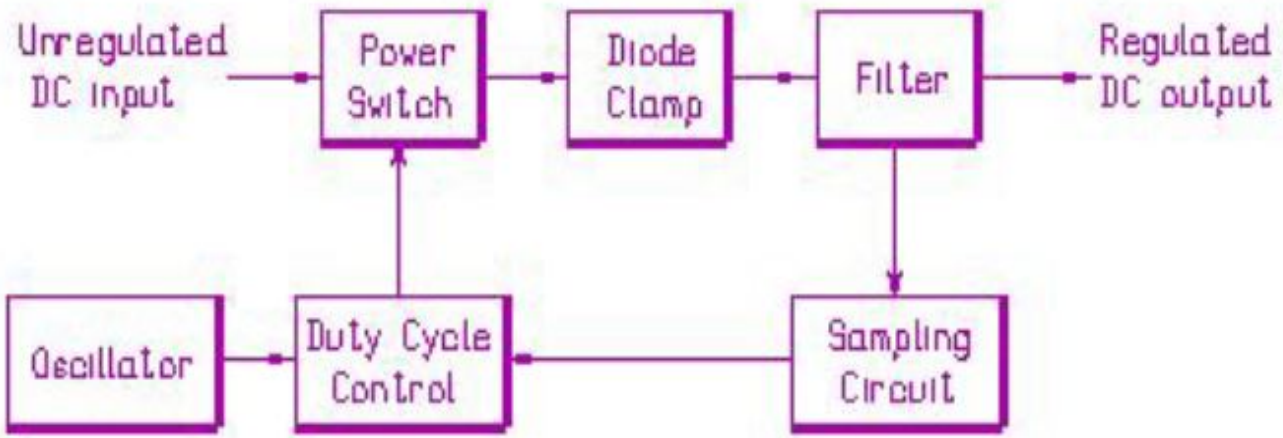
3-Terminal Variable Regulator

- The floating regulator could be made into a variable regulator by replacing R_2 with a pot. However, there are several disadvantages:
  - Minimum output voltage is V_{reg} instead of 0 V.
  - I_Q is relatively large and varies from chip to chip.
  - Power dissipation in R_2 can in some cases be quite large resulting in bulky and expensive equipment.
- A variety of 3-terminal variable regulators are available, e.g. LM317 (for +ve output) or LM 337 (for -ve output).

Switching Regulator



Block Diagram of Switch-Mode Regulator



It converts an unregulated dc input to a regulated dc output. Switching regulators are often referred to as dc to dc converters.

Comparing Switch-Mode to Linear Regulators

Advantages:

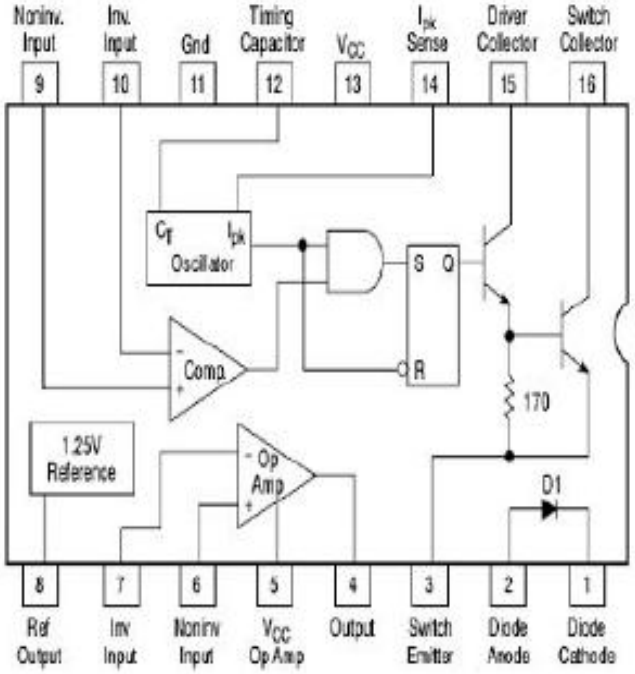
- 70–90% efficiency (about double that of linear ones)
- can make output voltage > input voltage, if desired
- can invert the input voltage
- considerable weight and size reductions, especially at high output power

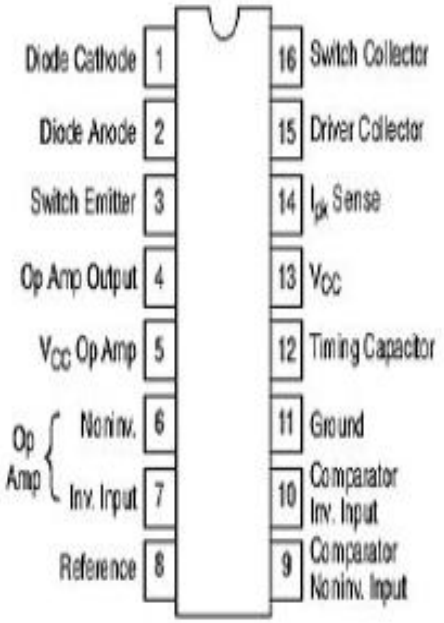
Disadvantages:

- More complex circuitry
- Potential EMI problems unless good shielding, low-loss ferrite cores and chokes are used

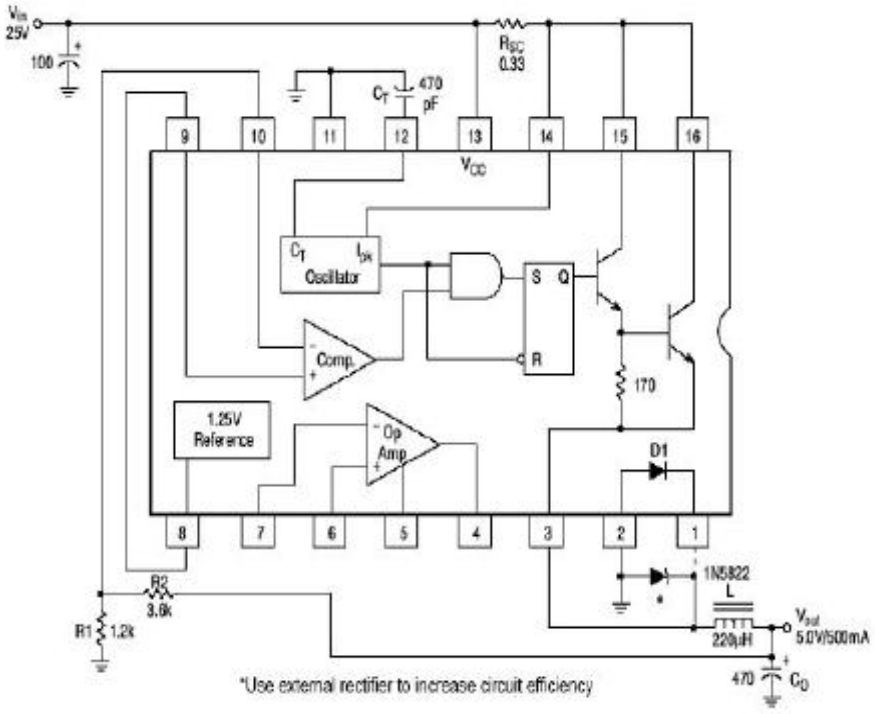
Monolithic Switching Regulator

[µA78S40]

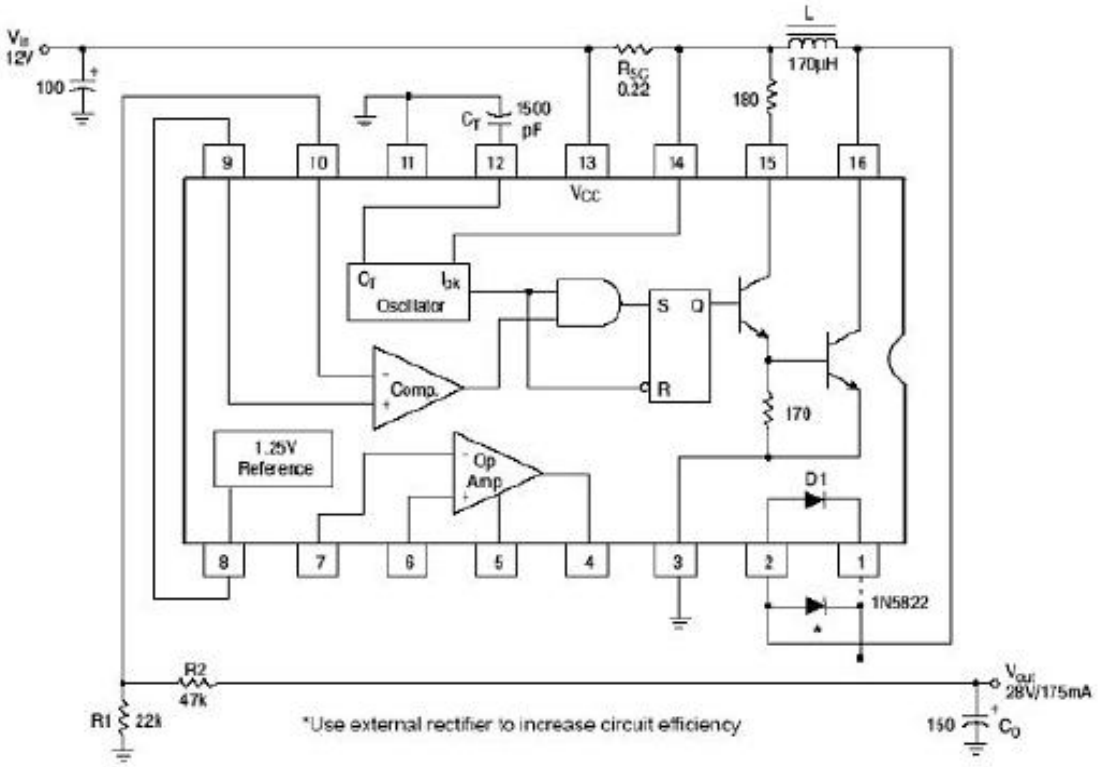




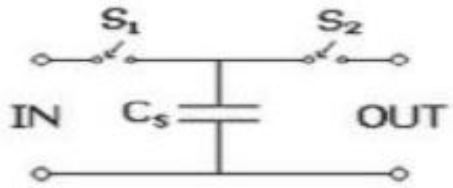
Step-Down converter



Step-Up Converter



Switched Capacitor Filter



$$q = CV$$

$$q_{IN} = C_S V_{IN}$$

$$q_{OUT} = C_S V_{OUT}$$

$$q = q_{OUT} - q_{IN} = C_S(V_{OUT} - V_{IN})$$

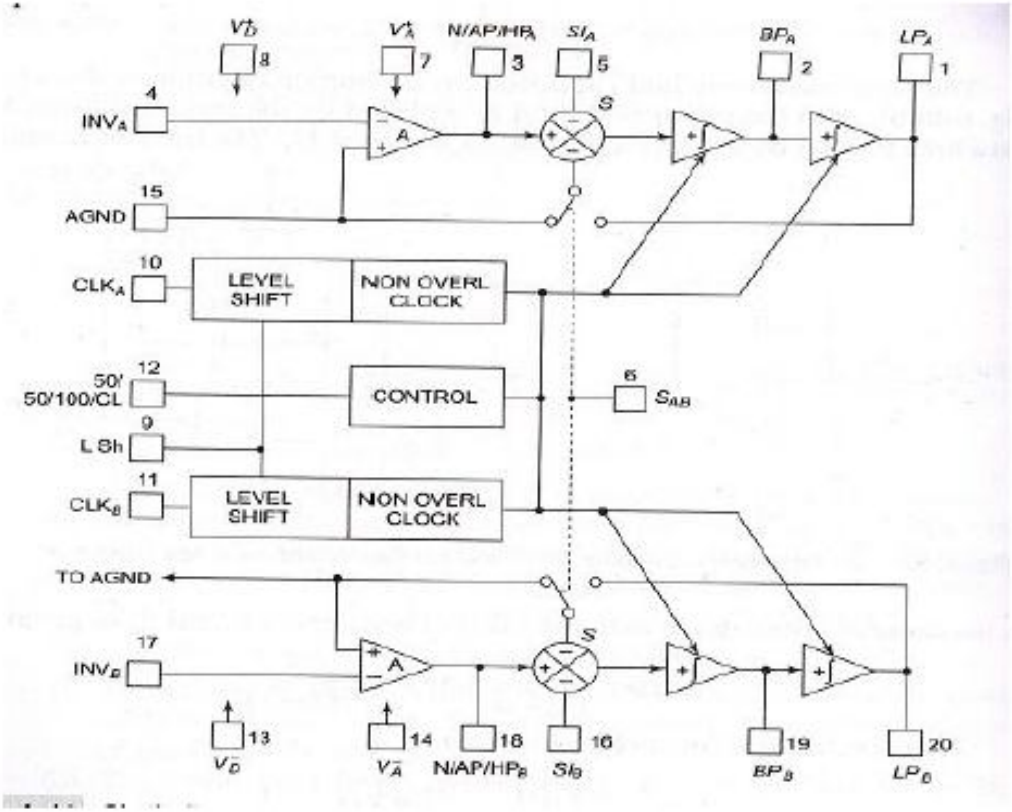
$$I = qf$$

$$I = C_S(V_{OUT} - V_{IN})f$$

$$V = V_{OUT} - V_{IN}$$

$$R = \frac{V}{I} = \frac{1}{C_S f}$$

Switched Capacitor Filter–MF10



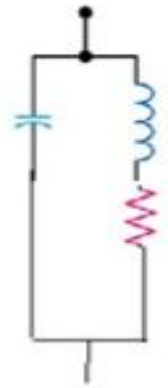
Tuned Amplifier

Tuned amplifiers

- To amplify the selective range of frequencies , the resistive load , Rc is replaced by a tuned circuit.
- The tuned circuit is capable of amplifying a signal over a narrow band of frequencies centered at fr.

$$f_r = \frac{1}{2\Pi\sqrt{LC}}$$

$$Z_r = \frac{L}{CR}$$



TYPES OF TUNED AMPLIFIERS

Single tuned amplifier

- one parallel tuned circuit is used as a load
- Limitation: Smaller Bandwidth , smaller gain bandwidth product, does not provide flatten response.

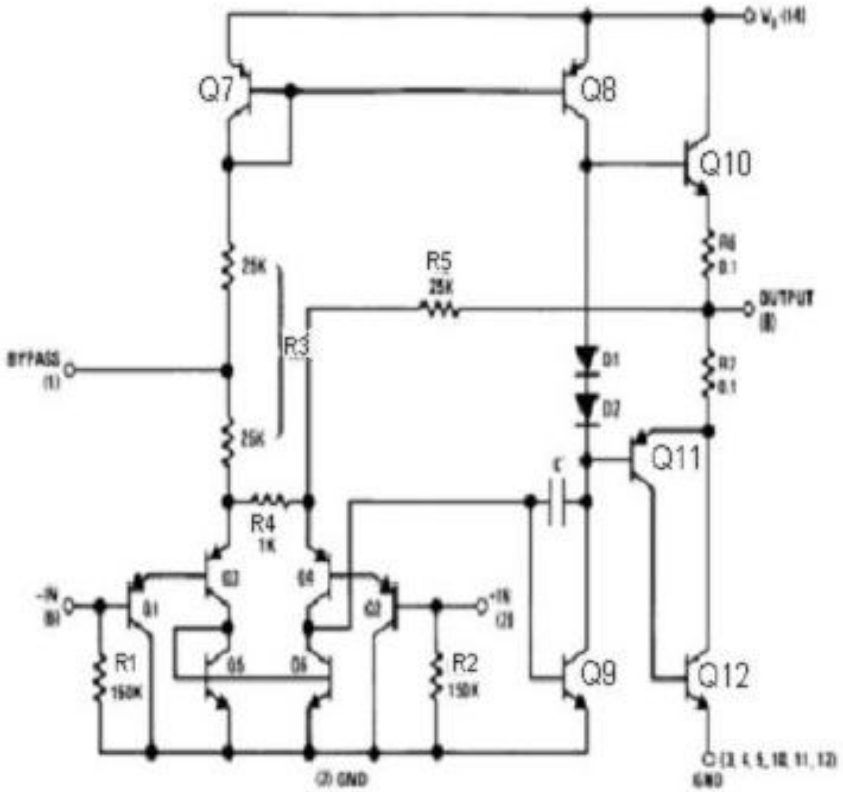
Double tuned amplifier

- It provides high gain, high selectivity and required bandwidth.
- Used in IF in radio and TV receivers.
- It gives greater 3db bandwidth having steep sides and flat top . But alignment of double tuned amplifier is difficult

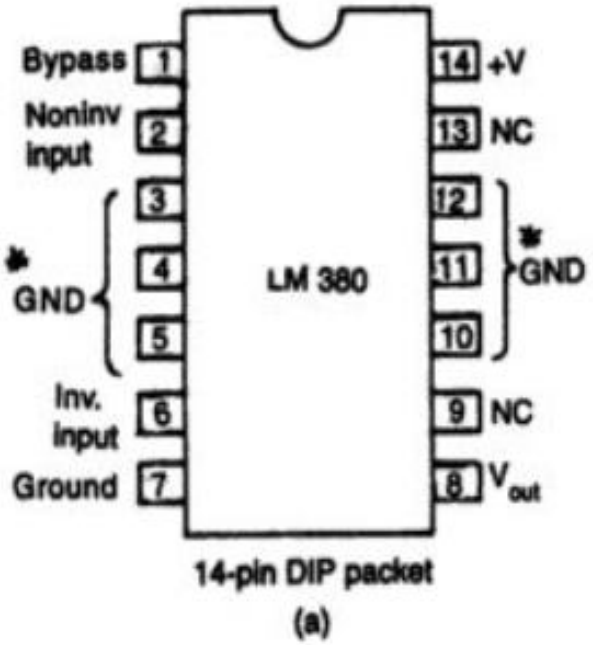
Stagger tuned amplifier

- Two single tuned amplifier are connected in cascaded form.
- Resonant frequency are displaced.
- To have better flat , wideband charcteristics with a very sharp rejective, narrow band characteristics.

Audio Power Amplifier

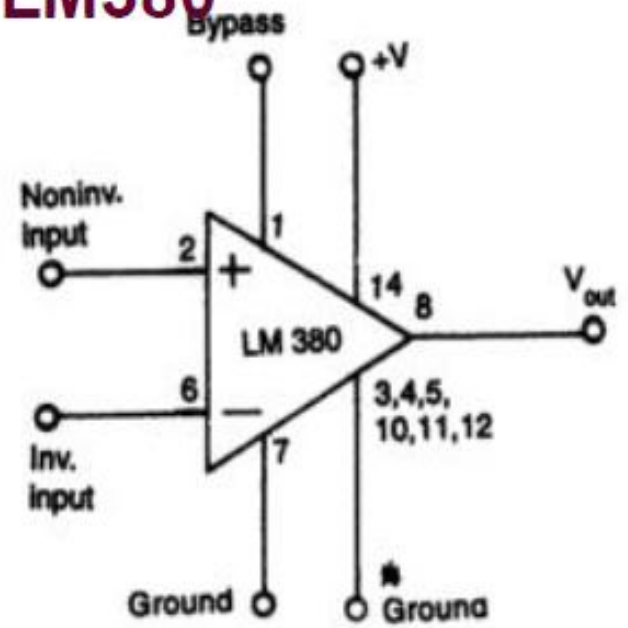


PIN DIAGRAM AND BLOCK DIAGRAM OF LM380



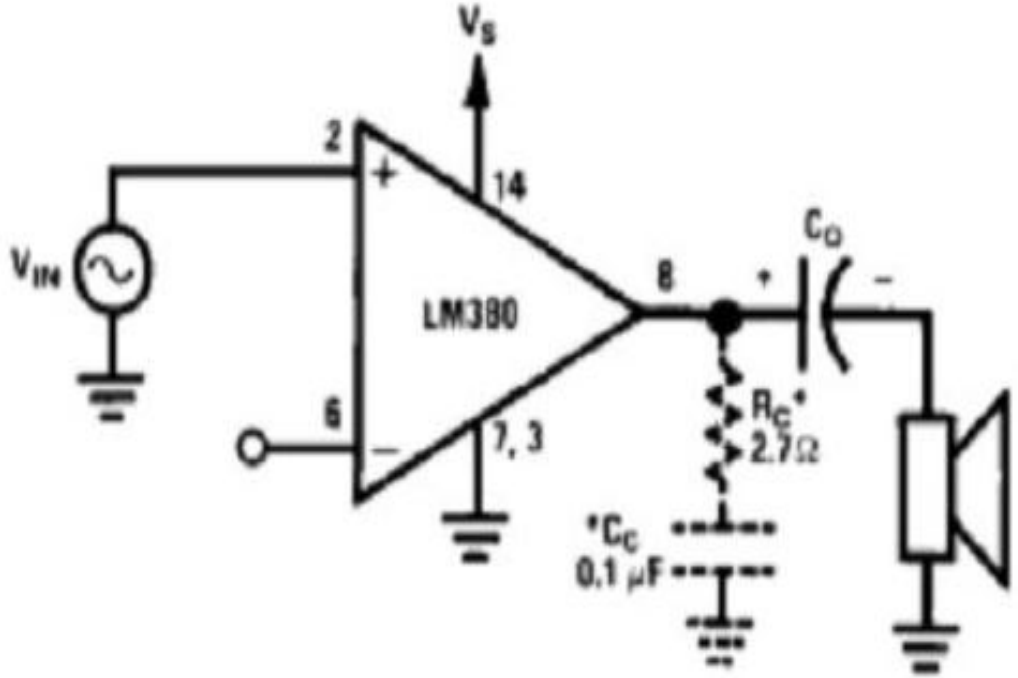
14-pin DIP packet

(a)



(b)

Audio Power Amplifier–LM380



Isolation Amplifier

- Provides a way to link a fixed ground to a floating ground.
- Isolates the DSP from the high voltage associated with the power amplifier.

ISOLATION AMPLIFIER

Purposes

- To break ground to permit incompatible circuits
- to be interfaced together while reducing noise
- To amplify signals while passing only low leakage current to prevent shock to people or damage to equipment
- To withstand high voltage to protect people, circuits, and equipment

OPTOCOUPLER

- The optocouplers provide protection and high-speed switching
- An optocoupler, also known as an opto-isolator, is an integral part of the opto electronics arena. It has fast proven its utility as an electrical isolator or a high-speed switch, and can be used in a variety of applications.
- The basic design for optocouplers involves use of an LED that produces a light signal to be received by a photodiode to detect the signal. In this way, the output current or current allowed to pass can be varied by the intensity of light.

Optoelectronic Integrated Circuits

Applications

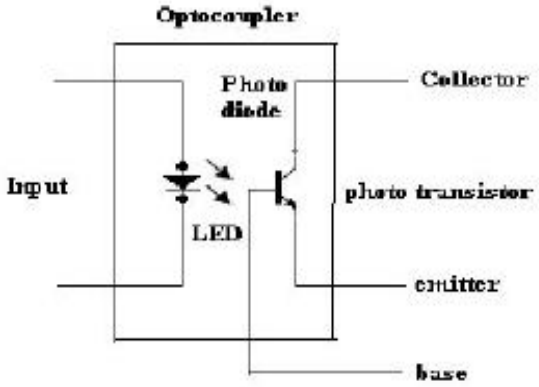
- Inter- and intra-chip optical interconnect and clock distribution
- Fiber transceivers
- Intelligent sensors
- Smart pixel array parallel processors

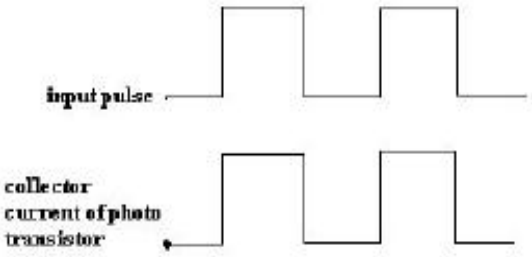
Optoelectronic Integrated Circuits

Approaches

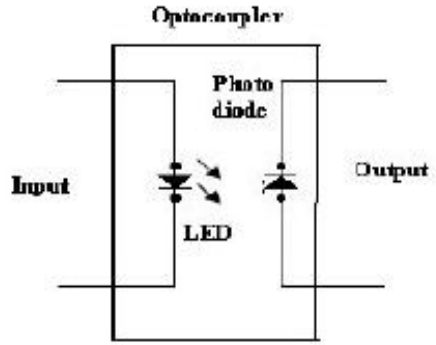
- Conventional hybrid assembly: multi-chip modules
- Total monolithic process development
- Modular integration on ICs:
- epitaxy-on-electronics
- flip-chip bump bonding w. substrate removal
- self-assembly

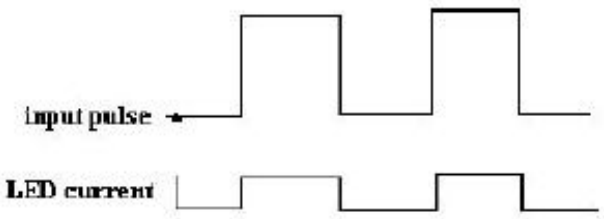
LED –Phototransistor Optocoupler



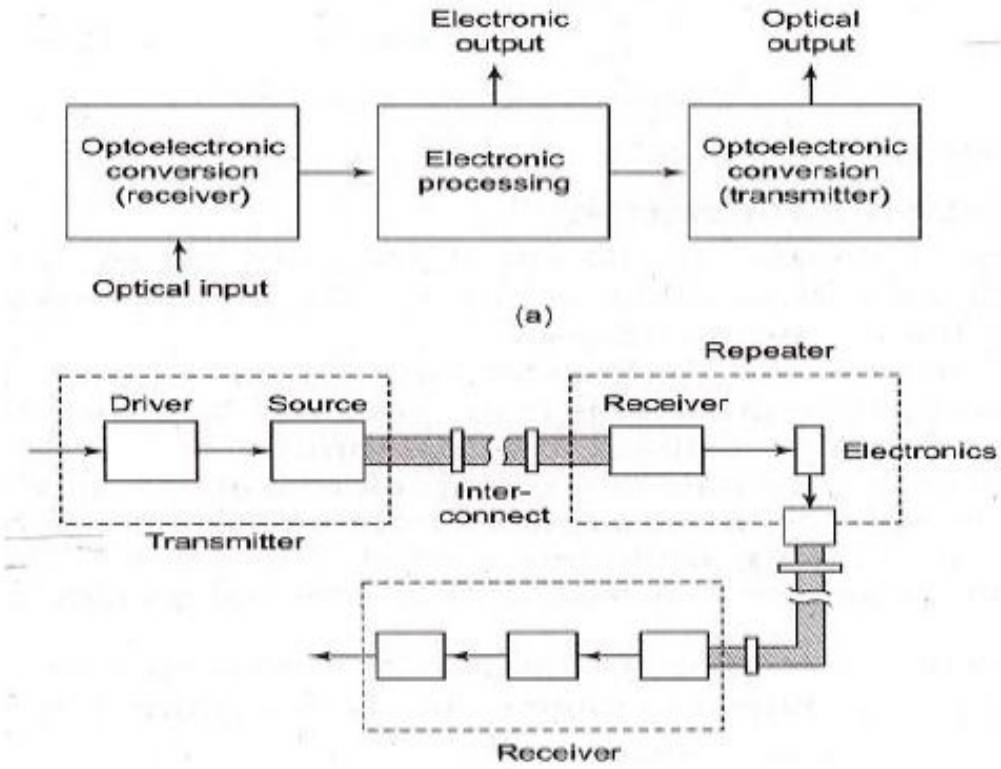


LED –Photodiode Optocoupler





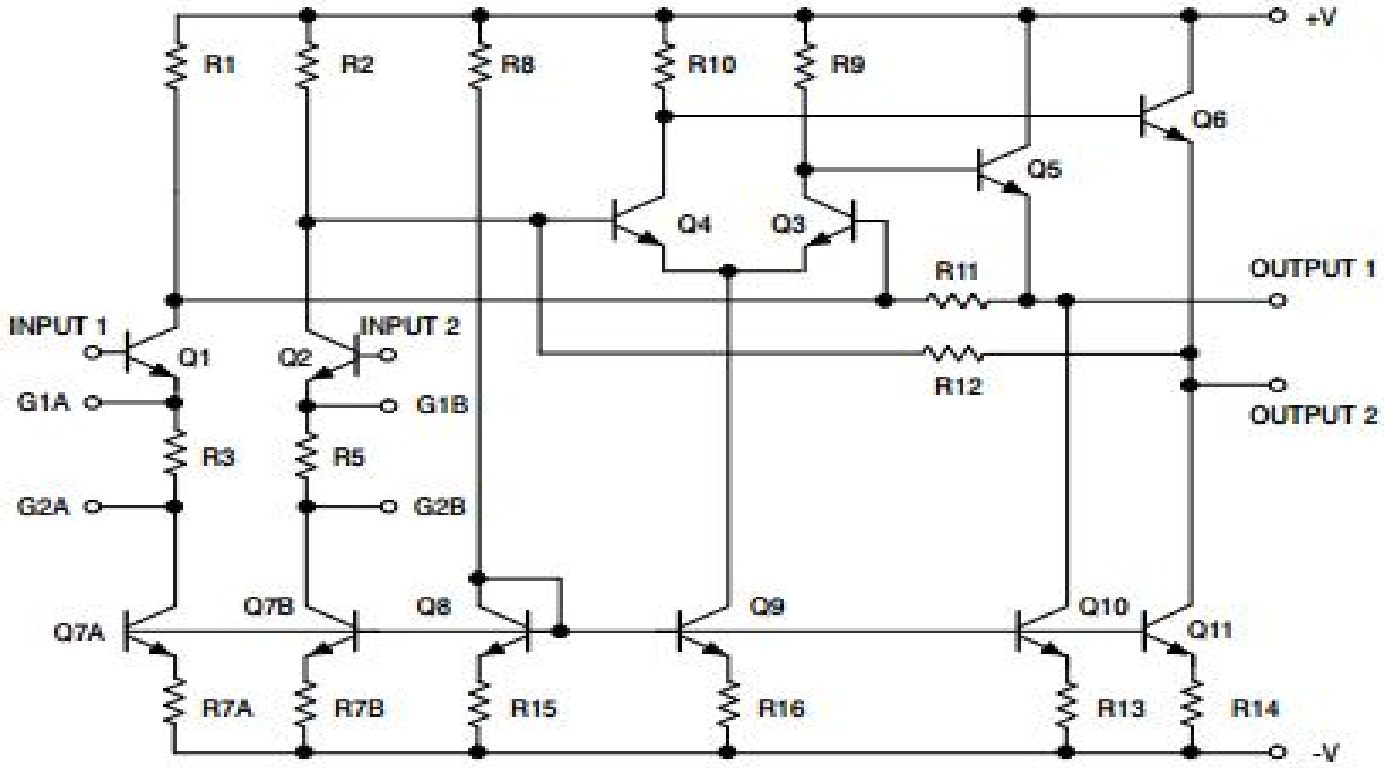
Optocoupler IC



Video Amplifiers

- The NE592 is a monolithic, two-stage, differential output, wideband video amplifier.
- It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor.
- The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter.
- This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.
- Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor

Block Diagram



Features and Applications

Features :

- 120 MHz Unity Gain Bandwidth
- Adjustable Gains from 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required
- Wave Shaping with Minimal External Components

Applications :

- Floppy Disk Head Amplifier
- Pulse Amplifier in Communications
- Magnetic Memory andVideo Recorder Systems

Voltage –Frequency Converter Circuit

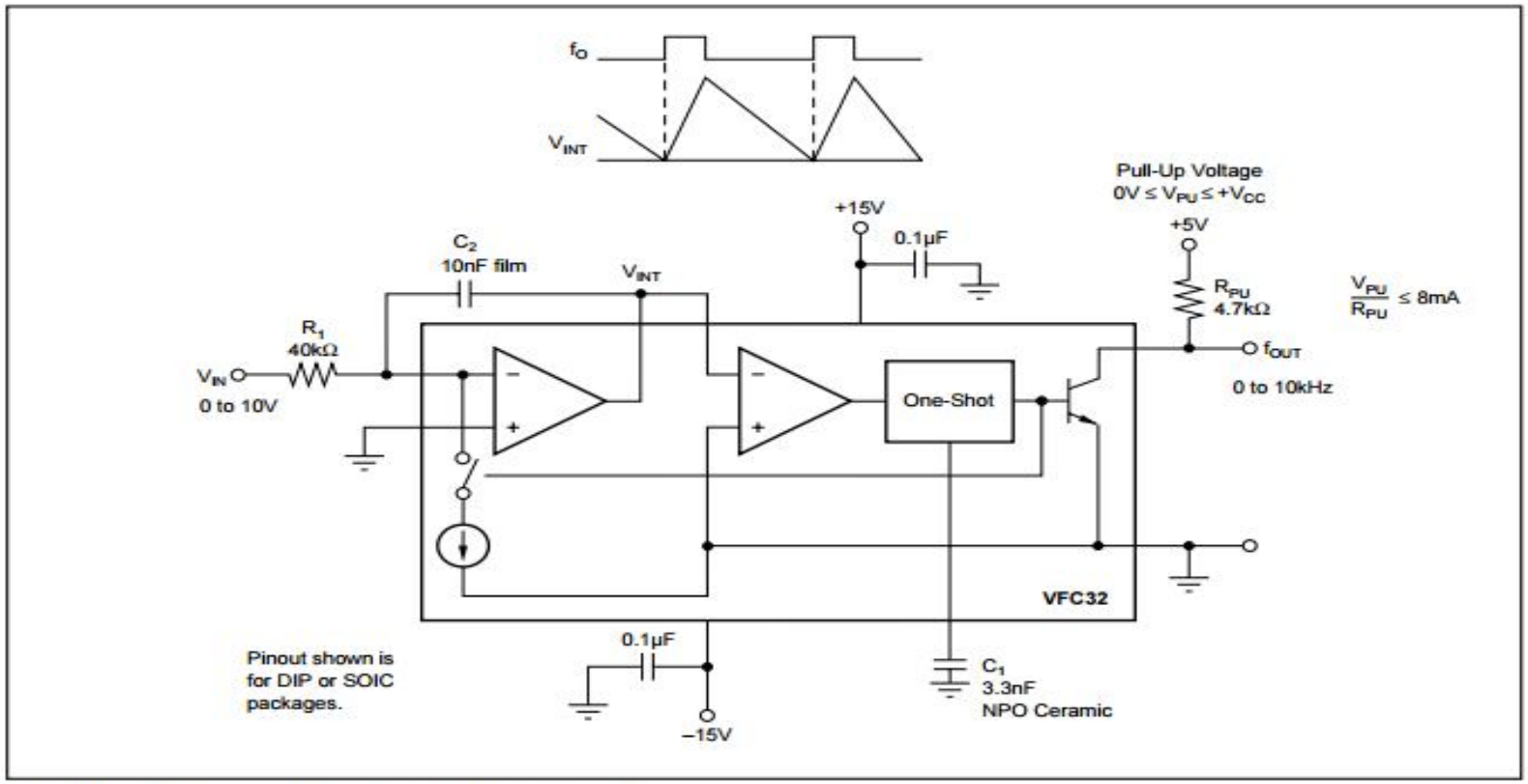


FIGURE 1. Voltage-to-Frequency Converter Circuit.

Frequency –Voltage Converter Circuit

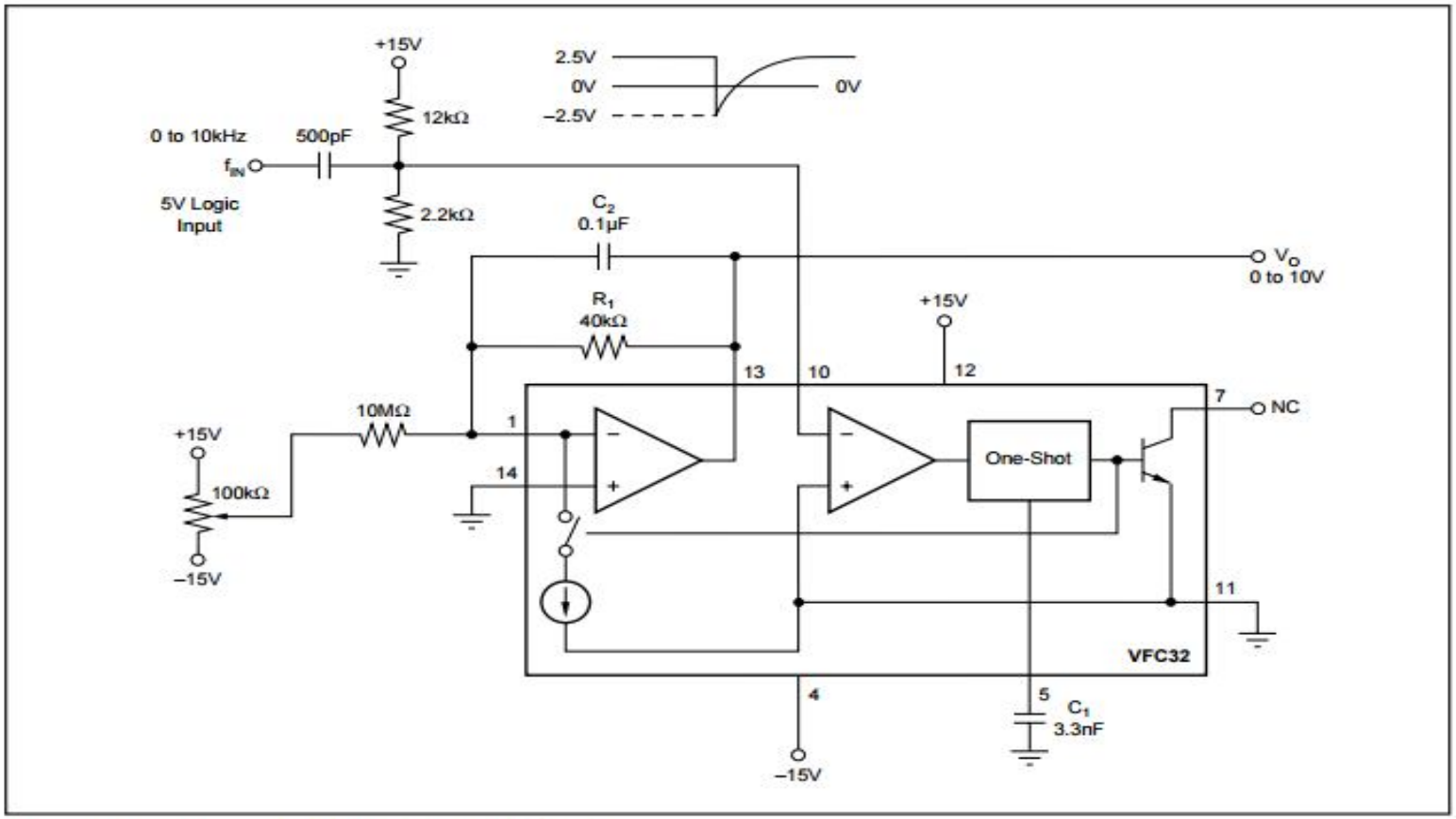
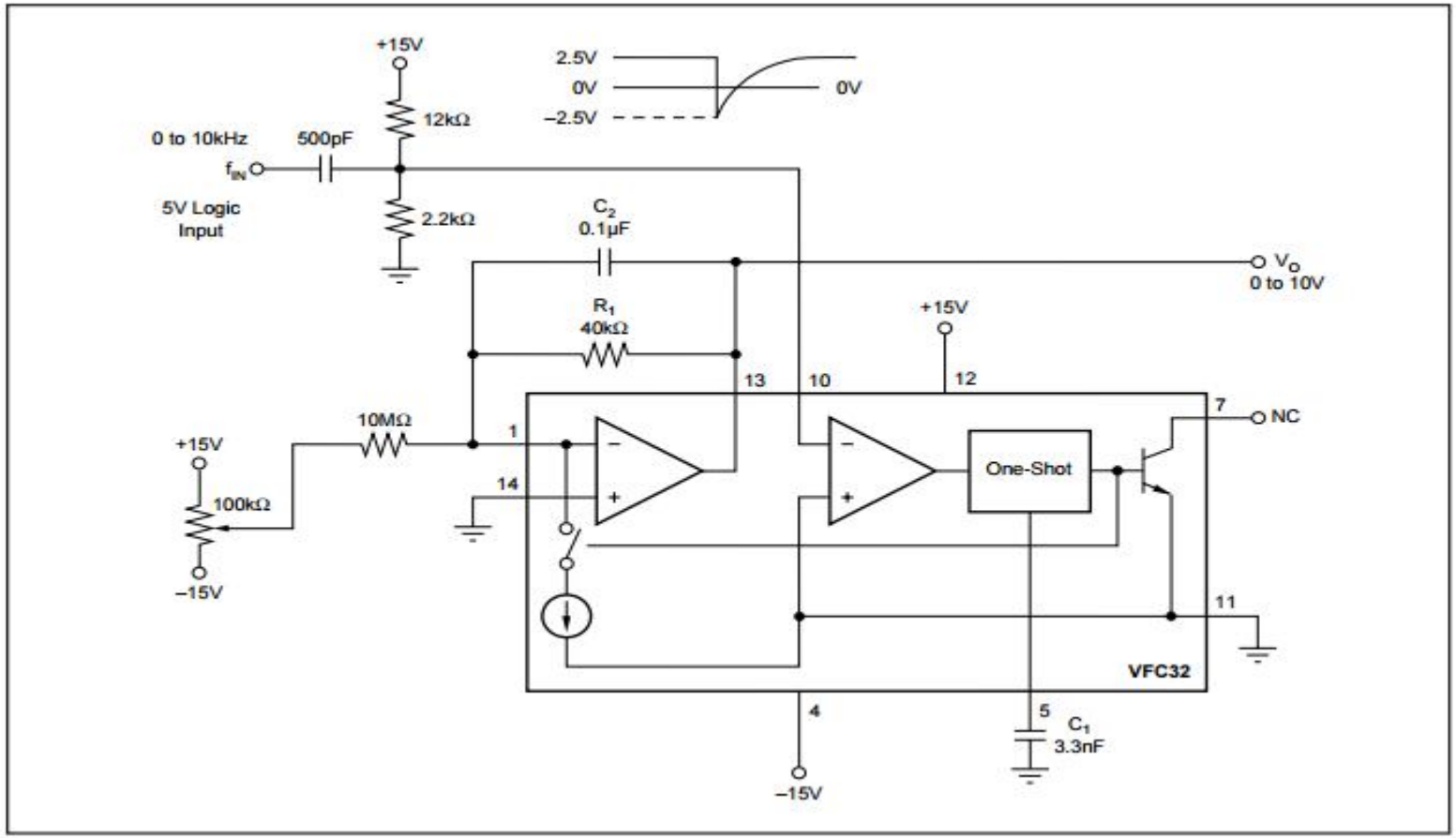


FIGURE 4. Frequency-to-Voltage Converter Circuit.

Frequency to Voltage Converter - Circuit



Sources of Noise in Op-amp

- Thermal noise - Brownian motion of atoms, molecules, ions.
- Shot noise – random movement of electrons or holes across a Pnjunction
- Transmit time noise – Propagation time of current carriers causes noise, especially at high frequencies
- Quantization noise

Low Noise Op-amps

Why do we need low noise op amps?

Dynamic range:

Signal-to-noise ratio (*SNR*)

$$= \frac{\text{Maximum RMS Signal}}{\text{Noise}}$$

(*SNDR* includes both noise and distortion)

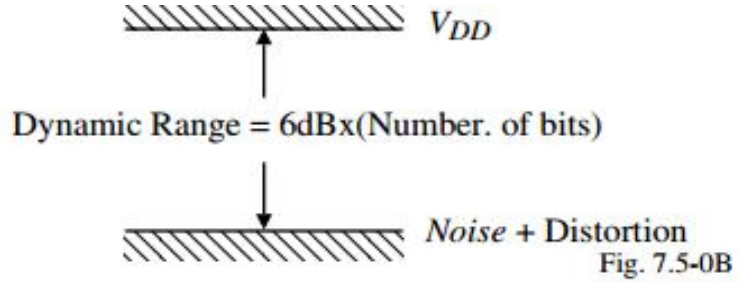


Fig. 7.5-0B

Consider a 14 bit digital-to-analog converter with a 1V reference with a bandwidth of 1MHz.

Maximum RMS signal is $\frac{0.5\text{V}}{\sqrt{2}} = 0.3535$ Vrms

A 14 bit D/A converter requires 14x6dB dynamic range or 84 dB or 16,400.

$\therefore$ The value of the least significant bit (*LSB*) $= \frac{0.3535}{16{,}400} = 21.6\mu\text{Vrms}$

If the equivalent input noise of the op amp is not less than this value, then the *LSB* cannot be resolved and the D/A converter will be in error. An op amp with an equivalent input-noise spectral density of $10\text{nV}/\sqrt{\text{Hz}}$ will have an rms noise voltage of approximately $(10\text{nV}/\sqrt{\text{Hz}})(1000\sqrt{\text{Hz}}) = 10\mu\text{Vrms}$ in a 1MHz bandwidth.

Op-amp Noise Analysis

Minimization of Noise in Op Amps

1.) Maximize the signal gain as close to the input as possible. (As a consequence, only the input stage will contribute to the noise of the op amp.)

2.) To minimize the 1/f noise:

   a.) Use PMOS input transistors with appropriately selected dc currents and W and L values.

   b.) Use lateral BJTs to eliminate the $1/f$ noise.

   c.) Use chopper stabilization to reduce the low-frequency noise.

Noise Analysis

1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)

2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.

3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.